High Efficiency Low Noise Synchronous Step-Down Switching Regulators

FEATURES

- **Maintains Constant Frequency at Low Output Currents**
- Dual N-Channel MOSFET Synchronous Drive
- **Programmable Fixed Frequency (PLL Lockable)**
- **Wide V_{IN} Range: 3.5V to 36V Operation**
- Ultrahigh Efficiency
- Very Low Dropout Operation: 99% Duty Cycle
- Low Dropout, 0.5A Linear Regulator for VPP Generation or Low Noise Audio Supply
- Built-In Power-On Reset Timer
- Programmable Soft Start
- Low-Battery Detector
- Remote Output Voltage Sense
- Foldback Current Limiting (Optional)
- Pin Selectable Output Voltage
- Logic Controlled Micropower Shutdown: $I_Q < 25\mu A$
- Output Voltages from 1.19V to 9V
- Available in 24-Lead Narrow SSOP and 28-Lead SSOP Packages

APPLICATIONS

- Notebook and Palmtop Computers, PDAs
- Cellular Telephones and Wireless Modems
- Portable Instruments
- Battery-Operated Devices
- DC Power Distribution Systems

DESCRIPTION

The LTC®1436/LTC1437 are synchronous step-down switching regulator controllers which drive external N-channel power MOSFETs in a phase lockable, fixed frequency architecture. The Adaptive Power™ output stage selectively drives two N-channel MOSFETs at frequencies up to 400kHz while reducing switching losses to maintain high efficiencies at low output currents.

An auxiliary 0.5A linear regulator using an external PNP pass device provides a low noise, low dropout voltage source. A secondary winding feedback control pin (SFB) guarantees regulation regardless of load on the main output by forcing continuous operation.

An additional comparator is available for use as a low-battery detector. A power-on reset timer (POR) is included which generates a signal delayed by $65536/f_{CLK}$ (300ms typically) after the output is within 5% of the regulated output voltage. Internal resistive dividers provide pin selectable output voltages with remote sense capability.

The operating current level is user-programmable via an external current sense resistor. Wide input supply range allows operation from 3.5V to 30V (36V maximum).

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TYPICAL APPLICATION

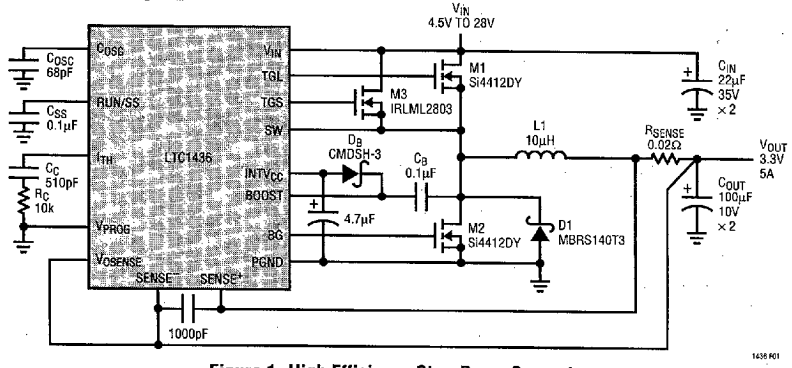
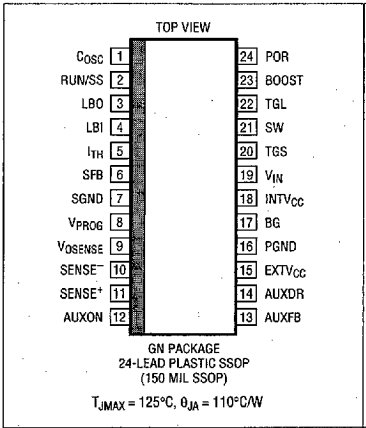


Figure 1. High Efficiency Step-Down Converter

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (V_{IN}) ..... 36V to –0.3V
Topside Driver Supply Voltage (Boost) ..... 42V to –0.3V
Switch Voltage (SW) ..... V_{IN} + 5V to –5V
$EXTV_{CC}$ Voltage ..... 10V to –0.3V
POR, LBO Voltages ..... 12V to –0.3V
AUXFB Voltage ..... 20V to –0.3V
AUXDR Voltage ..... 28V to –0.3V
SENSE+, SENSE–,
V_{OSENSE} Voltages ..... $INTV_{CC}$ + 0.3V to –0.3V
V_{PROG} Voltage ..... $INTV_{CC}$ to –0.3V
PLL LPF, I_{TH} Voltages ..... 2.7V to –0.3V
AUXON, PLLIN, SFB,
RUN/SS, LBI Voltages ..... 10V to –0.3V
Peak Driver Output Current < 10µs (TGL, BG) 2A
Peak Driver Output Current < 10µs (TGS) 250mA
$INTV_{CC}$ Output Current 50mA
Operating Temperature Range
LTC143XC ..... 0°C to 70°C
LTC143XI ..... –40°C to 85°C
Junction Temperature (Note 1) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

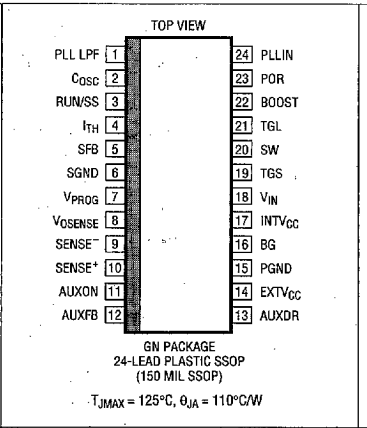


GN PACKAGE
24-LEAD PLASTIC SSOP
(150 MIL SSOP)

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER

LTC1436CGN
LTC1436IGN

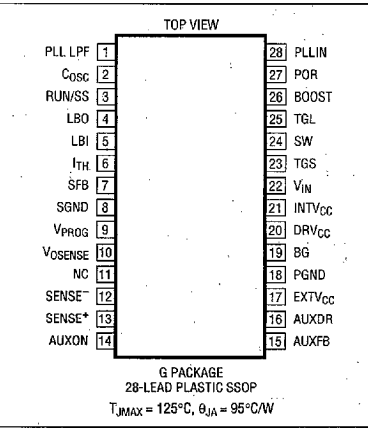


GN PACKAGE
24-LEAD PLASTIC SSOP
(150 MIL SSOP)

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER

LTC1436CGN-PLL
LTC1436IGN-PLL



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC1437CG
LTC1437IG

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 15V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
I_{IN} V_{OSENSE}	Feedback Current	V_{PROG} Pin Open (Note 2)			10	50	nA
V_{OUT}	Regulated Output Voltage	(Note 2)					
	1.19V (Adjustable) Selected	V_{PROG} Pin Open	●	1.178	1.19	1.202	V
	3.3V Selected	V_{PROG} = 0V	●	3.220	3.30	3.380	V
	5V Selected	V_{PROG} = $INTV_{CC}$	●	4.900	5.00	5.100	V

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 15V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{LINEREG}$	Reference Voltage Line Regulation	V_{IN} = 3.6V to 20V (Note 2), V_{PROG} Pin Open			0.002	0.01	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	I_{TH} Sinking 5µA (Note 2)	●		0.5	0.8	%
		I_{TH} Sourcing 5µA (Note 2)	●		−0.5	−0.8	%
V_{SFB}	Secondary Feedback Threshold	V_{SFB} Ramping Negative	●	1.16	1.19	1.22	V
I_{SFB}	Secondary Feedback Current	V_{SFB} = 1.5V			−1	−2	µA
V_{OVL}	Output Overvoltage Lockout	V_{PROG} Pin Open		1.24	1.28	1.32	V
I_{PROG}	V_{PROG} Input Current						
		0.5V > V_{PROG}			−3	−6	µA
		$INTV_{CC}$ − 0.5V < V_{PROG} < $INTV_{CC}$			3	6	µA
I_Q	Input DC Supply Current	$EXTV_{CC}$ = 5V (Note 3)					
	Normal Mode	3.6V < V_{IN} < 30V, V_{AUXON} = 0V			260		µA
	Shutdown	$V_{RUN/SS}$ = 0V, 3.6V < V_{IN} < 15V			16	25	µA
$V_{RUN/SS}$	RUN Pin Threshold		●	0.8	1.3	2	V
$I_{RUN/SS}$	Soft Start Current Source	$V_{RUN/SS}$ = 0V		1.5	3	4.5	µA
$\Delta V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{OSENSE} = 0V, 5V, V_{PROG} Pin Open		130	150	180	mV
	TGL Transition Time						
TGL t_r	Rise Time	C_{LOAD} = 3000pF			50	150	ns
TGL t_f	Fall Time	C_{LOAD} = 3000pF			50	150	ns
	TGS Transition Time						
TGS t_r	Rise Time	C_{LOAD} = 500pF			90	150	ns
TGS t_f	Fall Time	C_{LOAD} = 500pF			50	150	ns
	BG Transition Time						
BG t_r	Rise Time	C_{LOAD} = 3000pF			50	150	ns
BG t_f	Fall Time	C_{LOAD} = 3000pF			40	150	ns
Internal V_{CC} Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 30V, V_{EXTVCC} = 4V	●	4.8	5.0	5.2	V
$V_{LDO\ INT}$	$INTV_{CC}$ Load Regulation	I_{INTVCC} = 15mA, V_{EXTVCC} = 4V			−0.2	−1	%
$V_{LDO\ EXT}$	$EXTV_{CC}$ Voltage Drop	I_{INTVCC} = 15mA, V_{EXTVCC} = 5V			130	230	mV
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	I_{INTVCC} = 15mA, V_{EXTVCC} Ramping Positive	●	4.5	4.7		V
Oscillator and Phase-Locked Loop							
f_{OSC}	Oscillator Frequency	C_{OSC} = 100pF, LTC1436 (Note 4),		112	125	138	kHz
		LTC1436-PLL/LTC1437, V_{PLLLPF} = 0V					
	VCO High	LTC1436-PLL/LTC1437, V_{PLLLPF} = 2.4V		200	240		kHz
R_{PLLIN}	PLL IN Input Resistance				50		kΩ
I_{PLLLPF}	Phase Detector Output Current						
	Sinking Capability	f_{PLLIN} < f_{OSC}		10	15	20	µA
	Sourcing Capability	f_{PLLIN} > f_{OSC}		10	15	20	µA
Power-On Reset							
V_{SATPOR}	POR Saturation Voltage	I_{POR} = 1.6mA, V_{OSENSE} = 1V, V_{PROG} Pin Open			0.6	1	V
I_{LPOR}	POR Leakage	V_{POR} = 12V, V_{OSENSE} = 1.2V, V_{PROG} Pin Open			0.2	1	µA
V_{THPOR}	POR Trip Voltage	V_{PROG} Pin Open, V_{OSENSE} Ramping Negative		−11	−7.5	−4	%
t_{DPOR}	POR Delay	V_{PROG} Pin Open			65536		Cycles

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 15V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Battery Comparator							
V_{SATLBO}	LBO Saturation Voltage	I_{LBO} = 1.6mA, V_{LBI} = 1.1V			0.6	1	V
I_{LLBO}	LBO Leakage	V_{LBO} = 12V, V_{LBI} = 1.4V	●		0.01	1	µA
V_{THLBI}	LBI Trip Voltage	High to Low Transition on LBO	●	1.16	1.19	1.22	V
I_{INLBI}	LBI Input Current	V_{LBI} = 1.19V	●		1	50	nA
V_{HYSLBO}	LBO Hysteresis				20		mV
Auxiliary Regulator/Comparator							
I_{AUXDR}	AUXDR Current Max Current Sinking Capability Control Current Leakage When Off	V_{EXTVCC} = 0V V_{AUXDR} = 4V, V_{AUXFB} = 1.0V, V_{AUXON} = 5V V_{AUXDR} = 5V, V_{AUXFB} = 1.5V, V_{AUXON} = 5V V_{AUXDR} = 24V, V_{AUXFB} = 1.5V, V_{AUXON} = 0V		10	15 1 0.01	 5 1	mA µA µA
$I_{IN\ AUXFB}$	AUXFB Input Current	V_{AUXFB} = 1.19V, V_{AUXON} = 5V			0.01	1	µA
$I_{IN\ AUXON}$	AUXON Input Current	V_{AUXON} = 5V			0.01	1	µA
$V_{TH\ AUXON}$	AUXON Trip Voltage	V_{AUXDR} = 4V, V_{AUXFB} = 1.0V		1.0	1.19	1.4	V
$V_{SAT\ AUXDR}$	AUXDR Saturation Voltage	I_{AUXDR} = 1.6mA, V_{AUXFB} = 1.0V, V_{AUXON} = 5V			0.4	0.8	V
V_{AUXFB}	AUXFB Voltage	V_{AUXON} = 5V, 11V < V_{AUXDR} < 24V (Note 5) V_{AUXON} = 5V, 3V < V_{AUXDR} < 7V (Note 5)	● ●	11.5 1.14	12 1.19	12.5 1.24	V V
$V_{TH\ AUXDR}$	AUXFB Divider Disconnect Voltage	V_{AUXON} = 5V (Note 5), Ramping Negative		7.5	8.5	9.5	V

The ● denotes specifications which apply over the full operating temperature range.

LTC1436CGN/LTC1436CGN-PLL/LTC1437CG: 0°C ≤ T_A ≤ 70°C

LTC1436IGN/LTC1436IGN-PLL/LTC1437IG: –40°C ≤ T_A ≤ 85°C

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC1436CGN/LTC1436CGN-PLL/LTC1436IGN/LTC1436IGN-PLL: $T_J = T_A + (P_D)(110\ °C/W)$

LTC1437CG/LTC1437IG: $T_J = T_A + (P_D)(95\ °C/W)$

Note 2: The LTC1436/LTC1437 are tested in a feedback loop which servos V_{OSENSE} to the balance point for the error amplifier (V_{ITH} = 1.19V).

Note 3: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information section.

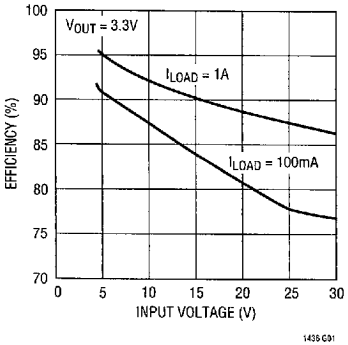
Note 4: Oscillator frequency is tested by measuring the C_{OSC} charge and discharge currents and applying the formula:

$$f_{OSC}\ (kHz) = \left(\frac{8.4(10^8)}{C_{OSC}\ (pF) + 11}\right)\left(\frac{1}{I_{CHG}} + \frac{1}{I_{DIS}}\right)^{-1}$$

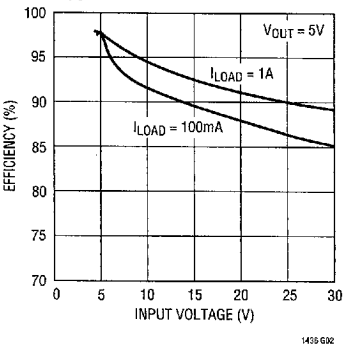
Note 5: The Auxiliary Regulator is tested in a feedback loop which servos V_{AUXFB} to the balance point for the error amplifier. For applications with V_{AUXDR} > 9.5V, V_{AUXFB} uses an internal resistive divider. See Applications Information.

TYPICAL PERFORMANCE CHARACTERISTICS

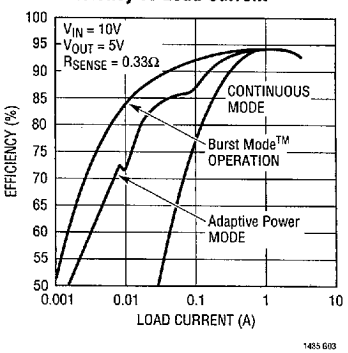
Efficiency vs Input Voltage
V_{OUT} = 3.3V



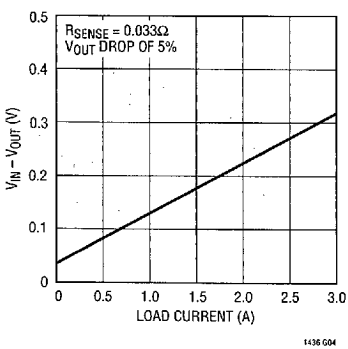
Efficiency vs Input Voltage
V_{OUT} = 5V



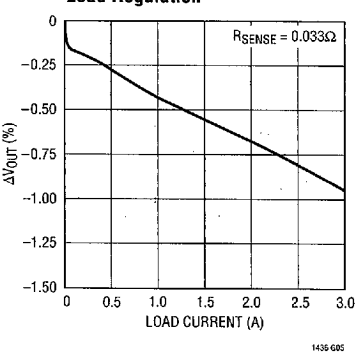
Efficiency vs Load Current



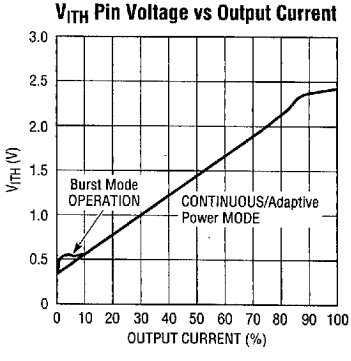
V_{IN} – V_{OUT} Dropout Voltage vs Load Current



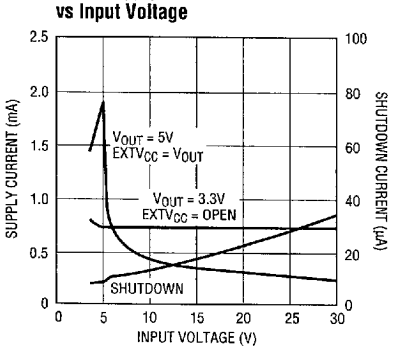
Load Regulation



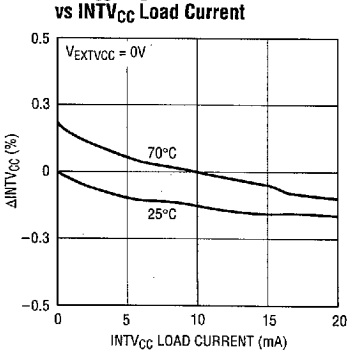
V_{ITH} Pin Voltage vs Output Current



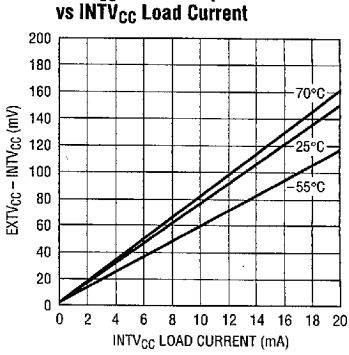
Input Supply Current vs Input Voltage



$INTV_{CC}$ Regulation vs $INTV_{CC}$ Load Current



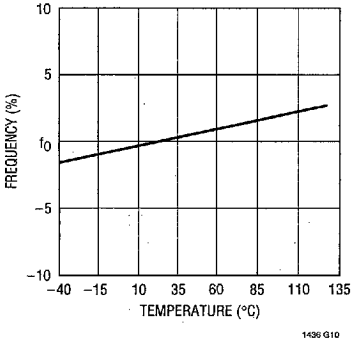
$EXTV_{CC}$ Switch Drop vs $INTV_{CC}$ Load Current



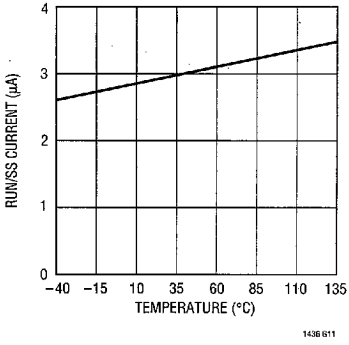
Burst Mode is a trademark of Linear Technology Corporation.

TYPICAL PERFORMANCE CHARACTERISTICS

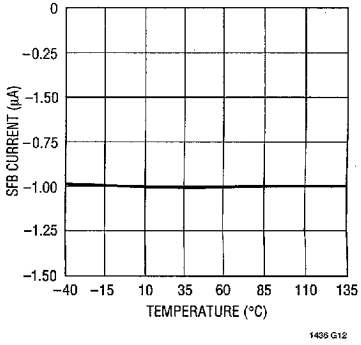
Normalized Oscillator Frequency vs Temperature



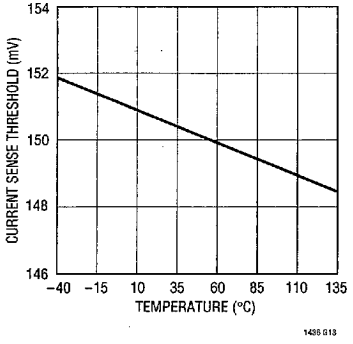
RUN/SS Pin Current vs Temperature



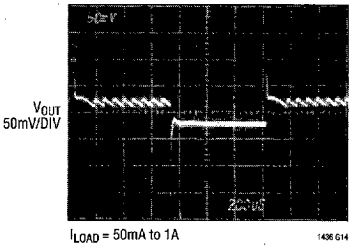
SFB Pin Current vs Temperature



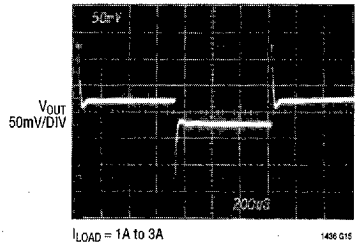
Maximum Current Sense Threshold Voltage vs Temperature



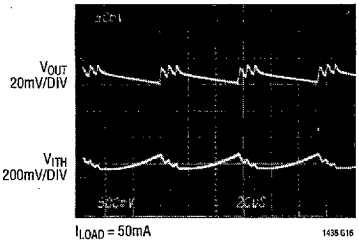
Transient Response



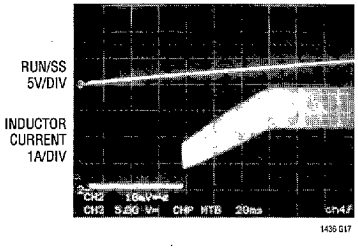
Transient Response



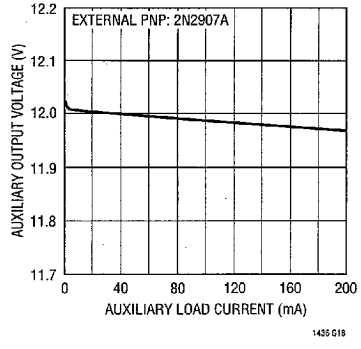
Burst Mode Operation



Soft Start: Load Current vs Time

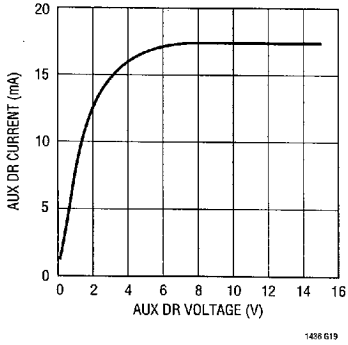


Auxiliary Regulator Load Regulation

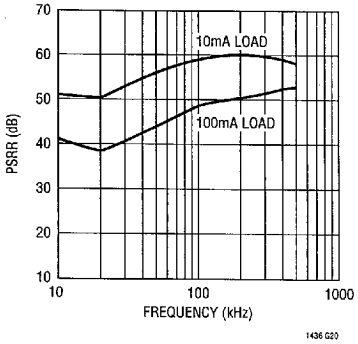


TYPICAL PERFORMANCE CHARACTERISTICS

Auxiliary Regulator Sink Current Available



Auxiliary Regulator PSRR



PIN FUNCTIONS

V_{IN}: Main Supply Pin. Must be closely decoupled to the IC's signal ground pin.

$INTV_{CC}$: Output of the Internal 5V Regulator and $EXTV_{CC}$ Switch. The driver and control circuits are powered from this voltage. Must be closely decoupled to power ground with a minimum of 2.2µF tantalum or electrolytic capacitor.

DRV_{CC}: Bottom MOSFET Driver Supply Voltage.

$EXTV_{CC}$: Input to the Internal Switch Connected to $INTV_{CC}$. This switch closes and supplies V_{CC} power whenever $EXTV_{CC}$ is higher than 4.7V. See $EXTV_{CC}$ connection in Applications Information section. Do not exceed 10V on this pin. Connect to V_{OUT} if $V_{OUT} \geq 5V$.

BOOST: Supply to Topside Floating Driver. The bootstrap capacitor is returned to this pin. Voltage swing at this pin is from $INTV_{CC}$ to $V_{IN} + INTV_{CC}$.

SW: Switch Node Connection to Inductor. Voltage swing at this pin is from a Schottky diode (external) voltage drop below ground to V_{IN}.

SGND: Small Signal Ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

PGND: Driver Power Ground. Connects to source of bottom N-channel MOSFET and the (–) terminal of C_{IN}.

$SENSE^-$: The (–) Input to the Current Comparator.

$SENSE^+$: The (+) Input to the Current Comparator. Built-in offsets between $SENSE^-$ and $SENSE^+$ pins in conjunction with R_{SENSE} set the current trip thresholds.

V_{OSENSE}: Receives the remotely sensed feedback voltage either from the output or from an external resistive divider across the output. The V_{PROG} pin determines which point V_{OSENSE} must connect to.

V_{PROG}: This voltage selects the output voltage. For $V_{PROG} < V_{INTVCC}/3$ the output is set to 3.3V with V_{OSENSE} connected to the output. With $V_{PROG} > V_{INTVCC}/1.5$ the output is set to 5V with V_{OSENSE} connected to the output. Leaving V_{PROG} open (DC) allows the output voltage to be set by an external resistive divider connected to V_{OSENSE}.

C_{OSC}: External capacitor C_{OSC} from this pin to ground sets the operating frequency.

I_{TH}: Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 2.5V.

RUN/SS: Combination of Soft Start and Run Control Inputs. A capacitor to ground at this pin sets the ramp time to full current output. The time is approximately 0.5s/µF.

PIN FUNCTIONS

Forcing this pin below 1.3V causes the device to be shut down. In shutdown all functions are disabled.

TGL: High Current Gate Drive for Main Top N-Channel MOSFET. This is the output of a floating driver with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW.

TGS: High Current Gate Drive for a Small Top N-Channel MOSFET. This is the output of a floating driver with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW. Leaving TGS open invokes Burst Mode operation at low load currents.

BG: High Current Gate Drive for Bottom N-Channel MOSFET. Voltage swing at this pin is from ground to $INTV_{CC}$ (DRV_{CC}).

SFB: Secondary Winding Feedback Input. Normally connected to a feedback resistive divider from the secondary winding. This pin should be tied to: ground to force continuous operation; $INTV_{CC}$ in applications that don't use a secondary winding; and a resistive divider from the output in applications using a secondary winding.

POR: Open Drain Output of an N-Channel Pull-Down. This pin sinks current when the output voltage is 7.5% out of regulation and releases 65536 oscillator cycles after the output voltage rises to –5% of its regulated value. The POR output is asserted when Run/SS is low independent of V_{OUT}.

LBO: Open Drain Output of an N-Channel Pull-Down. This pin will sink current when the LBI pin goes below 1.19V.

LBI: The (+) Input of the Low Battery Voltage Comparator. The (–) input is connected to a 1.19V reference.

PLLIN: External Synchronizing Input to Phase Detector. This pin is internally terminated to SGND with 50kΩ. Tie this pin to SGND in applications which do not use the phase-locked loop.

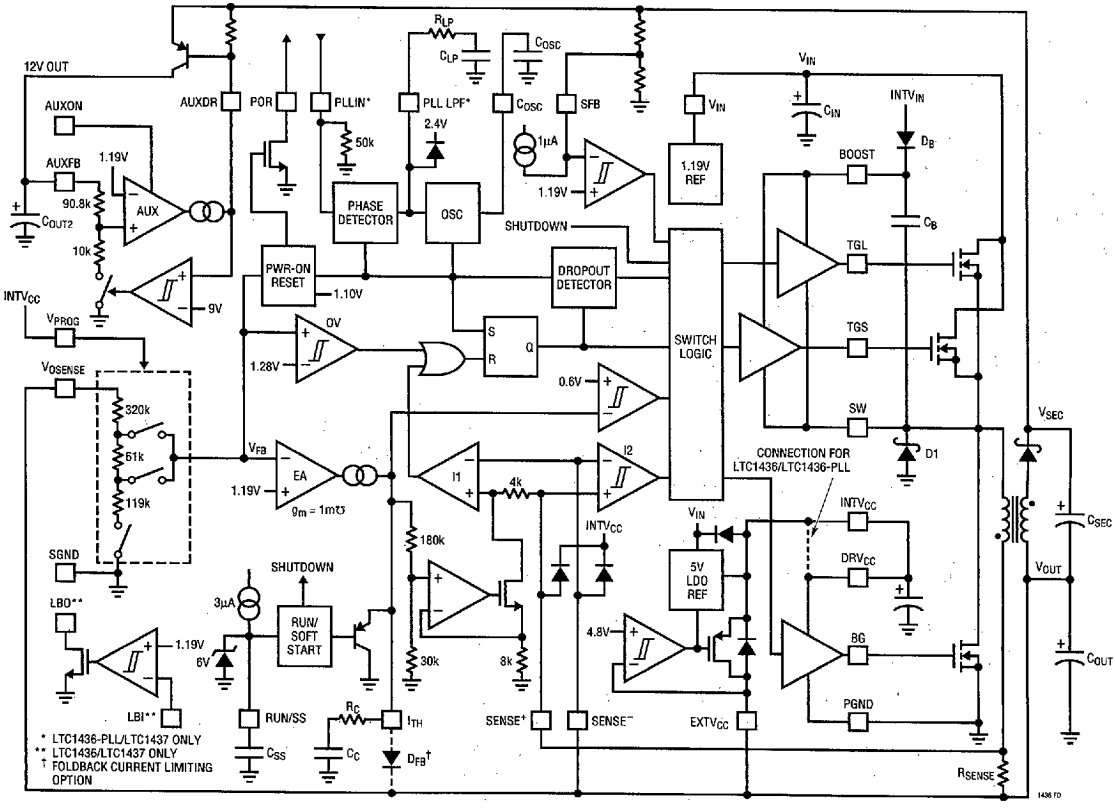
PLL LPF: Output of Phase Detector and Control Input of Oscillator. Normally a series RC lowpass filter network is connected from this pin to ground. Tie this pin to SGND in applications which do not use the phase-locked loop. Can be driven by 0V to 2.4V logic signal for a frequency shifting option.

AUXFB: Feedback Input to the Auxiliary Regulator/Comparator. When used as a linear regulator, this input can either be connected to an external resistive divider or directly to the collector of the external PNP pass device for 12V operation. When used as a comparator, this is the noninverting input of a comparator whose inverting input is tied to the internal 1.19V reference. See Auxiliary Regulator/Comparator in Applications Information section.

AUXON: Pulling this pin high turns on the auxiliary regulator/comparator. The threshold is 1.19V.

AUXDR: Open Drain Output of the Auxiliary Regulator/Comparator. The base of an external PNP device is connected to this pin for use as a linear regulator. An external pull-up resistor is required for use as a comparator. A voltage > 9.5V on AUXDR causes the internal 12V resistive divider to be connected to AUXFB.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC1436/LTC1437 use a constant frequency, current mode step-down architecture. During normal operation, the top MOSFET is turned on each cycle when the oscillator sets the RS latch and turned off when the main current comparator I1 resets the RS latch. The peak inductor current at which I1 resets the RS latch is controlled by the voltage on I_{TH} pin, which is the output of error amplifier EA. V_{PRGM} and V_{OSENSE} pins, described in the Pin Functions, allow EA to receive an output feedback voltage V_{FB} from either internal or external resistive dividers. When the load current increases, it causes a slight decrease in V_{FB} relative to the 1.19V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by current comparator I2, or the beginning of the next cycle.

The top MOSFET drivers are biased from floating bootstrap capacitor C_B, which normally is recharged during each off cycle. However, when V_{IN} decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector counts the number of oscillator cycles that the top MOSFET remains on, and periodically forces a brief off period to allow C_B to recharge.

The main control loop is shut down by pulling RUN/SS pin low. Releasing RUN/SS allows an internal 3μA current source to charge soft start capacitor C_{SS}. When C_{SS} reaches 1.3V, the main control loop is enabled with the I_{TH} voltage clamped at approximately 30% of its maximum value. As C_{SS} continues to charge, I_{TH} is gradually released allowing normal operation to resume.

Comparator OV guards against transient overshoots >7.5% by turning off the top MOSFET and keeping it off until the fault is removed.

Low Current Operation

Adaptive Power mode allows the LTC1436/LTC1437 to automatically change between two output stages sized for different load currents. TGL and BG pins drive large synchronous N-channel MOSFETs for operation at high currents, while the TGS pin drives a much smaller N-channel MOSFET used in conjunction with a Schottky diode for operation at low currents. This allows the loop to continue to operate at normal frequency as the load current decreases without incurring the large MOSFET gate charge losses. If the TGS pin is left open, the loop defaults to Burst Mode operation in which the large MOSFETs operate intermittently based on load demand.

Adaptive Power mode provides constant frequency operation down to approximately 1% of rated load current. This results in an order of magnitude reduction of load current before Burst Mode operation commences. Without the small MOSFET (i.e.: no Adaptive Power mode), the transition to Burst Mode operation is approximately 10% of rated load current.

The transition to low current operation begins when comparator I2 detects current reversal and turns off the bottom MOSFET. If the voltage across R_{SENSE} does not exceed the hysteresis of I2 (approximately 20mV) for one full cycle, then on following cycles the top drive is routed to the small MOSFET at TGS pin and BG pin is disabled. This continues until an inductor current peak exceeds 20mV/R_{SENSE} or the I_{TH} voltage exceeds 0.6V, either of which causes drive to be returned to TGL pin on the next cycle.

Two conditions can force continuous synchronous operation, even when the load current would otherwise dictate low current operation. One is when the common mode voltage of the $SENSE^+$ and $SENSE^-$ pins is below 1.4V and the other is when the SFB pin is below 1.19V. The latter condition is used to assist in secondary winding regulation as described in the Applications Information section.

Frequency Synchronization

A Phase-locked loop (PLL) is available on the LTC1436-PLL and LTC1437 to allow the oscillator to be synchronized to an external source connected to the PLLIN pin. The output of the phase detector at the PLL LPF pin is also the control input of the oscillator, which operates over a 0V to 2.4V range corresponding to –30% to 30% in frequency. When locked, the PLL aligns the turn-on of the top MOSFET to the rising edge of the synchronizing signal. When PLLIN is left open or at a constant DC voltage, PLL LPF goes low, forcing the oscillator to minimum frequency.

OPERATION (Refer to Functional Diagram)

Power-On Reset

The POR pin is an open drain output which pulls low when the main regulator output voltage is out of regulation. When the output voltage rises to within 7.5% of regulation, a timer is started which releases POR after 2^{16} (65536) oscillator cycles. In shutdown, the POR output is pulled low.

Auxiliary Linear Regulator

The auxiliary linear regulator in the LTC1436/LTC1437 controls an external PNP transistor for operation up to 500mA. An internal AUXFB resistive divider set for 12V operation is invoked when AUXDR pin is above 9.5V to allow 12V VPP supplies to be easily implemented. When AUXDR is below 8.5V an external feedback divider may be used to set other output voltages. Taking the AUXON pin low shuts down the auxiliary regulator providing a convenient logic controlled power supply.

The AUX block can be used as a comparator having its inverting input tied to the internal 1.19V reference. The AUXDR pin is used as the output and requires an external pull-up to a supply less than 8.5V in order to inhibit the invoking of the internal resistive divider.

$INTV_{CC}/DRV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most of the other LTC1436/LTC1437 circuitry is derived from the $INTV_{CC}$ pin. The bottom MOSFET driver supply DRV_{CC} pin is internally connected to $INTV_{CC}$ in the LTC1436 and externally connected to $INTV_{CC}$ in the LTC1437. When the $EXTV_{CC}$ pin is left open, an internal 5V low dropout regulator supplies $INTV_{CC}$ power. If $EXTV_{CC}$ is taken above 4.8V, the 5V regulator is turned off and an internal switch is turned on to connect $EXTV_{CC}$ to $INTV_{CC}$. This allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as the output of the regulator itself or a secondary winding, as described in the Applications Information section.

4

APPLICATIONS INFORMATION

The basic LTC1436 application circuit is shown in Figure 1, High Efficiency Step-Down Converter. External component selection is driven by the load requirement, and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_{OSC} and L can be chosen. Next, the power MOSFETs and D1 are selected. Finally, C_{IN} and C_{OUT} are selected. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 28V (limited by the external MOSFETs).

R_{SENSE} Selection For Output Current

R_{SENSE} is chosen based on the required output current. The LTC1436/LTC1437 current comparator has a maximum threshold of $150mV/R_{SENSE}$ and an input common mode range of SGND to $INTV_{CC}$. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current ΔI_L.

Allowing a margin for variations in the LTC1436/LTC1437 and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

The LTC1436/LTC1437 work well with values of R_{SENSE} from 0.005Ω to 0.2Ω.

C_{OSC} Selection for Operating Frequency

The LTC1436/LTC1437 use a constant frequency architecture with the frequency determined by an external oscillator capacitor C_{OSC}. Each time the topside MOSFET turns on, the voltage on C_{OSC} is reset to ground. During the on-time, C_{OSC} is charged by a fixed current plus an additional current which is proportional to the output voltage of the phase detector V_{PLLLPF} (LTC1436-PLL/LTC1437). When the voltage on the capacitor reaches 1.19V, C_{OSC} is reset to ground. The process then repeats.

The value of C_{OSC} is calculated from the desired operating frequency. Assuming the phase-locked loop has no external oscillator input (V_{PLLLPF} = 0V):

APPLICATIONS INFORMATION

$$C_{OSC}\,(pF) = \left[\frac{1.37(10^4)}{\text{Frequency}\,(kHz)}\right] - 11$$

A graph for selecting C_{OSC} vs frequency is given in Figure 2. As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The maximum recommended switching frequency is 400kHz. When using Figure 2 for synchronizable applications, choose C_{OSC} corresponding to a frequency approximately 30% below your center frequency. (See Phase-Locked Loop and Frequency Synchronization.)

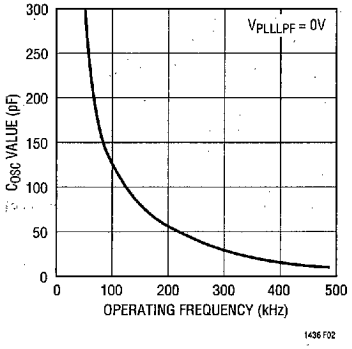


Figure 2. Timing Capacitor Value

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4\ (I_{MAX})$. Remember, the maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has an effect on low current operation. The transition to low current operation begins when the inductor current reaches zero while the bottom MOSFET is on. Lower inductor values (higher ΔI_L) will cause this to occur at higher load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation (TGS pin open), lower inductance values will cause the burst frequency to decrease.

The Figure 3 graph gives a range of recommended inductor values vs operating frequency and V_{OUT}.

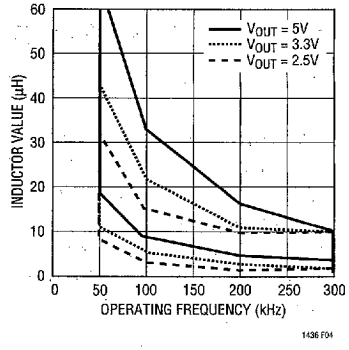


Figure 3. Recommended Inductor Values

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy, or Kool Mµ® cores. Actual core loss is

Kool Mµ is a registered trademark of Magnetics, Inc.

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independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are prefered at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. **Do not allow the core to saturate!**

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, designs for surface mount are available which do not increase the height significantly.

Power MOSFET and D1 Selection

Three external power MOSFETs must be selected for use with the LTC1436/LTC1437: a pair of N-channel MOSFETs for the top (main) switch and an N-channel MOSFET for the bottom (synchronous) switch.

To take advantage of the Adaptive Power output stage, two topside MOSFETs must be selected. A large (low $R_{SD(ON)}$) MOSFET and a small (higher $R_{DS(ON)}$) MOSFET are required. The large MOSFET is used as the main switch and works in conjunction with the synchronous switch. The smaller MOSFET is only enabled under low load current conditions. This increases midcurrent efficiencies while continuing to operate at constant frequency. Also, by using the small MOSFET the circuit can maintain constant frequency operation down to lower currents before cycle skipping occurs.

The $R_{DS(ON)}$ recommended for the small MOSFET is around 0.5Ω. Be careful not to use a MOSFET with an $R_{DS(ON)}$ that is too low; remember, we want to conserve gate charge. (A higher $R_{DS(ON)}$ MOSFET has a smaller gate capacitance and thus requires less current to charge its gate). For cost sensitive applications the small MOSFET can be removed. The circuit will then begin Burst Mode operation as the load current is dropped.

The peak-to-peak gate drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5V during start-up (see $EXTV_{CC}$ Pin Connection). Consequently, logic level threshold MOSFETs must be used in most LTC1436/LTC1437 applications. The only exception is applications in which $EXTV_{CC}$ is powered from an external supply greater than 8V (must be less than 10V), in which standard threshold MOSFETs [$V_{GS(TH)} < 4V$] may be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{SD(ON)}$, reverse transfer capacitance C_{RSS}, input voltage and maximum output current. When the LTC1436/LTC1437 are operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{(V_{IN} - V_{OUT})}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + k(V_{IN})^{1.85}(I_{MAX})(C_{RSS})(f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and k is a constant inversely related to the gate drive current.

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Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actual provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage or during a short circuit when the duty cycle in this switch is nearly 100%. Refer to the Foldback Current Limiting section for further applications information.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET characteristics. The constant $k = 2.5$ can be used to estimate the contributions of the two terms in the main switch dissipation equation.

The Schottky diode D1 shown in Figure 1 serves two purposes. During continuous synchronous operation, D1 conducts during the dead-time between the conduction of the two large power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency. During low current operation, D1 operates in conjunction with the small top MOSFET to provide an efficient low current output stage. A 1A Schottky is generally a good compromise for both regions of operation due to the relatively small average current.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx I_{MAX}\frac{\left[V_{OUT}\left(V_{IN}-V_{OUT}\right)\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement is satisified, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L\left(ESR + \frac{1}{4fC_{OUT}}\right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. With $\Delta I_L = 0.4I_{OUT(MAX)}$ the output ripple will be less than 100mV at maximum V_{IN}, assuming:

C_{OUT} Required ESR $< 2R_{SENSE}$

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR (size) product of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Other capacitor types

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include Sanyo OS-CON, Nichicon PL series and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces the 5V supply which powers the drivers and internal circuitry within the LTC1436/LTC1437. The $INTV_{CC}$ pin can supply up to 15mA and must be bypassed to ground with a minimum of 2.2µF tantalum or low ESR electrolytic. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate drivers.

High input voltage applications, in which large MOSFETs are being driven at high frequencies, may cause the maximum junction temperature rating for the LTC1436/LTC1437 to be exceeded. The IC supply current is dominated by the gate charge supply current when not using an output derived $EXTV_{CC}$ source. The gate charge is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 1 of the Electrical Characteristics. For example, the LTC1437 is limited to less than 19mA from a 30V supply:

$$T_J = 70°C + (19mA)(30V)(95°C/W) = 124°C$$

To prevent maximum junction temperature from being exceeded, the input supply current must be checked when operating in continuous mode at maximum V_{IN}.

$EXTV_{CC}$ Connection

The LTC1436/LTC1437 contain an internal P-channel MOSFET switch connected between the $EXTV_{CC}$ and $INTV_{CC}$ pins. The switch closes and supplies the $INTV_{CC}$ power whenever the $EXTV_{CC}$ pin is above 4.8V, and remains closed until $EXTV_{CC}$ drops below 4.5V. This allows the MOSFET driver and control power to be derived from the output during normal operation (4.8V < V_{OUT} < 9V) and from the internal regulator when the output is out of regulation (start-up, short circuit). Do not apply greater than 10V to the $EXTV_{CC}$ pin and ensure that $EXTV_{CC} \leq V_{IN}$.

Significant efficiency gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of Duty Cycle/Efficiency. For 5V regulators this supply means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. However, for 3.3V and other lower voltage regulators, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the internal 5V regulator resulting in an efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ connected directly to V_{OUT}. This is the normal connection for a 5V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage which has been boosted to greater than 4.8V. This can be done with either the inductive boost winding as shown in Figure 4a or the capacitive charge pump shown in Figure 4b. The charge pump has the advantage of simple magnetics.
4. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 5V to 10V range ($EXTV_{CC} \leq V_{IN}$), it may be used to power $EXTV_{CC}$, providing it is compatible with the MOSFET gate drive requirements. When driving standard threshold MOSFETs, the external supply must always be present during operation to prevent MOSFET failure due to insufficient gate drive.

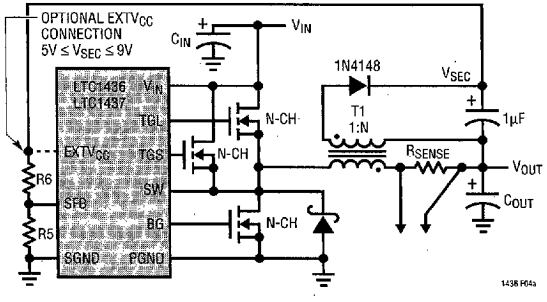

Figure 4a. Secondary Output Loop and $EXTV_{CC}$ Connection

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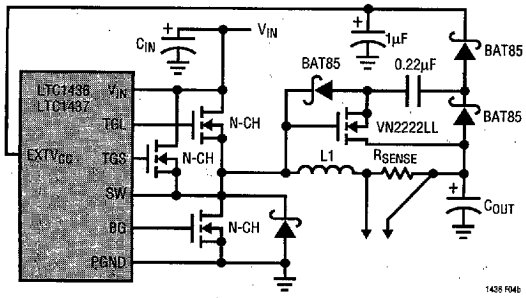

Figure 4b. Capacitive Charge Pump for EXT V_{CC}

Topside MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor C_B connected to the Boost pin supplies the gate drive voltage for the topside MOSFET(s). Capacitor C_B in the functional diagram is charged through diode D_B from INTV$_{CC}$ when the SW pin is low. When one of the topside MOSFET(s) is to be turned on, the driver places the C_B voltage across the gate source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage SW rises to V_{IN} and the Boost pin rises to V_{IN} + INTV$_{CC}$. The value of the boost capacitor C_B needs to be 100 times greater than the total input capacitance of the topside MOSFET(s). In most applications 0.1µF is adequate. The reverse breakdown on D_B must be greater than $V_{IN(MAX)}$.

Output Voltage Programming

The output voltage is pin selectable for all members of the LTC1436/LTC1437 family. The output voltage is selected by the V_{PROG} pin as follows:

V_{PROG} = 0V	V_{OUT} = 3.3V
V_{PROG} = INTV$_{CC}$	V_{OUT} = 5V
V_{PROG} = Open (DC)	V_{OUT} = Adjustable

The LTC1436/LTC1437 family also has remote output voltage sense capability. The top of an internal resistive divider is connected to V_{OSENSE}. For fixed 3.3V and 5V output voltage applications the V_{OSENSE} pin is connected to the output voltage as shown in Figure 5a. When using an external resistor divider, the V_{PROG} pin is left open (DC) and the V_{OSENSE} pin is connected to the feedback resistors as shown in Figure 5b.

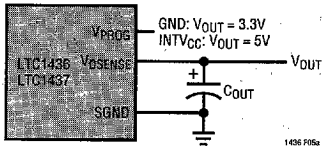

Figure 5a. LTC1436/LTC1437 Fixed Output Applications

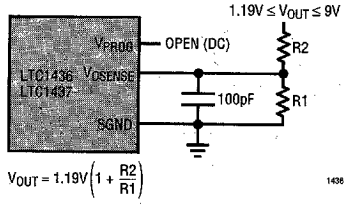

Figure 5b. LTC1436/LTC1437 Adjustable Applications

Power-On Reset Function (POR)

The power-on reset function monitors the output voltage and turns on an open drain device when it is out of regulation. An external pull-up resistor is required on the POR pin.

When power is first applied or when coming out of shutdown, the POR output is pulled to ground. When the output voltage rises above a level which is 5% below the final regulated output value, an internal counter starts. After counting 2^{16} (65536) clock cycles, the POR pull-down device turns off.

The POR output will go low whenever the output voltage drops below 7.5% of its regulated value for longer than approximately 30µs, signaling an out-of-regulation condition. In shutdown, the POR output is pulled low even if the regulator's output is held up by an external source.

Run/Soft Start Function

The RUN/SS pin is a dual purpose pin which provides the soft start function and a means to shut down the LTC1436/LTC1437. Soft start reduces surge currents from V_{IN} by gradually increasing the internal current limit. *Power supply sequencing* can also be accomplished using this pin.

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An internal 3μA current source charges up an external capacitor C_{SS}. When the voltage on RUN/SS reaches 1.3V the LTC1436/LTC1437 begin operating. As the voltage on RUN/SS continues to ramp from 1.3V to 2.4V, the internal current limit is also ramped at a proportional linear rate. The current limit begins at approximately $50mV/R_{SENSE}$ (at $V_{RUN/SS} = 1.3V$) and ends at $150mV/R_{SENSE}$ ($V_{RUN/SS} \geq 2.7V$). The output current thus ramps up slowly, charging the output capacitor. If RUN/SS has been pulled all the way to ground there is a delay before starting of approximately 500ms/μF, followed by an additional 500ms/μF to reach full current.

$$t_{DELAY} = 5(10^5)C_{SS} \text{ seconds}$$

Pulling the RUN/SS pin below 1.3V puts the LTC1436/LTC1437 into a low quiescent current shutdown ($I_Q < 25\mu A$). This pin can be driven directly from logic as shown in Figure 6. Diode D1 in Figure 6 reduces the start delay but allows C_{SS} to ramp up slowly for the soft start function; this diode and C_{SS} can be deleted if soft start is not needed. The RUN/SS pin has an internal 6V Zener clamp (see Functional Diagram).

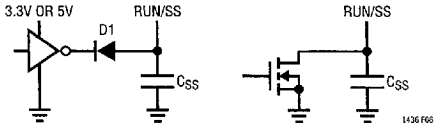


Figure 6. Run/SS Pin Interfacing

Foldback Current Limiting

As described in Power MOSFET and D1 Selection, the worst-case dissipation for either MOSFET occurs with a short-circuited output, when the synchronous MOSFET conducts the current limit value almost continuously. In most applications this will not cause excessive heating, even for extended fault intervals. However, when heat sinking is at a premium or higher $R_{DS(ON)}$ MOSFETs are being used, foldback current limiting should be added to reduce the current in proportion to the severity of the fault.

Foldback current limiting is implemented by adding a diode D_{FB} between the output and I_{TH} pins as shown in the Function Diagram. In a hard short ($V_{OUT} = 0V$), the current will be reduced to approximately 25% of the maximum output current. This technique may be used for all applications with regulated output voltages of 1.8V or greater.

Phase-Locked Loop and Frequency Synchronization

The LTC1436-PLL/LTC1437 each have an internal voltage-controlled oscillator and phase detector comprising a phase-locked loop. This allows the top MOSFET turn-on to be locked to the rising edge of an external source. The frequency range of the voltage-controlled oscillator is ±30% around the center frequency f_O.

The value of C_{OSC} is calculated from the desired operating frequency f_O. Assuming the phase-locked loop is *locked* ($V_{PLLLPF} = 1.19V$):

$$C_{OSC}(pF) = \left[\frac{2.1(10^4)}{\text{Frequency}(kHz)}\right] - 11$$

Stating the frequency as a function of V_{PLLLPF} and C_{OSC}:

$$\text{Frequency}(kHz) = \frac{8.4(10^8)}{\left[C_{OSC}(pF)+11\right]\left[\frac{1}{17\mu A + 18\mu A\left(\frac{V_{PLLLPF}}{2.4V}\right)} + 2000\right]}$$

The phase detector used is an edge sensitive digital type which provides zero degrees phase shift between the external and internal oscillators. This type of phase detector will not lock up on input frequencies close to the harmonics of the VCO center frequency. The PLL hold-in range Δf_H is equal to the capture range: $\Delta f_H = \Delta f_C = \pm 0.3 f_O$.

APPLICATIONS INFORMATION

The output of the phase detector is a complementary pair of current sources charging or discharging the external filter network on the PLL LPF pin. The relationship between the PLL LPF pin and operating frequency is shown in Figure 7. A simplified block diagram is shown in Figure 8.

If the external frequency (f_{PLLIN}) is greater than the oscillator frequency (f), current is sourced continuously, pulling up the PLL LPF pin. When the external frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLL LPF pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. Thus the voltage on the PLL LPF pin is adjusted until the phase and frequency of the external and internal oscillators are identical. At this stable operating point the phase comparator output is open and the filter capacitor C_{LP} holds the voltage.

The loop filter components C_{LP} and R_{LP} smooth out the current pulses from the phase detector and provide a stable input to the voltage-controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically, R_{LP} = 10k and C_{LP} is 0.01µF to 0.1µF. Be sure to connect the low side of the filter to SGND.

The PLL LPF pin can be driven with external logic to obtain a 1:1.9 frequency shift. The circuit shown in Figure 9 will provide a frequency shift from f_0 to $1.9f_0$ as the voltage and V_{PLLLPF} increases from 0V to 2.4V. Do not exceed 2.4V on V_{PLLLPF}.

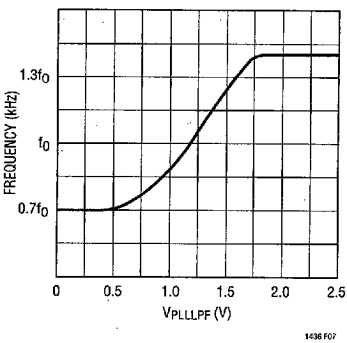


Figure 7. Operating Frequency vs V_{PLLLPF}

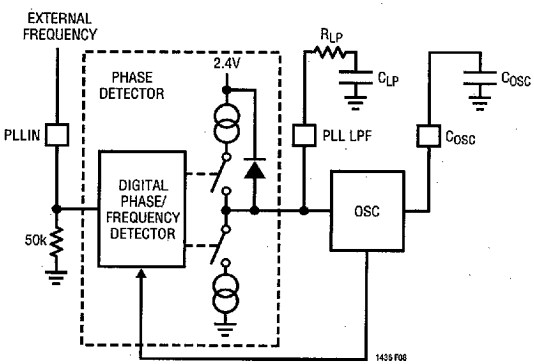


Figure 8. Phase-Locked Loop Block Diagram

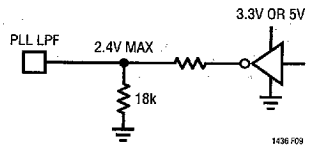


Figure 9. Directly Driving PLL LPF Pin

Low Battery Comparator

The LTC1436/LTC1437 have an on-chip low battery comparator which can be used to sense a low battery condition when implemented as shown in Figure 10. The resistor divider R3, R4 sets the comparator trip point as follows:

$$V_{LBTRIP} = 1.19V\left(1+\frac{R4}{R3}\right)$$

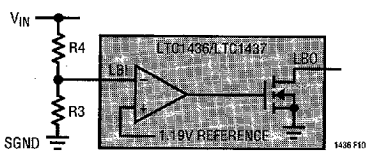


Figure 10. Low Battery Comparator

APPLICATIONS INFORMATION

The divided down voltage at the negative (–) input to the comparator is compared to an internal 1.19V reference. A 20mV hysteresis is built in to assure rapid switching. The output is an open drain MOSFET and requires a pull-up resistor. This comparator is *not* active in shutdown. The low side of the resistive divider should connect to SGND.

SFB Pin Operation

When the SFB pin drops below its ground-referenced 1.19V threshold, continuous mode operation is forced. In continuous mode, the large N-channel main and synchronous switches are used regardless of the load on the main output.

In addition to providing a logic input to force continuous synchronous operation, the SFB pin provides a means to regulate a flyback winding output. Continuous synchronous operation allows power to be drawn from the auxiliary windings without regard to the primary output load. The SFB pin provides a way to force continuous synchronous operation as needed by the flyback winding.

The secondary output voltage is set by the turns ratio of the transformer in conjunction with a pair of external resistors returned to the SFB pin as shown in Figure 4a. The secondary regulated voltage V_{SEC} in Figure 4a is given by:

$$V_{SEC} \approx (N+1)V_{OUT} > 1.19V\left(1+\frac{R6}{R5}\right)$$

where N is the turns ratio of the transformer and V_{OUT} is the main output voltage sensed by V_{OSENSE}.

Auxiliary Regulator/Comparator

The auxiliary regulator/comparator can be used as a comparator or low dropout regulator (by adding an external PNP pass device).

When the voltage present at the AUXON pin is greater than 1.19V the regulator/comparator is on. Special circuitry consumes a small (20μA) bias current while still remaining stable when operating as a low dropout regulator. No excess current is drawn when the input stage is overdriven when used as a comparator.

The AUXDR pin is internally connected to an open drain MOSFET which can sink up to 10mA. The voltage on AUXDR determines whether or not an internal 12V resistive divider is connected to AUXFB as described below. A pull-up resistor is required on AUXDR and the voltage must not exceed 28V.

With the addition of an external PNP pass device, a linear regulator capable of supplying up to 0.5A is created. As shown in Figure 12a, the base of the external PNP connects to the AUXDR pin together with a pull-up resistor. The output voltage V_{OAUX} at the collector of the external PNP is sensed by the AUXFB pin.

The input voltage to the auxiliary regulator can be taken from a secondary winding on the primary inductor as shown in Figure 11a. In this application, the SFB pin regulates the input voltage to the PNP regulator (see SFB Pin Operation) and should be set to approximately 1V to 2V above the required output voltage of the auxiliary regulator. A Zener diode clamp may be required to keep V_{SEC} under the 28V AUXDR pin specification when the primary is heavily loaded and the secondary is not.

The AUXFB pin is the feedback point of the regulator. An internal resistive divider is available to provide a 12V output by simply connecting AUXFB directly to the collector of the external PNP. The internal resistive divider is selected when the voltage at AUXFB goes above 9.5V with 1V built-in hysteresis. For other output voltages, an external resistive divider is fed back to AUXFB as shown in Figure 11b. The output voltage V_{OAUX} is set as follows:

$V_{OAUX} = 1.19V(1+R8/R7) < 8V$ AUXDR < 8.5V
$V_{OAUX} = 12V$ AUXDR ≥ 12V

The circuit can also be used as a noninverting voltage comparator as shown in Figure 11c. When AUXFB drops below 1.19V, the AUXDR pin will be pulled low. A minimum current of 5μA is required to pull the AUXDR pin to 5V when used as a comparator output, in order to counteract a 1.5μA internal current source.

APPLICATIONS INFORMATION

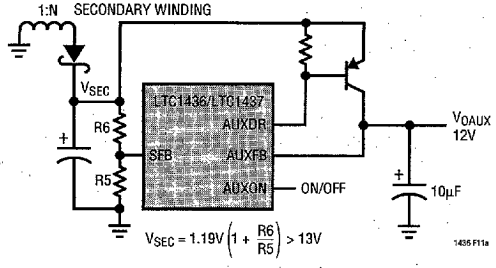


Figure 11a. 12V Output Auxiliary Regulator Using Internal Feedback Resistors

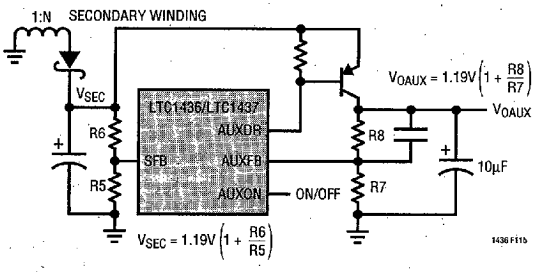


Figure 11b. 5V Output Auxiliary Regulator Using External Feedback Resistors

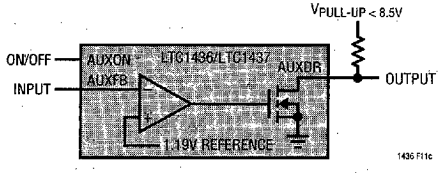


Figure 11c. Auxiliary Comparator Configuration

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1436/LTC1437 circuits: LTC1436/LTC1437 V_{IN} current, $INTV_{CC}$ current, I^2R losses and topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table which excludes MOSFET driver and control currents. V_{IN} current results in a small (<1%) loss which increases with V_{IN}.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ which is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs. It is for this reason that the Adaptive Power output stage switches to a low Q_T MOSFET during low current operation.

   By powering $EXTV_{CC}$ from an output-derived source, the additional V_{IN} current resulting from the driver and control currents will be scaled by a factor of Duty Cycle/Efficiency. For example, in a 20V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 3mA of V_{IN} current. This reduces the midcurrent loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are predicted from the DC resistances of the MOSFET, inductor and current shunt. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the topside main MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)} = 0.05\Omega$, $R_L = 0.15\Omega$ and $R_{SENSE} = 0.05\Omega$, then the total resistance is 0.25Ω. This results in losses ranging from 3% to 10% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to drop at high output currents.

APPLICATIONS INFORMATION

4. Transition losses apply only to the topside MOSFET(s), and only when operating at high input voltages (typically 20V or greater). Transition losses can be estimated from:

   Transition Loss = $2.5(V_{IN})^{1.85}(I_{MAX})(C_{RSS})(f)$

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, Schottky conduction losses during dead-time and inductor core losses, generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $(\Delta I_{LOAD})(ESR)$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} which generates a feedback error signal. The regulator loop then acts to return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The I_{TH} external components shown in the Figure 1 circuit will provide adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $25(C_{LOAD})$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Automotive Considerations: Plugging into the Cigarette Lighter

As battery-powered devices go mobile, there is a natural interest in plugging into the cigarette lighter in order to conserve or even recharge battery packs during operation. But before you connect, be advised: you are plugging into the supply from hell. The main battery line in an automobile is the source of a number of nasty potential transients, including load dump, reverse battery, and double battery.

Load dump is the result of a loose battery cable. When the cable breaks connection, the field collapse in the alternator can cause a positive spike as high as 60V which takes several hundred milliseconds to decay. Reverse battery is just what it says, while double battery is a consequence of tow-truck operators finding that a 24V jump start cranks cold engines faster than 12V.

The network shown in Figure 12 is the most straightforward approach to protect a DC/DC converter from the ravages of an automotive battery line. The series diode prevents current from flowing during reverse battery, while the transient suppressor clamps the input voltage during load dump. Note that the transient suppressor should not conduct during double battery operation, but must still clamp the input voltage below breakdown of the converter. Although the LT1436/LTC1437 have a maximum input voltage of 36V, most applications will be limited to 30V by the MOSFET BV_{DSS}.

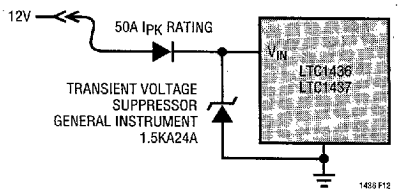


Figure 12. Automotive Application Protection

Design Example

As a design example, assume V_{IN} = 12V (nominal), V_{IN} = 22V (max), V_{OUT} = 3.3V, I_{MAX} = 3A and f = 250kHz, R_{SENSE} and C_{OSC} can immediately be calculated:

$$R_{SENSE} = \frac{100mV}{3A} = 0.033\Omega$$

$$C_{OSC} = \left(\frac{1.37(10^4)}{250}\right) - 11 = 43pF$$

APPLICATIONS INFORMATION

Refering to Figure 3, a 10µH inductor falls within the recommended range. To check the actual value of the ripple current the following equation is used:

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

The highest value of the ripple current occurs at the maximum input voltage:

$$\Delta I_L = \frac{3.3V}{250kHz(10\mu H)}\left(1-\frac{3.3V}{22V}\right) = 1.12A$$

The power dissipation on the topside MOSFET can be easily estimated. Choosing a Siliconix Si4412DY results in: $R_{DS(ON)}$ = 0.042Ω, C_{RSS} = 100pF. At maximum input voltage with T (estimated) = 50°C:

$$P_{MAIN} = \frac{3.3V}{22V}(3)^2\left[1+(0.005)(50°C-25°C)\right](0.042\Omega) + 2.5(22V)^{1.85}(3A)(100pF)(250kHz) = 122mW$$

The most stringent requirement for the synchronous N-channel MOSFET occurs when V_{OUT} = 0 (i.e. short circuit). In this case the worst-case dissipation rises to:

$$P_{SYNC} = \left[I_{SC(AVG)}\right]^2(1+\delta)R_{DS(ON)}$$

With the 0.033Ω sense resistor $I_{SC(AVG)}$ = 4A will result, increasing the Si4412DY dissipation to 950mW at a die temperature of 105°C.

C_{IN} is chosen for an RMS current rating of at least 1.5A at temperature. C_{OUT} is chosen with an ESR of 0.03Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = R_{ESR}(\Delta I_L) = 0.03\Omega(1.12A) = 34mV_{P-P}$$

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1436/LTC1437. These items are also illustrated graphically in the layout diagram of Figure 13. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1436/LTC1437 signal ground pin must return to the (–) plate of C_{OUT}. The power ground connects to the source of the bottom N-channel MOSFET, anode of the Schottky diode, and (–) plate of C_{IN}, which should have as short lead lengths as possible.
2. Does the LTC1436/LTC1437 V_{OSENSE} pin connect to the (+) plate of C_{OUT}? In adjustable applications, the resistive divider R1/R2 must be connected between the (+) plate of C_{OUT} and signal ground. The 100pF capacitor should be as close as possible to the LTC1436/LTC1437.
3. Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the LTC1436/LTC1437.
4. Does the (+) plate of C_{IN} connect to the drain of the topside MOSFET(s) as closely as possible? This capacitor provides the AC current to the MOSFET(s).
5. Is the $INTV_{CC}$ decoupling capacitor connected closely between $INTV_{CC}$ and the power ground pin? This capacitor carries the MOSFET driver peak currents.
6. Keep the switching node SW away from sensitive small-signal nodes. Ideally, the switch node should be placed at the furthest point from the LTC1436/LTC1437.
7. Route the PLLIN line away from Boost and SW pins to avoid unwanted pickup (Boost and SW pins have high dV/dTs).
8. SGND should be used exclusively for grounding external components on PLL LPF, C_{OSC}, I_{TH}, LBI, SFB, V_{OSENSE} and AUXFB pins.

APPLICATIONS INFORMATION

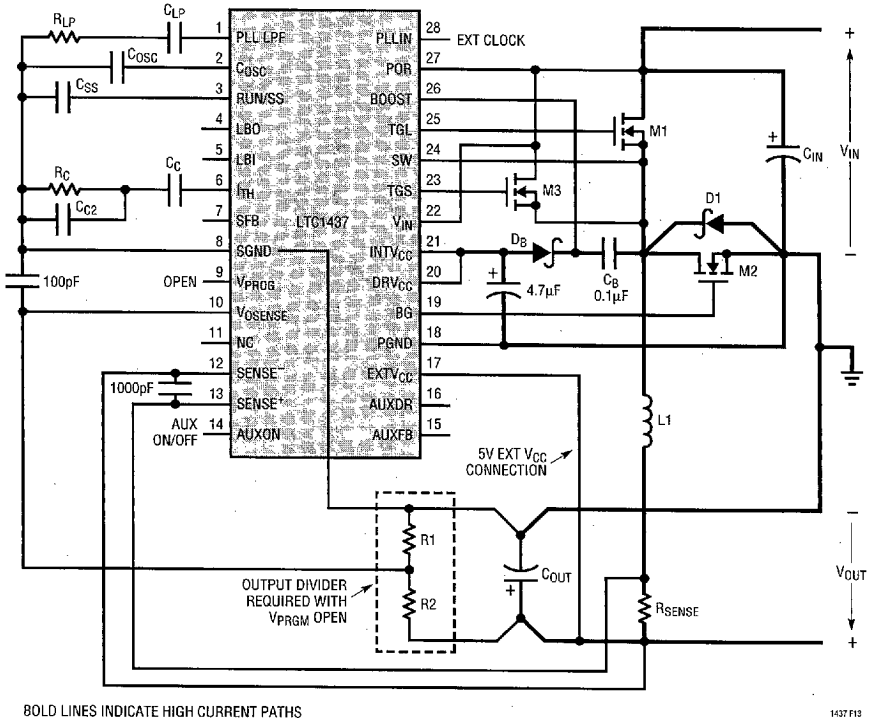
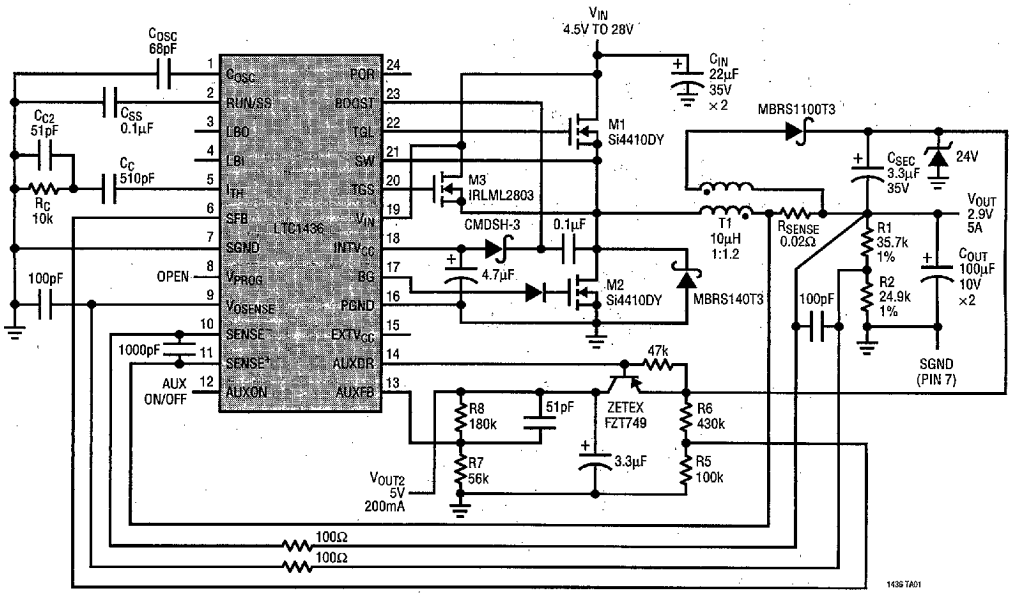


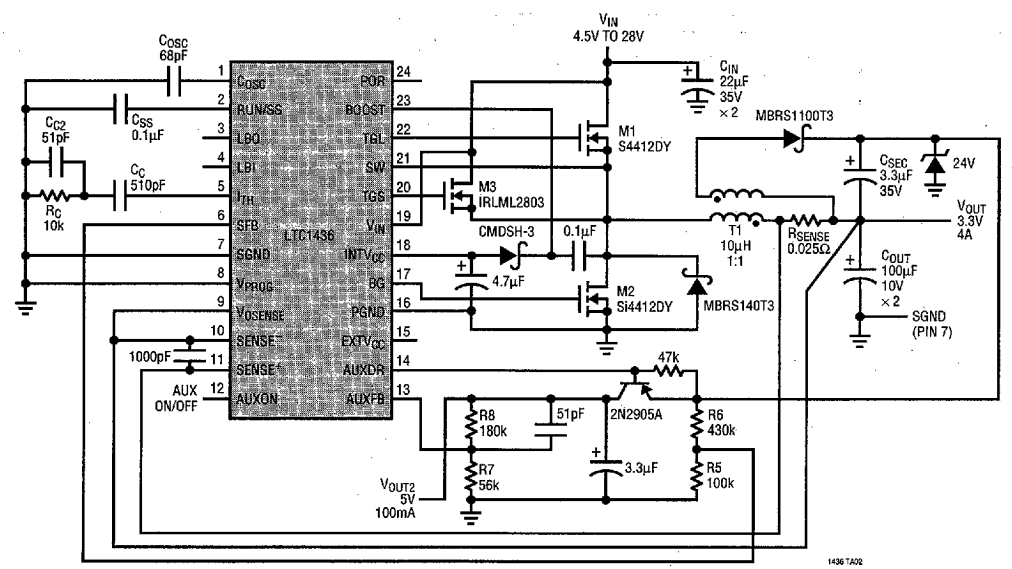
Figure 13. LTC1437 Layout Diagram

TYPICAL APPLICATIONS

LTC1436 2.9V/5A Adjustable with 5V Auxiliary Output

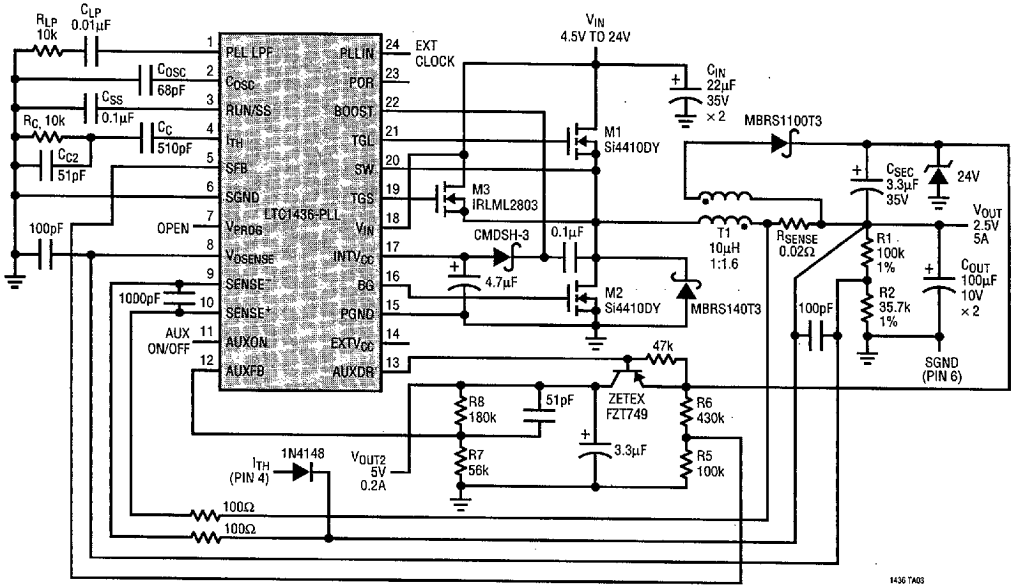


LTC1436 3.3V/4A Fixed Output with 5V Auxiliary Output

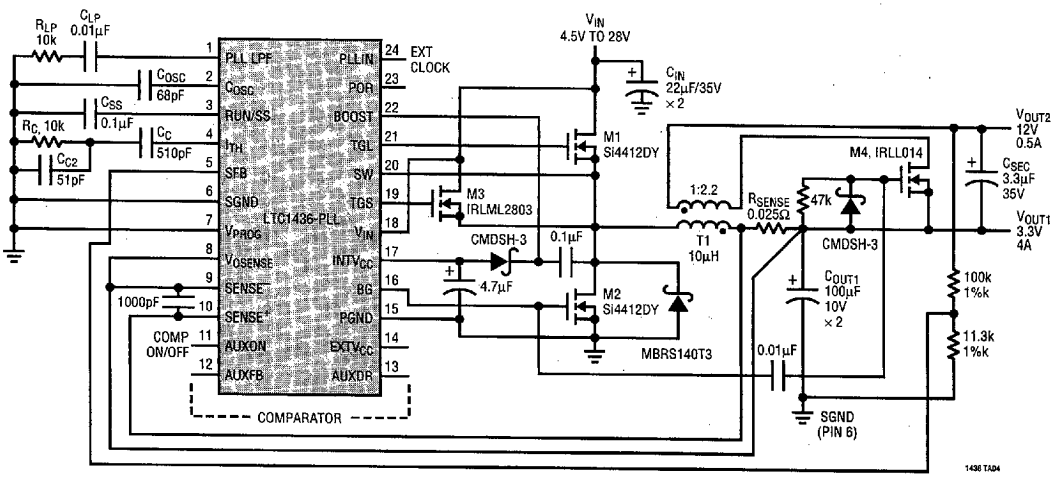


TYPICAL APPLICATIONS

LTC1436-PLL 2.5V/5A Adjustable Output with Foldback Current Limiting and 5V Auxiliary Output



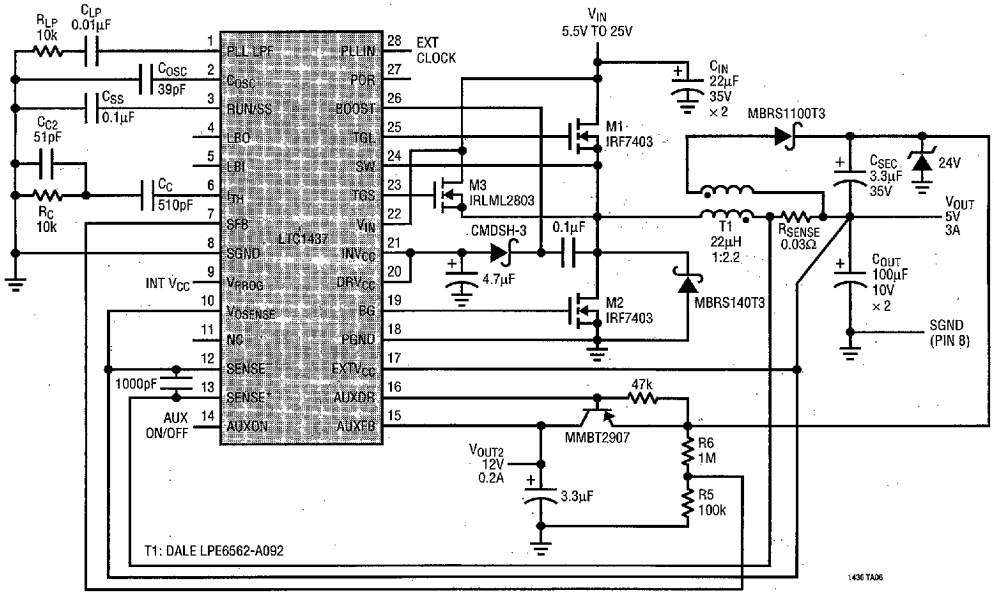
LTC1436-PLL 5V/3A Fixed Output with 12V/200mA Auxiliary Output and Uncommitted Comparator



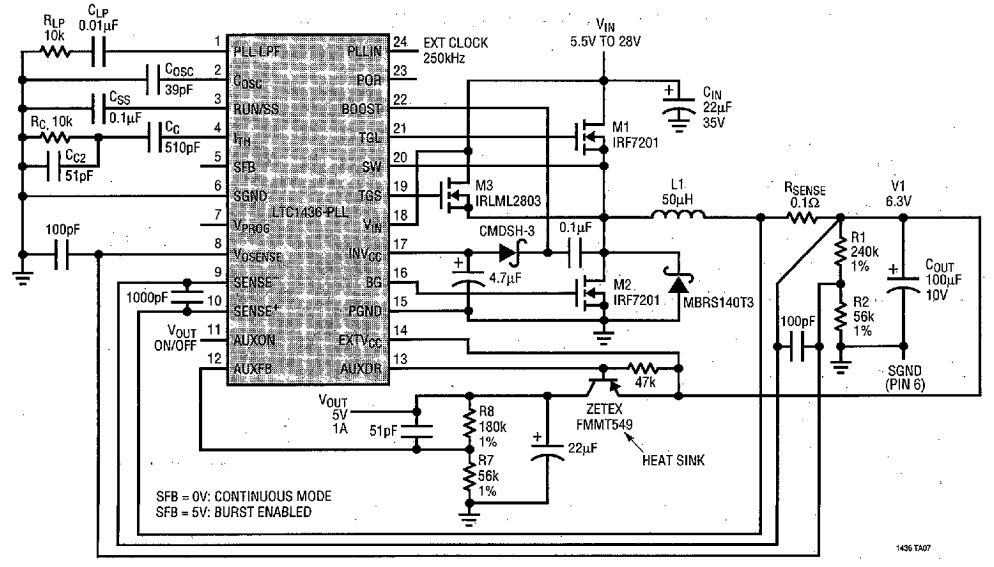
T1: DALE LPE6562-A092

TYPICAL APPLICATIONS

LTC1437 5V/3A Fixed Output with 12V Auxiliary Output

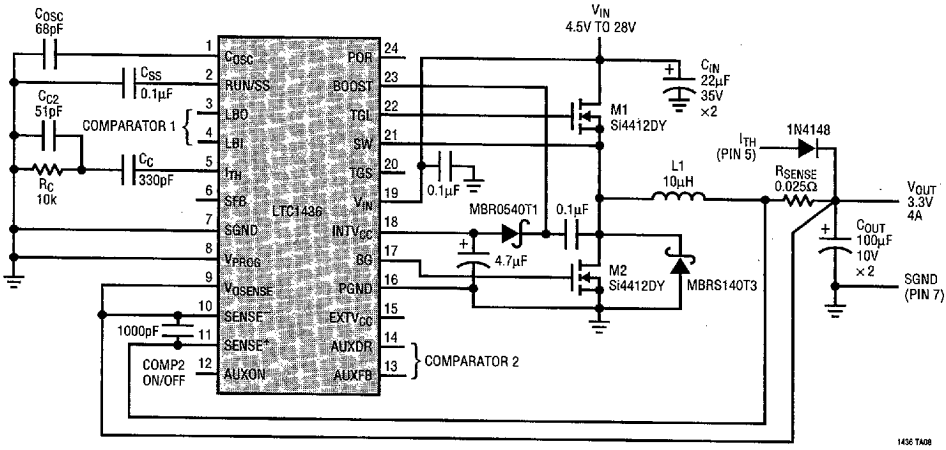


LTC1436-PLL Low Noise High Efficiency 5V/1A Regulator



TYPICAL APPLICATIONS

LTC1436 3.3V/4A Burst Mode Regulator with Foldback Current Limiting and Two Uncommited Comparators

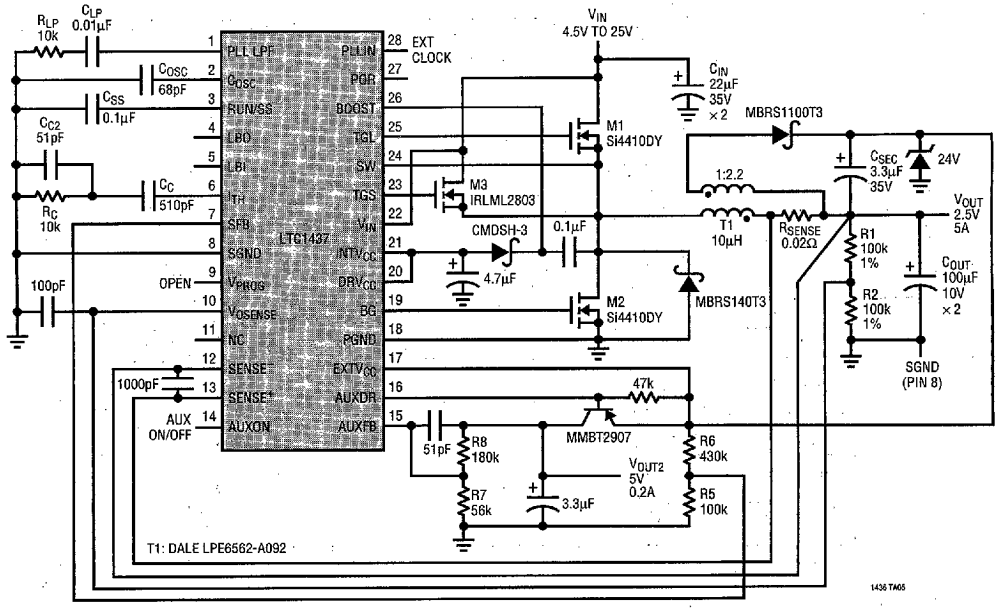


SFB = 0V: CONTINUOUS MODE
SFB = 5V: BURST ENABLED
L1: SUMIDA CDRH125-10

4

TYPICAL APPLICATION

LTC1437 2.5V/5A Adjustable Output with 5V Auxiliary Output



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1142HV/LTC1142	Dual High Efficiency Synchronous Step-Down Switching Regulators	Dual Synchronous, $V_{IN} \leq 20V$
LTC1148HV/LTC1148	High Efficiency Step-Down Switching Regulator Controllers	Synchronous, $V_{IN} \leq 20V$
LTC1159	High Efficiency Synchronous Step-Down Switching Regulator	Synchronous, $V_{IN} \leq 40V$, For Logic Threshold FETs
LT®1375/LT1376	1.5A, 500kHz Step-Down Switching Regulators	High Frequency, Small Inductor, High Efficiency Switchers, 1.5A Switch
LTC1430	High Power Step-Down Switching Regulator Controller	High Efficiency 5V to 3.3V Conversion at Up to 15A
LTC1435	High Efficency, Low Noise Synchronous Step-Down Switching Regulator	16-Pin Narrow SO and SSOP
LTC1438/LTC1439	Dual High Efficiency, Low Noise, Synchronous Step-Down Switching Regulators	Full-Featured Dual Controllers
LT1510	Constant-Voltage/ Constant-Current Battery Charger	1.3A, Li-Ion, NiCd, NiMH, Pb-Acid Charger
LTC1538-AUX	Dual High Efficiency, Low Noise, Synchronous Step-Down Switching Regulator	5V Standby in Shutdown
LTC1539	Dual High Efficiency, Low Noise, Synchronous Step-Down Switching Regulator	5V Standby in Shutdown