聯陽半導體
ITE Tech. Inc.

IT8203R

Jumper Free Over Clock Controller

Preliminary Specification 0.1

INTEGRATED TECHNOLOGY EXPRESS, INC.

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1. Features

- Five VID input (VIDIN0~4) and five VID output (VIDOUT0~VIDOUT4) pins
- Provides 10 GPIO pins
- Supports Auto-Recovery; build-in watch-dog timer and reset output signal pin
- Provides CPU changing detect pin (SLOTOCC#)
- Serial bus interface
- 28-pin SSOP

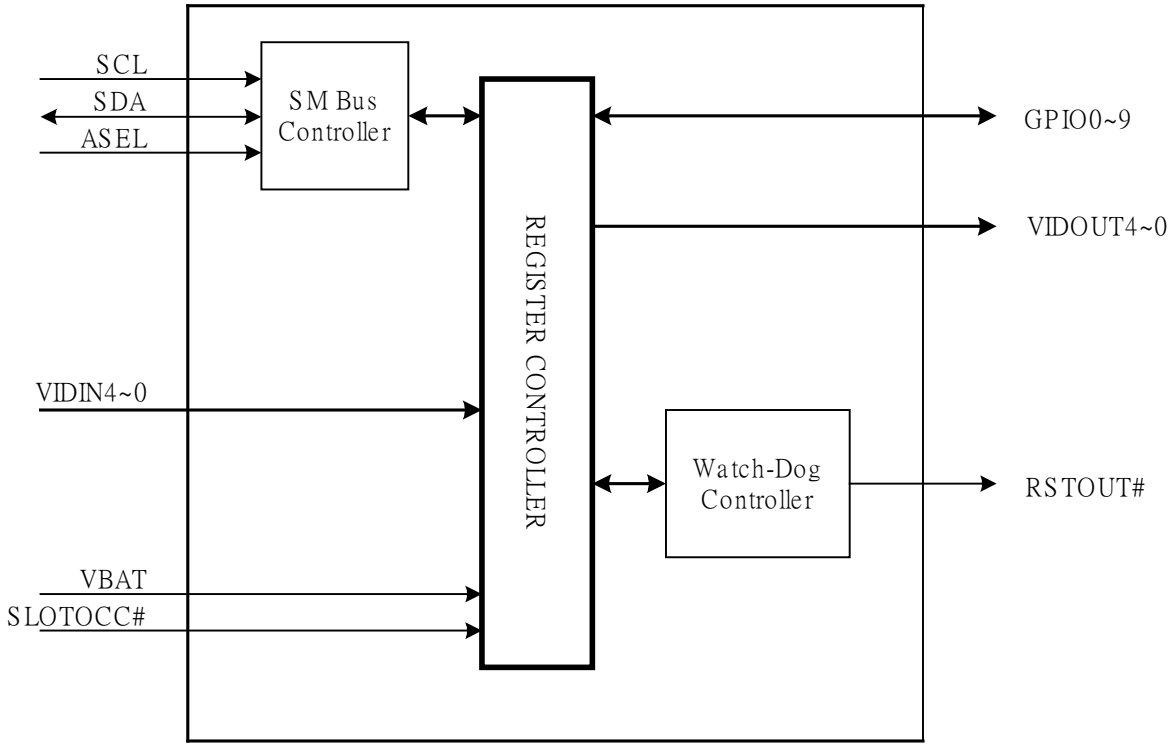
2. General Description

For acquiring better performance with lower cost, "Over-Clocking" gradually becomes a popular feature in the DIY market of PC motherboard. To do so, many interfaces on motherboard such as PWM, CPU, chipset, clock generator, AGP, DIMM, etc should be well handled.

Moreover, there is a trend to do "Jumperless" Over-Clocking in the motherboard design. For matching the trend, ITE develops a series of Jumper Free Over Clock Controllers targeted on different environments.

Generally, these controllers cover the following features:
- VID Interface and/or FID Interface handling
- GPIO
- Watch Dog Timers with Reset Signals for system auto-recovery from different situations
- CPU changing detection

3. Block Diagram



4. Pin Configuration

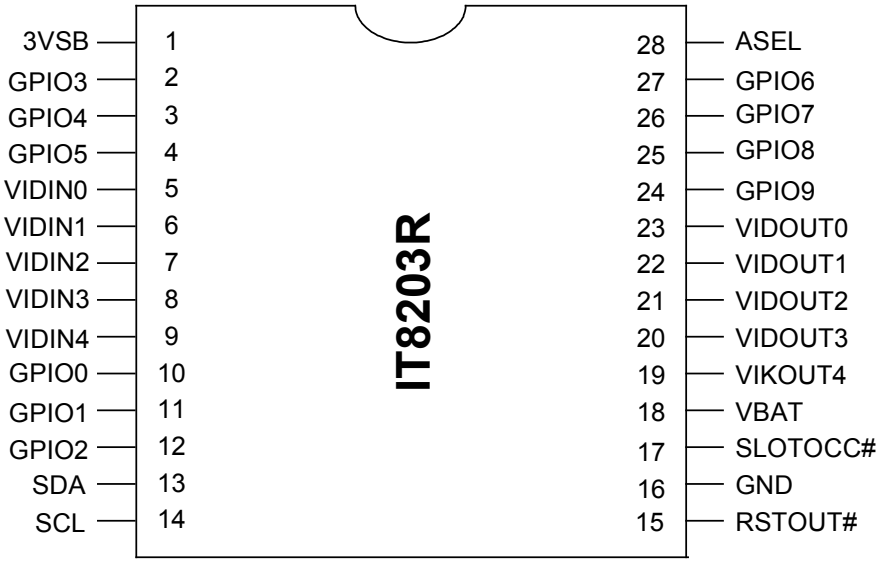


Table 4-1. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	3VSB	8	VIDIN3	15	RSTOUT#	22	VIDOUT1
2	GPIO3	9	VIDIN4	16	GND	23	VIDOUT0
3	GPIO4	10	GPIO0	17	SLOTOCC#	24	GPIO9
4	GPIO5	11	GPIO1	18	VBAT	25	GPIO8
5	VIDIN0	12	GPIO2	19	VIDOUT4	26	GPIO7
6	VIDIN1	13	SDA	20	VIDOUT3	27	GPIO6
7	VIDIN2	14	SCL	21	VIDOUT2	28	ASEL

Table 4-2. Pins Listed in Alphabetical Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	3VSB	3	GPIO4	14	SCL	8	VIDIN3
28	ASEL	4	GPIO5	13	SDA	9	VIDIN4
16	GND	27	GPIO6	17	SLOTOCC#	23	VIDOUT0
10	GPIO0	26	GPIO7	18	VBAT	22	VIDOUT1
11	GPIO1	25	GPIO8	5	VIDIN0	21	VIDOUT2
12	GPIO2	24	GPIO9	6	VIDIN1	20	VIDOUT3
2	GPIO3	15	RSTOUT#	7	VIDIN2	19	VIDOUT4

5. IT8203 Pin Descriptions

Table 5-1. Pin Descriptions of VID Interface

Pin(s) No.	Symbol	Attribute	Description
5-9	VIDIN0~ VIDIN4	I	*Voltage Identification Input Signals from CPU*
19-23	VIDOUT4~ VIDOUT0	OD12	*Voltage Identification Output Signals to PWM*

Table 5-2. Pin Descriptions of General Purpose I/O

Pin(s) No.	Symbol	Attribute	Description
10-12, 2-4, 27,26,25,24	GPIO0~ GPIO9	IO12	*General Purpose I/O pins*

Table 5-3. Pin Descriptions of SM Bus Interface

Pin(s) No.	Symbol	Attribute	Description
13	SDA	IOD12	*SMB Data Signal*
14	SCL	IK	*SMB Clock Signal*
28	ASEL	OD12	*Address Selector* 0: 7'h37 1: 7'h4E

Table 5-4. Pin Description of Watch-Dog Reset

Pin(s) No.	Symbol	Attribute	Description
24	RSTOUT#	OD12	*Watch-Dog Timeout Reset Output Signal*

Table 5-5. Pin Description of CPU Changing Detection

Pin(s) No.	Symbol	Attribute	Description
17	SLOTOCC#	IK	*CPU Changing Detect Pin* 0: CPU present 1: CPU absent

Table 5-6. Pin Description of Power/Ground

Pin(s) No.	Symbol	Attribute	Description
1	3VSB	I	*Power Supply of 3.3V*
16	GND	I	*Ground*
27	VBAT	I	*Battery Power Supply of 3.3V*

Notes: IO cell types are described below:
- I: Input PAD
- IK: Schmitt Trigger Input PAD
- IO12: Input/Output PAD, output driving is 12 mA
- IOD12: Input/open-drain Output PAD, output driving is 12 mA
- O12: 12mA Output PAD
- OD12: 12mA Open-Drain Output PAD

6. Register Description

6.1 Register Description

Table 6-1. List of Over Clock Registers

Register Name	R/W	Address	Default
VID Output Control Register (VFOCR)	R/W	0x00	8'h00
VID Programmed Output Register (VIDPOR)	R/W	0x02	8'h00
VID Output Register (VIDOR)	RO	0x03	8'h00
VID Input Register (VIDIR)	RO	0x04	8'h00
GPIO A Control Register (GPIOACR)	R/W	0x10	8'h00
GPIO B Control Register (GPIOBCR)	R/W	0x11	8'h00
GPIO A Data Register (GPIOADR)	R/W	0x12	8'hFF
GPIO B Data Register (GPIOBDR)	R/W	0x13	8'h0F
GPIO A Output Type Register (GPIOAOTR)	R/W	0x14	8'h00
GPIO B Output Type Register (GPIOBOTR)	R/W	0x15	8'h00
GPIO A Pull-up Resister Control Register (GPIOAPUR)	R/W	0x16	8'h00
GPIO B Pull-up Resister Control Register (GPIOBPUR)	R/W	0x17	8'h00
GPIO A Pull-down Resister Control Register (GPIOAPDR)	R/W	0x18	8'h00
GPIO B Pull-down Resister Control Register (GPIOBPDR)	R/W	0x19	8'h00
GPIO A and B Synchronize Control Register (GPIOSYNR)	R/W	0x1A	8'h00
Watch-Dog Timer Register (WDTR)	R/W	0x20	8'h00
Watch-Dog Timer Unit Register (WDTUR)	R/W	0x21	8'h00
Watch-Dog Timer Control Register (WDTCR)	R/W	0x22	8'h00

6.1.1 VID Output Control Register (VFOCR) — Offset 0x00

Bit	R/W	Default	Description
7-5	-	0h	**Reserved**
4	R/W	0h	**Dynamic VID Enable bit** 0: When this bit is set to “0”, the value of output pins VIDOUT[4:0] is the same as the value of VIDPOR register. 1: When this bit is set to “1”, the value of VIDOUT output pins is generated from the input signals VIDIN[4:0] and VIDPOR register. This bit is active when bit 1 (VIDOE) is set to 1.
3	WO	0h	**Clear New CPU Status (CLRCPU)** Write “1” to this bit to clear New CPU Status bit. To release the clear action, this bit should be written to “0” after being written to “1”. This bit is always read as “0”. Write “1” to clear this bit.
2	RO	0h	**New CPU Status (NCPU)** 0: CPU is not replaced. 1: CPU is replaced.
1	R/W	0h	**VID Output Enable (VIDOE)** 0: VIDDIN4~VIDIN0 pins pass to VIDOUT4~VIDOUT0 pins. 1: VIDOUT4~VIDOUT0 pins are controlled by VIDPOR[4:0].
0	R/W	0h	**Reserved**

6.1.2 VID Programmed Ouput Register (VIDPOR)— Offset 0x02

Bit	R/W	Default	Description
7-5	RO	0h	**Reserved**
4-0	R/W	0h	**VID Programmed Output Data (VIDPOD[4:0])** The value is valid when VIDOE bit is “1”. The sum of VIDPOD and VIDIN is output to VIDOUT4~VIDOUT0 output pins.

6.1.3 VID Ouput Register (VIDOR)— Offset 0x03

Bit	R/W	Default	Description
7-5	RO	0h	**Reserved**
4-0	RO	0h	**VID Output Data (VIDOD[4:0])** These bits store the value of VIDOUT4~VIDOUT0

6.1.4 VID Input Register (VIDIR)— Offset 0x04

Bit	R/W	Default	Description
7-5	RO	0h	**Reserved**
4-0	RO	0h	**VID Input Data (VIDID[4:0])** These bits reflect the value of VIDIN4~VIDIN0

6.1.5 GPIOA Control Register (GPIOACR)— Offset 0x10

Bit	R/W	Default	Description
7	R/W	0h	**Reserved** This bit must be set to zero.
6	R/W	0h	**GPIO 5 Input Enable** 0: GPIO 5 is an output pin. 1: GPIO 5 is an input pin.
5	R/W	0h	**GPIO 4 Input Enable** 0: GPIO 4 is an output pin. 1: GPIO 4 is an input pin.
4	R/W	0h	**GPIO 3 Input Enable** 0: GPIO 3 is an output pin. 1: GPIO 3 is an input pin.
3	R/W	0h	**Reserved** This bit must be set to zero.
2	R/W	0h	**GPIO 2 Input Enable** 0: GPIO 2 is an output pin. 1: GPIO 2 is an input pin.
1	R/W	0h	**GPIO 1 Input Enable** 0: GPIO 1 is an output pin. 1: GPIO 1 is an input pin.
0	R/W	0h	**GPIO 0 Input Enable** 0: GPIO 0 is an output pin. 1: GPIO 0 is an input pin.

6.1.6 GPIO B Control Register (GPIOBCR)— Offset 0x11

Bit	R/W	Default	Description
7-4	R/W	0h	**Reserved**
3	R/W	0h	**GPIO 9 Input Enable** 0: GPIO 9 is an output pin. 1: GPIO 9 is an input pin.
2	R/W	0h	**GPIO 8 Input Enable** 0: GPIO 8 is an output pin. 1: GPIO 8 is an input pin.
1	R/W	0h	**GPIO 7 Input Enable** 0: GPIO 7 is an output pin. 1: GPIO 7 is an input pin.
0	R/W	0h	**GPIO 6 Input Enable** 0: GPIO 6 is an output pin. 1: GPIO 6 is an input pin.

6.1.7 GPIO A Data Register (GPIOADR)— Offset 0x12

Bit	R/W	Default	Description
7	R/W	1h	**Reserved** This bit must be set to one.
6	R/W	1h	**GPIO 5 Data bit** If GPIO 5 is an input pin, this bit will be the input value from GPIO 5. If GPIO 5 is an output pin, this bit will be the value output to GPIO 5.
5	R/W	1h	**GPIO 4 Data bit** If GPIO 4 is an input pin, this bit will be the input value from GPIO 4. If GPIO 4 is an output pin, this bit will be the value output to GPIO 4.
4	R/W	1h	**GPIO 3 Data bit** If GPIO 3 is an input pin, this bit will be the input value from GPIO 3. If GPIO 3 is an output pin, this bit will be the value output to GPIO 3.
3	R/W	1h	**Reserved** This bit must be set to one.
2	R/W	1h	**GPIO 2 Data bit** If GPIO 2 is an input pin, this bit will be the input value from GPIO 2. If GPIO 2 is an output pin, this bit will be the value output to GPIO 2.
1	R/W	1h	**GPIO 1 Data bit** If GPIO 1 is an input pin, this bit will be the input value from GPIO 1. If GPIO 1 is an output pin, this bit will be the value output to GPIO 1.
0	R/W	1h	**GPIO 0Data bit** If GPIO 0 is an input pin, this bit will be the input value from GPIO 0. If GPIO 0 is an output pin, this bit will be the value output to GPIO 0.

6.1.8 GPIO B Data Register (GPIOBDR)— Offset 0x13

Bit	R/W	Default	Description
7-4	RO	0h	**Reserved**
3	R/W	1h	**GPIO 9 Data bit** If GPIO 9 is an input pin, this bit will be the input value from GPIO 9. If GPIO 9 is an output pin, this bit will be the value output to GPIO 9.
2	R/W	1h	**GPIO 8 Data bit** If GPIO 8 is an input pin, this bit will be the input value from GPIO 8. If GPIO 8 is an output pin, this bit will be the value output to GPIO 8.
1	R/W	1h	**GPIO 7 Data bit** If GPIO 7 is an input pin, this bit will be the input value from GPIO 7. If GPIO 7 is an output pin, this bit will be the value output to GPIO 7.
0	R/W	1h	**GPIO 6 Data bit** If GPIO 6 is an input pin, this bit will be the input value from GPIO 6. If GPIO 6 is an output pin, this bit will be the value output to GPIO 6.

6.1.9 GPIO A Output Type Register (GPIOAOTR)— Offset 0x14

Bit	R/W	Default	Description
7	R/W	0h	**Reserved** This bit must be set to zero.
6	R/W	0h	**GPIO 5 Output Type** 0: GPIO 5 is an open-drain output pin. 1: GPIO 5 is a push-pull output pin.
5	R/W	0h	**GPIO 4 Output Type** 0: GPIO 4 is an open-drain output pin. 1: GPIO 4 is a push-pull output pin.
4	R/W	0h	**GPIO 3 Output Type** 0: GPIO 3 is an open-drain output pin. 1: GPIO 3 is a push-pull output pin.
3	R/W	0h	**Reserved** This bit must be set to zero.
2	R/W	0h	**GPIO 2 Output Type** 0: GPIO 2 is an open-drain output pin. 1: GPIO 2 is a push-pull output pin.
1	R/W	0h	**GPIO 1 Output Type** 0: GPIO 1 is an open-drain output pin. 1: GPIO 1 is a push-pull output pin.
0	R/W	0h	**GPIO 0 Output Type** 0: GPIO 0 is an open-drain output pin. 1: GPIO 0 is a push-pull output pin.

6.1.10 GPIO B Output Type Register (GPIOBOTR)— Offset 0x15

Bit	R/W	Default	Description
7-4	RO	0h	**Reserved**
3	R/W	0h	**GPIO 9 Output Type** 0: GPIO 9 is an open-drain output pin. 1: GPIO 9 is a push-pull output pin.
2	R/W	0h	**GPIO 8 Output Type** 0: GPIO 8 is an open-drain output pin. 1: GPIO 8 is a push-pull output pin.
1	R/W	0h	**GPIO 7 Output Type** 0: GPIO 7 is an open-drain output pin. 1: GPIO 7 is a push-pull output pin.
0	R/W	0h	**GPIO 6 Output Type** 0: GPIO 6 is an open-drain output pin. 1: GPIO 6 is a push-pull output pin.

6.1.11 GPIO A Pull-up Resister Control Register (GPIOAPUR)— Offset 0x16

Bit	R/W	Default	Description
7	R/W	0h	**Reserved** This bit must be set to zero.
6	R/W	0h	**GPIO 5 Pull-up resister Enable** 0: Disable GPIO5 pull-up resister. 1: Enable GPIO5 pull-up resister.
5	R/W	0h	**GPIO 4 Pull-up resister Enable** 0: Disable GPIO4 pull-up resister. 1: Enable GPIO4 pull-up resister.
4	R/W	0h	**GPIO 3 Pull-up resister Enable** 0: Disable GPIO3 pull-up resister. 1: Enable GPIO3 pull-up resister.
3	R/W	0h	**Reserved** This bit must be set to zero.
2	R/W	0h	**GPIO 2 Pull-up resister Enable** 0: Disable GPIO2 pull-up resister. 1: Enable GPIO2 pull-up resister.
1	R/W	0h	**GPIO 1 Pull-up resister Enable** 0: Disable GPIO1 pull-up resister. 1: Enable GPIO1 pull-up resister.
0	R/W	0h	**GPIO 0 Pull-up resister Enable** 0: Disable GPIO0 pull-up resister. 1: Enable GPIO0 pull-up resister.

6.1.12 GPIO B Pull-up Resister Control Register (GPIOBPUR)— Offset 0x17

Bit	R/W	Default	Description
7-4	RO	0h	**Reserved**
3	R/W	0h	**GPIO 9 Pull-up resister Enable** 0: Disable GPIO 9 pull-up resister. 1: Enable GPIO 9 pull-up resister.
2	R/W	0h	**GPIO 8 Pull-up resister Enable** 0: Disable GPIO 8 pull-up resister. 1: Enable GPIO 8 pull-up resister.
1	R/W	0h	**GPIO 7 Pull-up resister Enable** 0: Disable GPIO 7 pull-up resister. 1: Enable GPIO 7 pull-up resister.
0	R/W	0h	**GPIO 6 Pull-up resister Enable** 0: Disable GPIO 6 pull-up resister. 1: Enable GPIO 6 pull-up resister.

6.1.13 GPIO A Pull-down Resister Control Register (GPIOAPDR)— Offset 0x18

Bit	R/W	Default	Description
7	R/W	0h	**Reserved** This bit must be set to zero.
6	R/W	0h	**GPIO 5 Pull-down resister Enable** 0: Disable GPIO5 pull-down resister. 1: Enable GPIO 5 pull-down resister.
5	R/W	0h	**GPIO 4 Pull-down resister Enable** 0: Disable GPIO 4 pull-down resister. 1: Enable GPIO 4 pull-down resister.
4	R/W	0h	**GPIO 3 Pull-down resister Enable** 0: Disable GPIO 3 pull-down resister. 1: Enable GPIO 3 pull-down resister.
3	R/W	0h	**Reserved** This bit must be set to zero.
2	R/W	0h	**GPIO 2 Pull-down resister Enable** 0: Disable GPIO2 pull-down resister. 1: Enable GPIO2 pull-down resister.
1	R/W	0h	**GPIO 1 Pull-down resister Enable** 0: Disable GPIO1 pull-down resister. 1: Enable GPIO1 pull-down resister.
0	R/W	0h	**GPIO 0 Pull-down resister Enable** 0: Disable GPIO0 pull-down resister. 1: Enable GPIO0 pull-down resister.

6.1.14 GPIO B Pull-down Resister Control Register (GPIOBPDR)— Offset 0x19

Bit	R/W	Default	Description
7-4	RO	0h	**Reserved**
3	R/W	0h	**GPIO 9 Pull-down resister Enable** 0: Disable GPIO 9 pull-down resister. 1: Enable GPIO 9 pull-down resister.
2	R/W	0h	**GPIO 8 Pull-down resister Enable** 0: Disable GPIO 8 pull-down resister. 1: Enable GPIO 8 pull-down resister.
1	R/W	0h	**GPIO 7 Pull-down resister Enable** 0: Disable GPIO 7 pull-down resister. 1: Enable GPIO 7 pull-down resister.
0	R/W	0h	**GPIO 6 Pull-down resister Enable** 0: Disable GPIO 6 pull-down resister. 1: Enable GPIO 6 pull-down resister.

6.1.15 GPIO A and B Synchronize Control Register (GPIOSYNR)— Offset 0x1A

Bit	R/W	Default	Description
7-2	RO	0h	**Reserved**
1	R/W	0h	**GPIO 9-0 Data out trigger** If GPIO 9~0 synchronize enable (bit 0), if this bit set to 1, the GPIO9 ~0 data is output to PAD. Write 0 to reset this bit.
0	R/W	0h	**GPIO 9~0 Synchronize Enable** 0: Disable GPIO 9-0 synchronize output. 1: Enable GPIO 9-0 synchronize output.

6.1.16 Watch-Dog Timer Register (WDTR)— Offset 0x20

Bit	R/W	Default	Description
7-0	R/W	0h	**Watch-Dog Timer** Read this register means how much time left that watch-dog will be timeout.

6.1.17 Watch-Dog Timer Unit Register (WDTUR)— Offset 0x21

Bit	R/W	Default	Description
7-4	RO	0h	**Reserved**
3-2	R/W	0h	**Watch-Dog Timer time-unit select** 2'b00: 1 s 2'b01: 0.1 s 2'b10: 10 ms 2/b11: 1 ms
1-0	R/W	0h	**RSTOUT# pulse width select** 2'b00: 1 s 2'b01: 0.1 s 2'b10: 10 ms 2/b11: 1 ms

6.1.18 Watch-Dog Timer Control Register (WDTCSR)— Offset 0x22

Bit	R/W	Default	Description
7-2	RO	0h	**Reserved**
1	R/W	0h	**Watch-Dog Time-out** 0: No watch-dog timeout event 1: watch-dog timeout occurred. Writing 1 can clear this bit.
0	R/W	0h	**Watch-Dog Timer Enable** 0: Disable watch-dog timer 1: Enable watch-dog timer

7. DC Characteristics

Absolute Maximum Ratings

Power Supply (V_{CC}) ..... -0.3V to 3.6V

Input Voltage ..... -0.3V to VCC + 0.3V

Output Voltage ..... -0.3V to VCC + 0.3V

Storage Temperature ..... -55°C to 150°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (Operation Condition Vcc=3.0V~3.6V, Tj=0°C~115°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	CMOS	-	-	0.3*Vcc	V
V_{IH}	Input High Voltage	CMOS	0.7*Vcc	-	-	V
Vt-	Schmitt trigger negative going threshold voltage	CMOS	-	1.20	-	V
Vt+	Schmitt trigger positive going threshold voltage	CMOS	-	2.10	-	V
V_{OL}	Output Low Voltage	I_{OL}= -12mA	-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}= -12mA	2.4	-	-	V
R_I	Input Pull-up resistance	V_{IL}=0V or V_{IH}=Vcc	-	75	-	KΩ
I_{IL}	Input Leakage current	no pull-up	-1	-	1	uA
I_{OZ}	Tri-state leakage current		-1	-	1	mA
C_{IN}	Input capacity		-	10	-	pF
C_{OUT}	Output capacity		-	10	-	pF
C_{BID}	Bi-directional buffer capacity		-	10	-	pF

8. AC Characteristics

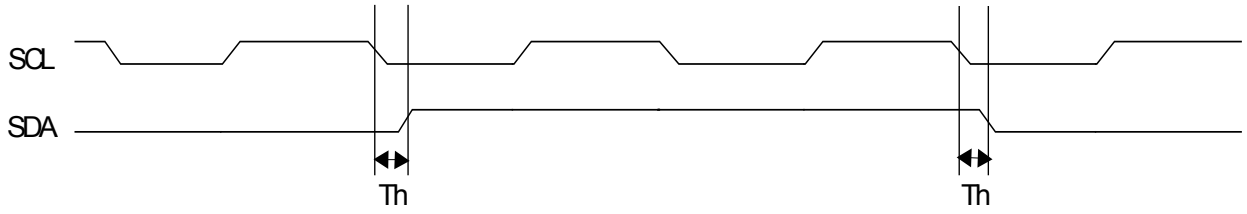


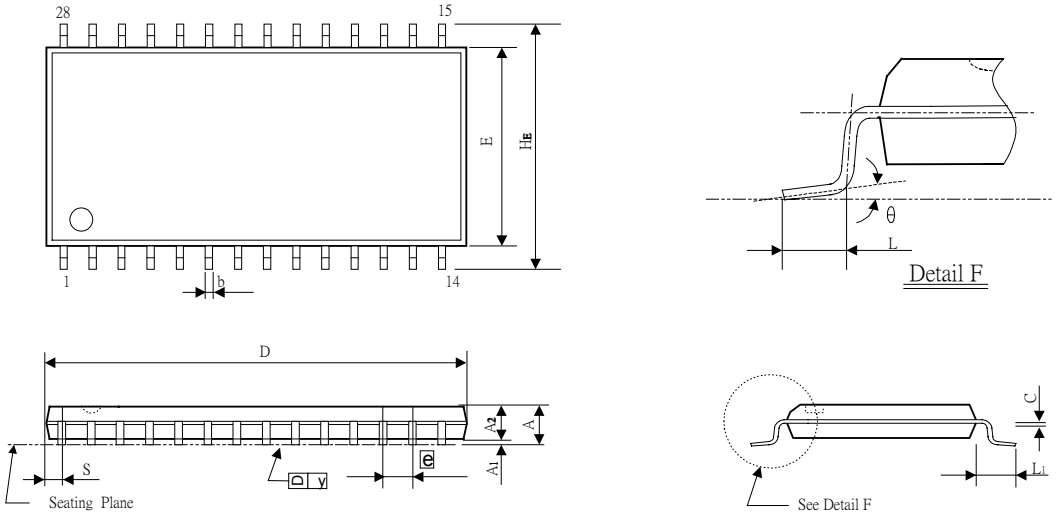
Figure 8-1. Serial Bus Waveform

Table 8-1. Serial Bus AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_h	Data Hold Time	-	300	-	ns

9. Package Information

SSOP 28L Outline Dimensions unit: inches/mm



Symbol	Dimension in inches			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.053	0.064	0.069	1.35	1.63	1.75
A1	0.004	0.006	0.010	0.10	0.152	0.25
A2	—	—	0.059	—	—	1.50
b	0.008	0.010	0.012	0.203	0.254	0.305
C	0.007	—	0.010	0.178	—	0.250
D	0.386	0.390	0.394	9.80	9.91	10.00
E	0.150	0.154	0.157	3.80	3.91	4.00
e	0.025BSC			0.635BSC		
HE	0.228	0.236	0.244	5.80	5.99	6.20
L	0.016	0.025	0.050	0.40	0.635	1.27
L1	0.041REF.			1.04REF.		
S	0.033REF.			0.838REF.		
y	—	—	0.004	—	—	0.10
θ	0°	—	8°	0°	—	8°

10. Ordering Information

Part No.	Package
IT8203R	28-SSOP