RICMOS™ SEA OF TRANSISTORS GATE ARRAY HR2210

FEATURES

RADIATION HARDNESS

- Total Dose Hardness of ≥1x10^6 rad(SiO_2)
- Dose Rate Upset Hardness ≥ 1x10^9 rad(Si)/sec
- Dose Rate Survivability ≥ 1x10^{12} rad(Si)/sec
- SEU Immunity to 1x10^{-10} Errors/Bit-Day (Flip-Flops & SRAMs)
- Neutron Fluence Hardness to 1x10^{14}/cm^2

PERFORMANCE

- Typical Gate Delays of 0.35 ns (Post-Radiation)
- Flip-Flop Toggle Frequencies of 410 MHz
- Capable of Supporting System Speeds of 50 MHz

OTHER

- In production on Honeywell's 0.8 µm Minimum Feature RICMOS™ Epitaxial Process
- Outside Foundry Netlist Import Capability
- 210K Gates: 90K Usable Minimum
- I/O Compiler With Over 1000 Options
- Compatible with TTL or CMOS
- Military Screening to Class B or Class S
- Configurable 16K Multiport SRAM or 106K ROM
- Soft Macro Compilers
- 8 Different Multiport SRAM Options
- Up to 276 Usable I/O Pads

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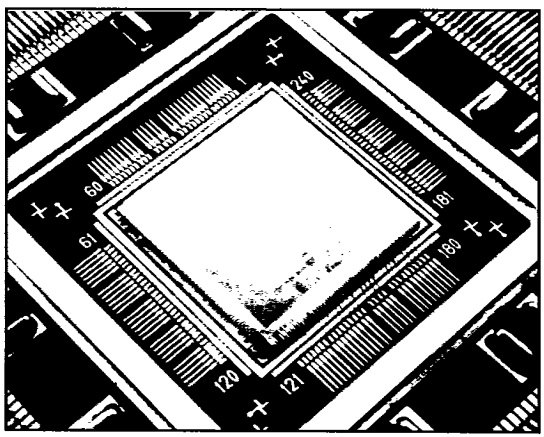
GENERAL DESCRIPTION

The RICMOS™ HR2210 is a performance oriented radiation-hardened sea of transistors gate array based on the 0.8 µm RICMOS™ process. The high density and performance characteristics of the RICMOS™ process allow the HR2210 to operate up to 50 MHz over the full military temperature range after exposure to ionizing radiation exceeding 1x10^6 rad(SiO_2). Flip-Flops and SRAMs have been hardened and demonstrated to a Soft Error Rate (SER) less than 1x10^{-10} errors/bit-day.

Logic designers need not have a background in radiation hardening. Honeywell's VDS ToolKit™ provides a full suite of user friendly design tools encompassing static timing analysis, test program generation, and automated place and route. User friendliness is enhanced through the use of design aids known as soft macro compilers which increase the designer's productivity during the schematic capture phase of the design cycle. The library for the HR2210 is virtually identical to Honeywell's RSCL (RICMOS™ Standard Cell Library) and Honeywell's RICMOS™ 1.2 µm gate arrays.

HR2210's design system contains 32 SSI logic elements, 16 data storage elements, 5 MSI soft macro compilers, 2 LSI supercells, and over 1000 I/O pad options. The library allows system integration of over 90,000 gates per chip with up to 276 signal pins. Each I/O site can be either Input, Output, or Bidirectional. The HR2210 features a global clock network capable of handling up to ten separate clock signals with a minimum amount of clock skew between registers. The HR2210 also supports SSD (Synchronous Scan Design) which permits scan path testing on all flip-flops and registers. This approach to testability segments the design and greatly reduces test time. The HR2210 is fully compatible with Honeywell's high reliability military screening procedures to both Class B and Class S requirements.



HR2210 Characteristics	
Raw / Usable Gate Count	206,712 / 90,000 Core Gates
Boundary Scan Gate Count	11,692 I/O Gates
Typical Delay	0.35 ns
Maximum Flip-Flop Toggle Frequency	410 MHz
I/O Interface Levels	CMOS, LSTTL
Input/Output Pins	Up to 276
Typical Power Dissipation	0.5 to 2.5W
Operating Temperature	-55 to 125°C
Process Technology (1)	RICMOS™
Minimum Geometry	0.8 µm
Design-For-Test Technique(2)	SSD / IEEE 1149.1 Boundary Scan

(1) RICMOS™ (Radiation Insensitive CMOS) process technology
(2) SSD (Synchronous Scan Design). Refer to Honeywell's RICMOS™ ASIC Library data book for more information.

The HR2210 provides cell options of configurable multiport SRAMs and configurable ROMs. Both can be sized in single bit increments. The SRAM has a maximum size of 16K bits and can be structured as a synchronous or asynchronous memory. The ROM is contact programmable to a maximum size of 106K bits. A 20K SRAM or 130K ROM would occupy about 30% of the HR2210 die.

Eight multiport SRAM options are available: 1 read/write, 1 read and 1 write, 2 read/write, 1 read/write and 1 read, 1 read/write and 1 write, 1 write and 2 read, 2 write and 1 read, or 2 write and 2 read.

I/O cells can be arranged for boundary scan and are IEEE 1149.1 compatible. An I/O compiler with over 1000 options allow configuration for TTL/ CMOS with 7 drive options, 3 slew rate options, pull up/pull down resistors, ringlatch, Schmitt triggers, and boundary scan.

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