Section 22 Electrical Characteristics

22.1 Absolute Maximum Ratings

Table 22-1 lists the absolute maximum ratings.

Table 22-1 Absolute Maximum Ratings – Preliminary –

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage (except port 4)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (port 4)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference voltage	V_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum rating are exceeded.

22.2 DC Characteristics

Table 22-2 lists the DC characteristics. Table 22-3 lists the permissible output currents.

Table 22-2 DC Characteristics – Preliminary –

Conditions: $V_{CC} = AV_{CC} = 5.0\ V \pm 10\%$, $V_{ref} = 4.5\ V$ to AV_{CC}, $V_{SS} = AV_{SS} = 0\ V$*1, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Port 2, $P6_4$ to $P6_7$, PA_4 to PA_7	V_T^-	1.0	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$	V	
		$V_T^+ - V_T^-$	0.4	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	V_{IH}	$V_{CC} \times 0.7$	—	V_{CC} +0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} +0.3	V	
	Port1,3,5, B to G, $P6_0$ to $P6_3$, PA_0 to PA_3		2.0	—	V_{CC} +0.3	V	
	Port4		2.0	—	AV_{CC} +0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0	V_{IL}	–0.3	—	0.5	V	
	NMI, EXTAL, Port1,3 to 5, B to G, $P6_0$ to $P6_3$, PA_0 to PA_3		–0.3	—	0.8	V	
Output high voltage	All output pins	V_{OH}	V_{CC} –0.5	—	—	V	$I_{OH} = -200\ \mu A$
			3.5	—	—	V	$I_{OH} = -1$ mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	$I_{OL} = 1.6$ mA
	Port1, A to C		—	—	1.0	V	$I_{OL} = 10$ mA
Input leakage current	$\overline{STBY}$, $\overline{RES}$, NMI, MD_2 to MD_0	I_{in}	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} –0.5 V
	Port4		—	—	1.0	µA	V_{in} = 0.5 to AV_{CC} –0.5 V

Note: 1. IF the A/D converter is not used,do not leave the AV_{CC}, AV_{SS}, and V_{ref} pins open. Connect AV_{CC} and V_{ref} to V_{CC}, and connect AV_{SS} to V_{SS}.

Table 22-2 DC Characteristics (cont) – Preliminary –

Conditions: $V_{CC} = AV_{CC} = 5.0\ V \pm 10\%$, $V_{ref} = 4.5\ V$ to AV_{CC}, $V_{SS} = AV_{SS} = 0\ V$*1, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Three-state leakage current (off state)	Port1 to 3, 5, 6, A to G	$\|I_{TSI}\|$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} –0.5 V
Input pull-up current	Port A to E	$-I_P$	50	—	300	µA	V_{in} = 0 V
Input capacitance	NMI	C_{IN}	—	—	50	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	All input pins except NMI		—	—	15	pF	
Current dissipation*2	Normal operation	I_{CC}*4	—	TBD	TBD	mA	f = 20 MHz
	Sleep mode		—	TBD	TBD	mA	f = 20 MHz
	Standby mode*3		—	0.01	5.0	µA	$T_a \le 50°C$
			—	—	20.0		$50°C < T_a$
Analog power supply current	During A/D conversion	AI_{CC}	—	TBD	TBD	mA	
	Idle		—	0.01	5.0	µA	
Reference current	During A/D conversion	AI_{CC}	—	TBD	TBD	mA	
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. If the A/D converter is not used,do not leave the AV_{CC}, AV_{SS}, and V_{ref} pins open. Connect AV_{CC} and V_{ref} to V_{CC}, and connect AV_{SS} to V_{SS}.
2. Current dissipation values are for V_{IH} min = V_{CC} –0.5 V and V_{IL} max = 0.5V with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for $V_{RAM} \le V_{CC} < 4.5V$, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.
4. I_{CC} depends on V_{CC} and f as follows:
I_{CC} max = TBD (mA) + TBD (mA/MHz.V) × V_{CC} × f [normal mode]
I_{CC} max = TBD (mA) + TBD (mA/MHz.V) × V_{CC} × f [sleep mode]

Table 22-2 DC Characteristics (cont) – Preliminary –

Conditions: $V_{CC} = AV_{CC} = 2.7$ to 5.5 V V_{ref}=2.7 V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V*[1], $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Port 2, $P6_4$ to $P6_7$, PA_4 to PA_7	V_T^-	$V_{CC} \times 0.2$	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$	V	
		$V_T^+ - V_T^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	VIH	$V_{CC} \times 0.9$	—	V_{CC} +0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} +0.3	V	
	Port1, 3, 5, B to G, $P6_0$ to $P6_3$, PA_0 to PA_3		$V_{CC} \times 0.7$	—	V_{CC} +0.3	V	
	Port4		$V_{CC} \times 0.7$	—	AV_{CC} +0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, Port1, 3 to 5, B to G, $P6_0$ to $P6_3$, PA_0 to PA_3		–0.3	—	$V_{CC} \times 0.2$	V	$V_{CC} < 4.0$ V
					0.8		V_{CC} = 4.0 to 5.5 V
Output high voltage	All output pins	V_{OH}	V_{CC} –0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} –1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Port1, A to C		—	—	1.0	V	I_{OL} = 10 mA
Input leakage current	$\overline{STBY}$, $\overline{RES}$, NMI, MD_2 to MD_0	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{IN} = 0.5 to V_{CC} –0.5V
	Port4		—	—	1.0	µA	V_{IN} = 0.5 to AV_{CC} –0.5V

Note: 1. IF the A/D converter is not used,do not leave the AV_{CC}, AV_{SS}, and V_{ref} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.

Table 22-2 DC Characteristics (cont) – Preliminary –

Conditions: $V_{CC} = AV_{CC} = 2.7$ to 5.5 V V_{ref}=2.7 V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V*1, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Three-state leakage current (off state)	Port1 to 3, 5, 6, A to G	$\|I_{TSI}\|$	—	—	1.0	µA	V_{IN} = 0.5 to V_{CC} –0.5 V
Input pull-up current	Port A to E	$-I_P$	10	—	300	µA	V_{CC} = 2.7 V to 5.5 V, V_{IN} = 0 V
Input capacitance	NMI	C_{IN}	—	—	50	pF	V_{IN} = 0 V f = 1 MHz T_a = 25°C
	All input pins except NMI		—	—	15	pF	
Current dissipation*2	Normal operation	I_{CC}*4	—	TBD	TBD	mA	f = 10 MHz
	Sleep mode		—	TBD	TBD	mA	f = 10 MHz
	Standby mode*3		—	0.01	5.0	µA	$T_a \leq 50$°C
			—	—	20.0		50°C < T_a
Analog power supply current	During A/D conversion	AI_{CC}	—	TBD	TBD	mA	
	Idle		—	0.01	5.0	µA	
Reference current	During A/D conversion	AI_{CC}	—	TBD	TBD	mA	
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. If the A/D converter is not used,do not leave the AV_{CC}, AV_{SS}, and V_{ref} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.
2. Current dissipation values are for V_{IH} min = V_{CC} –0.5 V and V_{IL} max = 0.5V with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 2.7$ V, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3V.
4. I_{CC} depends on V_{CC} and f as follows:
I_{CC} max = TBD (mA) + TBD (mA/MHz × V) × V_{CC} × f [normal mode]
I_{CC} max = TBD (mA) + TBD (mA/MHz × V) × V_{CC} × f [sleep mode]

Table 22-3 Permissible Output Currents – Preliminary –

Conditions: $V_{CC} = AV_{CC} = 2.7$ to 5.5 V, $V_{ref} = 2.7$ to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	Port1, A to C	I_{OL}	—	—	10	mA
	Other output pins		—	—	2.0	mA
Permissible output low current (total)	Total of 32 pins including port1 and A to C	ΣI_{OL}	—	—	80	mA
	Total of all output pins, including the above		—	—	120	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	40	mA

Notes: 1. To protect chip reliability, do not exceed the output current values in table 22-3.
2. When driving a darlington pair or LED, always insert a current-limiting resister in the output line, as show in figures 22-1 and 22-2.

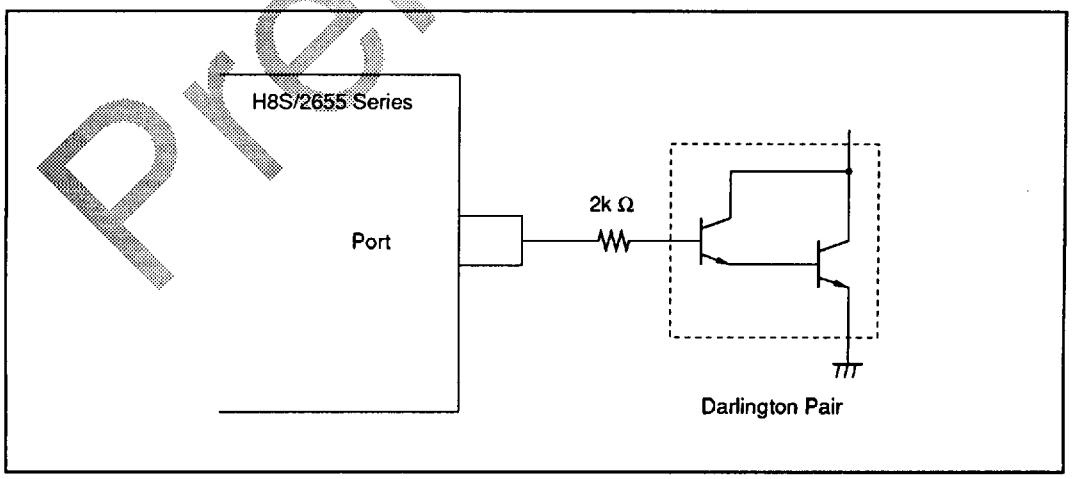

Figure 22-1 Darlington Pair Drive Circuit (Example)

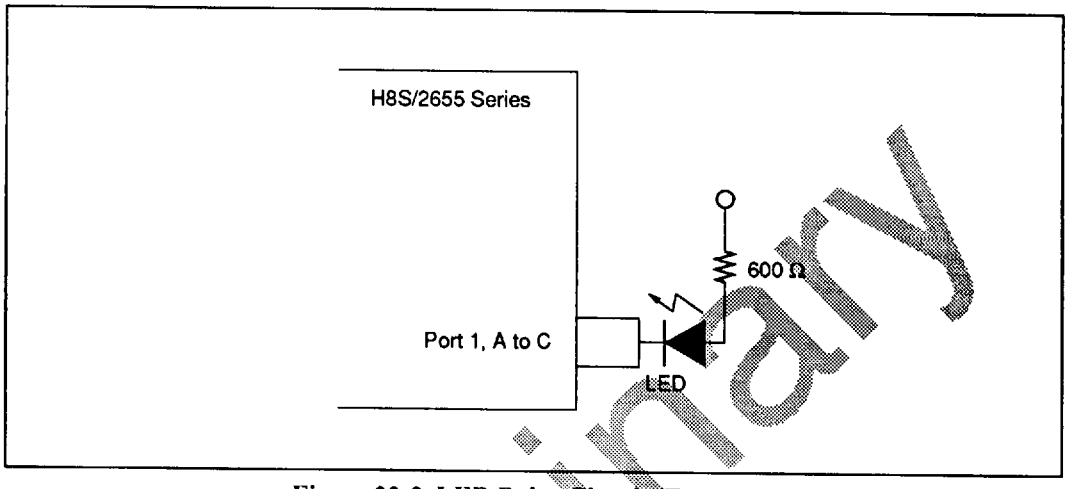

Figure 22-2 LED Drive Circuit (Example)

22.3 AC Characteristics

Figure 22-3 show, the test conditions for the AC characteristics.

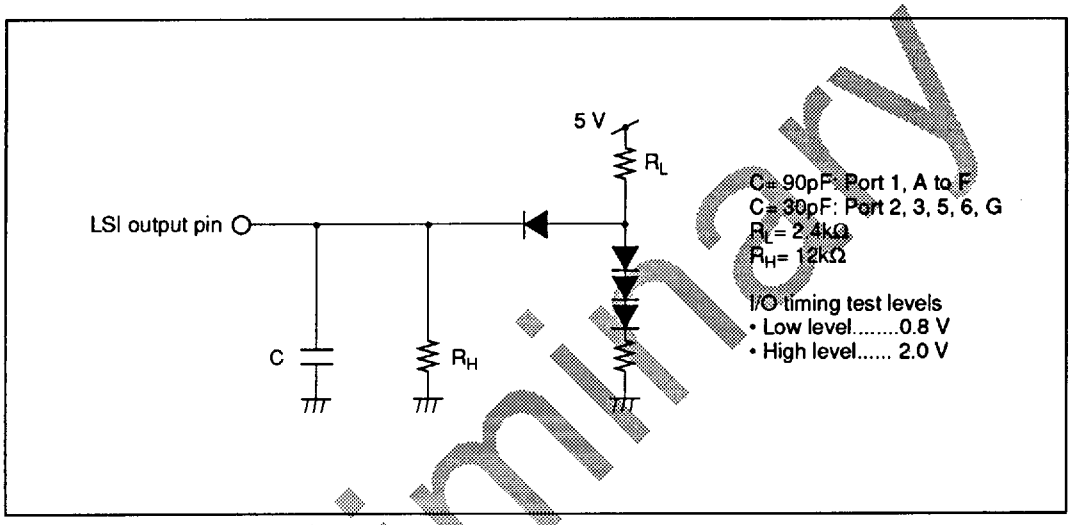

Figure 22-3 Output Load Circuit

22.3.1 Clock Timing

Table 22-4 lists the clock timing

Table 22-4 Clock Timing – Preliminary –

Condition A: $V_{CC} = AV_{CC} = 2.7$ V to 5.5 V, $V_{ref} = 2.7$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, ø = 2 to 10 MHz, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Condition B: $V_{CC} = AV_{CC} = 5.0$ V ± 10%, $V_{ref} = 4.5$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, ø = 2 to 20 MHz, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Item	Symbol	Min	Max	Unit	Test Conditions
Clock cycle time	t_{cyc}	50	2000	ns	22.4
Clock high pulse width	t_{CH}	20	—	ns	22.4
Clock low pulse width	t_{CL}	20	—	ns	
Clock rise time	t_{Cr}	—	5	ns	
Clock delay time	t_{Cf}	—	5	ns	
Clock oscillator setting time at reset (crystal)	t_{OSC1}	10	—	ms	22.5
Clock oscillator setting time in software standby (crystal)	t_{OSC2}	10	—	ms	
External clock output stabilization delay time	t_{DEXT}	500	—	µs	

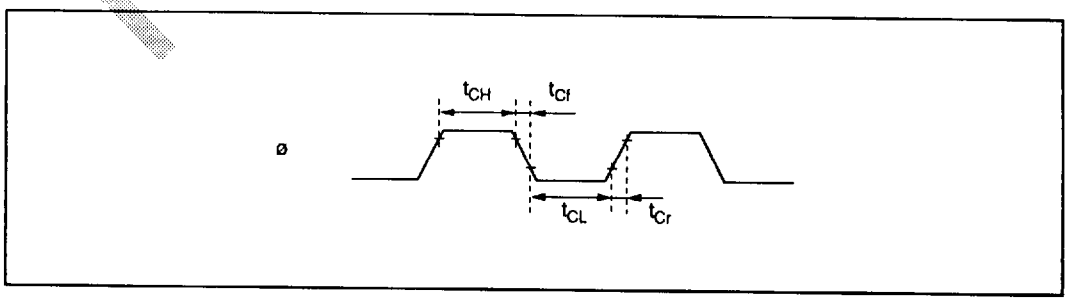

Figure 22-4 System Clock Timing

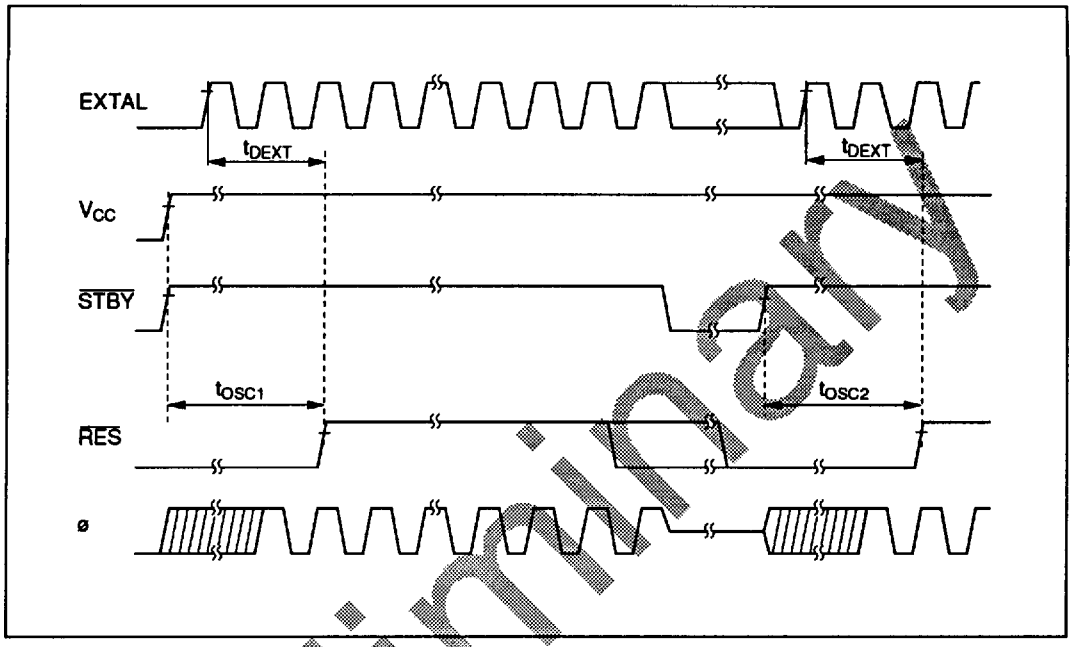

Figure 22-5 Oscillator Settling Timing

22.3.2 Control Signal Timing

Table 22-5 lists the control signal timing.

Table 22-5 Control Signal Timing – Preliminary –

Condition A: $V_{CC} = AV_{CC} = 2.7$ V to 5.5 V, $V_{ref} = 2.7$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, ø = 2 to 10 MHz, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Condition B: $V_{CC} = AV_{CC} = 5.0$ V ± 10%, $V_{ref} = 4.5$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, ø = 2 to 20 MHz, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

		Condition A		Condition B			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	ns	Figure 22-6
$\overline{RES}$ pulse width	t_{RESW}	10	—	10	—	t_{cyc}	
NMI setup time	t_{NMIS}	150	—	150	—	ns	Figure 22-7
NMI hold time	t_{NMIH}	10	—	10	—		
NMI pulse width (exiting software standby mode)	t_{NMIW}	200	—	200	—	ns	
IRQ setup time	t_{IRQS}	150	—	150	—	ns	
IRQ hold time	t_{IRQH}	10	—	10	—	ns	
IRQ pulse width (exiting software standby mode)	t_{IRQW}	200	—	200	—	ns	

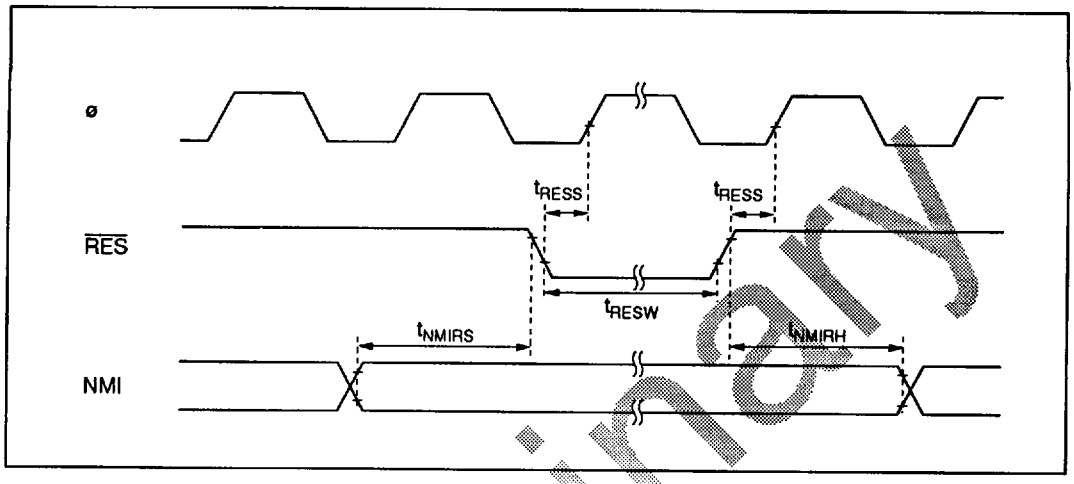

Figure 22-6 Reset Input Timing

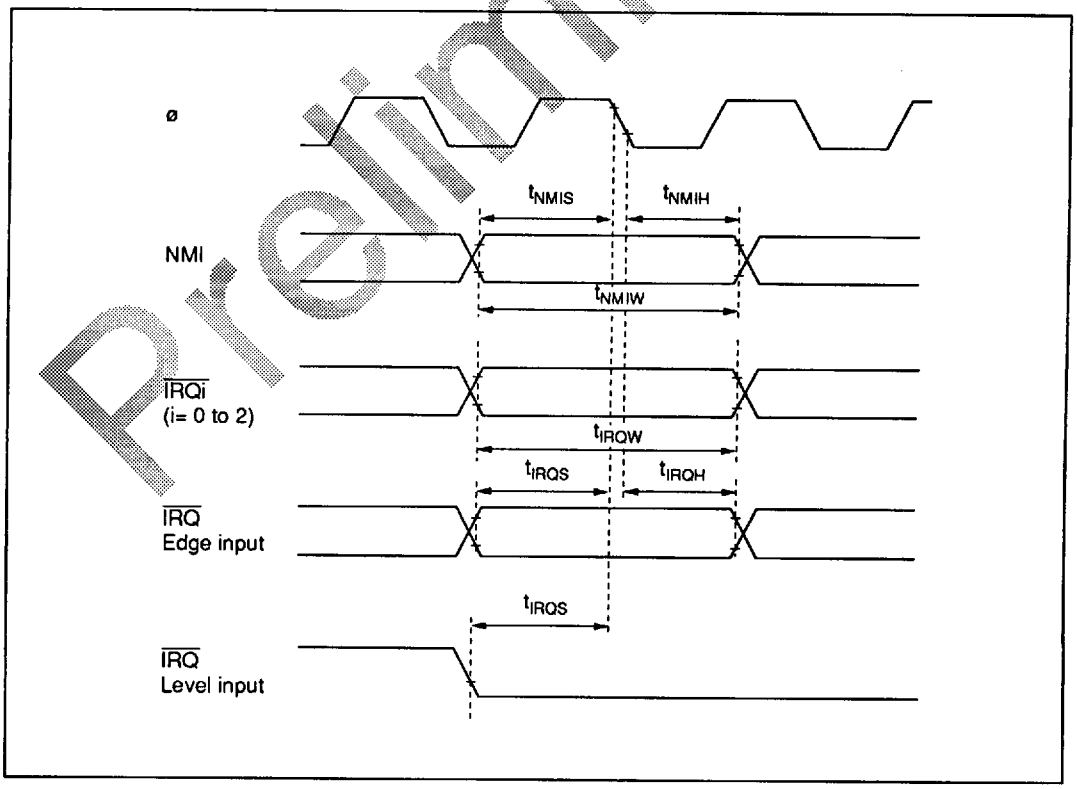

Figure 22-7 Interrupt Input Timing

22.3.3 Bus Timing

Table 22-6 lists the bus timing.

Table 22-6 Bus Timing – Preliminary –

Condition A: $V_{CC} = AV_{CC} = 2.7$ V to 5.5 V, $V_{ref} = 2.7$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, ø = 2 to 10 MHz, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Condition B: $V_{CC} = AV_{CC} = 5.0$ V ± 10%, $V_{ref} = 4.5$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, ø= 2 to 20 MHz, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

		Condition A		Condition B			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Address delay time	t_{AD}	—	40	—	20	ns	
Address setup time	t_{AS}	TBD	—	TBD	—	ns	
Address hold time	t_{AH}	TBD	—	TBD	—	ns	
Precharge time	t_{PCH}	1.5 × t_{cyc} –40	—	1.5 × t_{cyc} –20	—	ns	
$\overline{CS}$ delay time 1	t_{CSD1}	—	40	—	20	ns	
$\overline{CS}$ delay time 2	t_{CSD2}	—	40	—	20	ns	
$\overline{CS}$ pulse width	t_{CSW}	2.5 × t_{cyc} –40	—	2.5 × t_{cyc} –20	—	ns	
$\overline{AS}$ delay time	t_{ASD}	—	60	—	30	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	60	—	30	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	60	—	30	ns	
$\overline{CAS}$ delay time	t_{CASD}	—	40	—	20	ns	
Read data setup time	t_{RDS}	—	30	—	15	ns	
Read data hold time	t_{RDH}	—	0	—	0	ns	
Read data access time1	t_{ACC1}	—	1.0 × t_{cyc} –50	—	1.0 × t_{cyc} –25	ns	
Read data access time2	t_{ACC2}	—	1.5 × t_{cyc} –50	—	1.5 × t_{cyc} –25	ns	
Read data access time3	t_{ACC3}	—	2.0 × t_{cyc} –50	—	2.0 × t_{cyc} –25	ns	
Read data access time4	t_{ACC4}	—	2.5 × t_{cyc} –50	—	2.5 × t_{cyc} –25	ns	

Table 22-6 Bus Timing (cont) – Preliminary –

Condition A: $V_{CC} = AV_{CC} = 2.7$ V to 5.5 V, $V_{ref} = 2.7$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, ø = 2 to 10 MHz, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Condition B: $V_{CC} = AV_{CC} = 5.0$ V ± 10%, $V_{ref} = 4.5$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, ø = 2 to 20 MHz, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

		Condition A		Condition B			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Read data access time5	t_{ACC5}	—	3.0 × t_{cyc} –50	—	3.0 × t_{cyc} –25	ns	
$\overline{WR}$ delay time 1	t_{WRD1}	—	60	—	30	ns	
$\overline{WR}$ delay time 2	t_{WRD2}	—	60	—	30	ns	
$\overline{WR}$ pulse width 1	t_{WSW1}	—	1.0 × t_{cyc} –40	—	1.0 × t_{cyc} –20	ns	
$\overline{WR}$ pulse width 2	t_{WSW2}	—	1.5 × t_{cyc} –0	—	1.5 × t_{cyc} –20	ns	
Write data delay time	t_{WDD}	—	TBD	—	TBD	ns	
Write data setup time	t_{WDS}	0	—	0	—	ns	
Write data hold time	t_{WDH}	20	—	10	—	ns	
$\overline{WR}$ setup time	t_{WCS}	0.5 × t_{cyc} –20	—	0.5 × t_{cyc} –10	—	ns	
$\overline{WR}$ hold time	t_{WHS}	0.5 × t_{cyc} –20	—	0.5 × t_{cyc} –10	—	ns	
$\overline{CAS}$ setup time	t_{CSR}	0.5 × t_{cyc} –20	—	0.5 × t_{cyc} –10	—	ns	
$\overline{WAIT}$ setup time	t_{WTS}	60	—	30	—	ns	
$\overline{WAIT}$ hold time	t_{WTH}	10	—	5	—	ns	
$\overline{BREQ}$ setup time	t_{BRQS}	60	—	30	—	ns	
$\overline{BACK}$ delay time	t_{BACD}	—	60	—	30	ns	
Bus-floating time	t_{BZD}	—	100	—	50	ns	
$\overline{BREQO}$ delay time	t_{BRQOD}	—	60	—	30	ns	

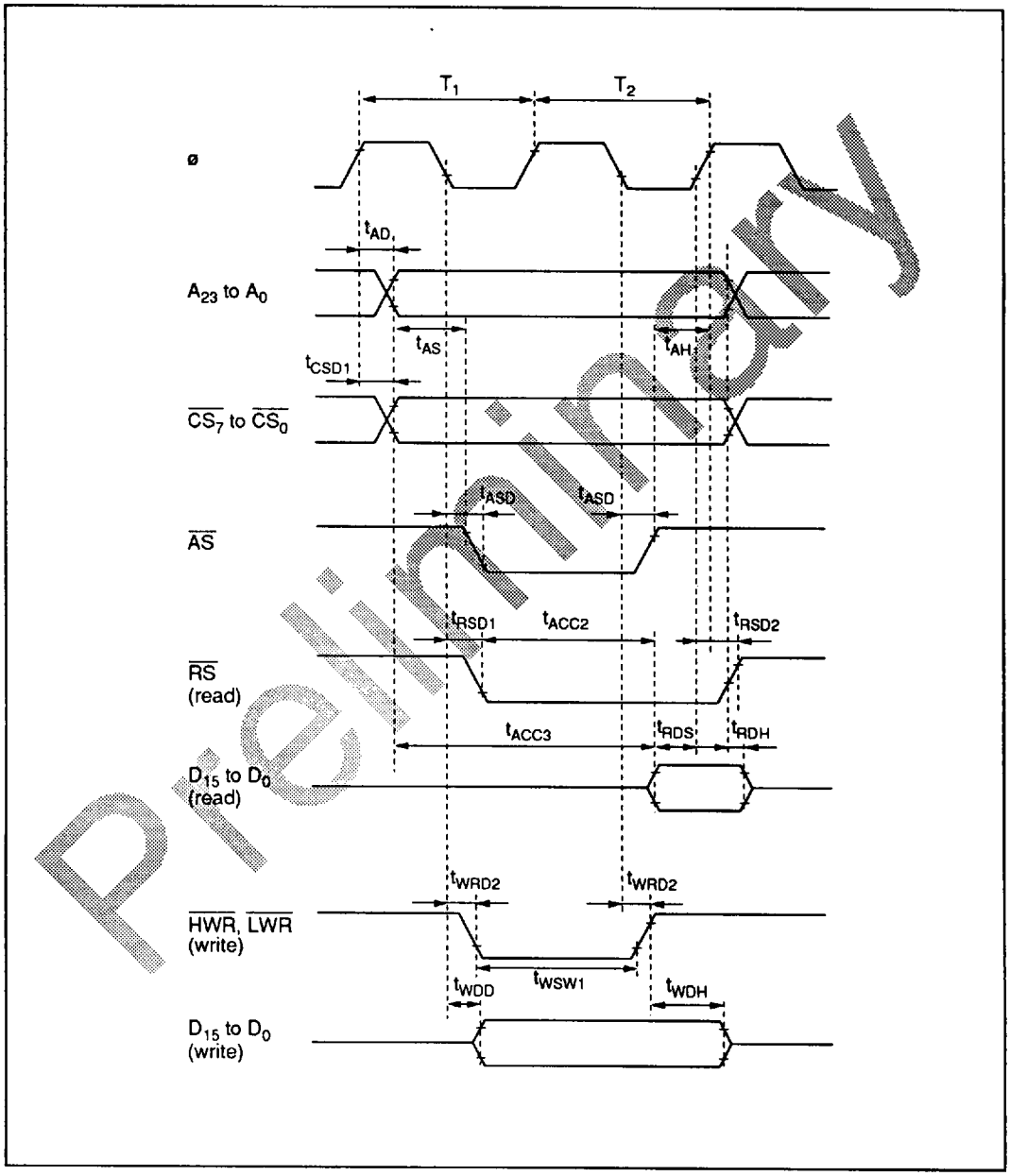

Figure 22-8 Basic Bus Timing: Two-State Access

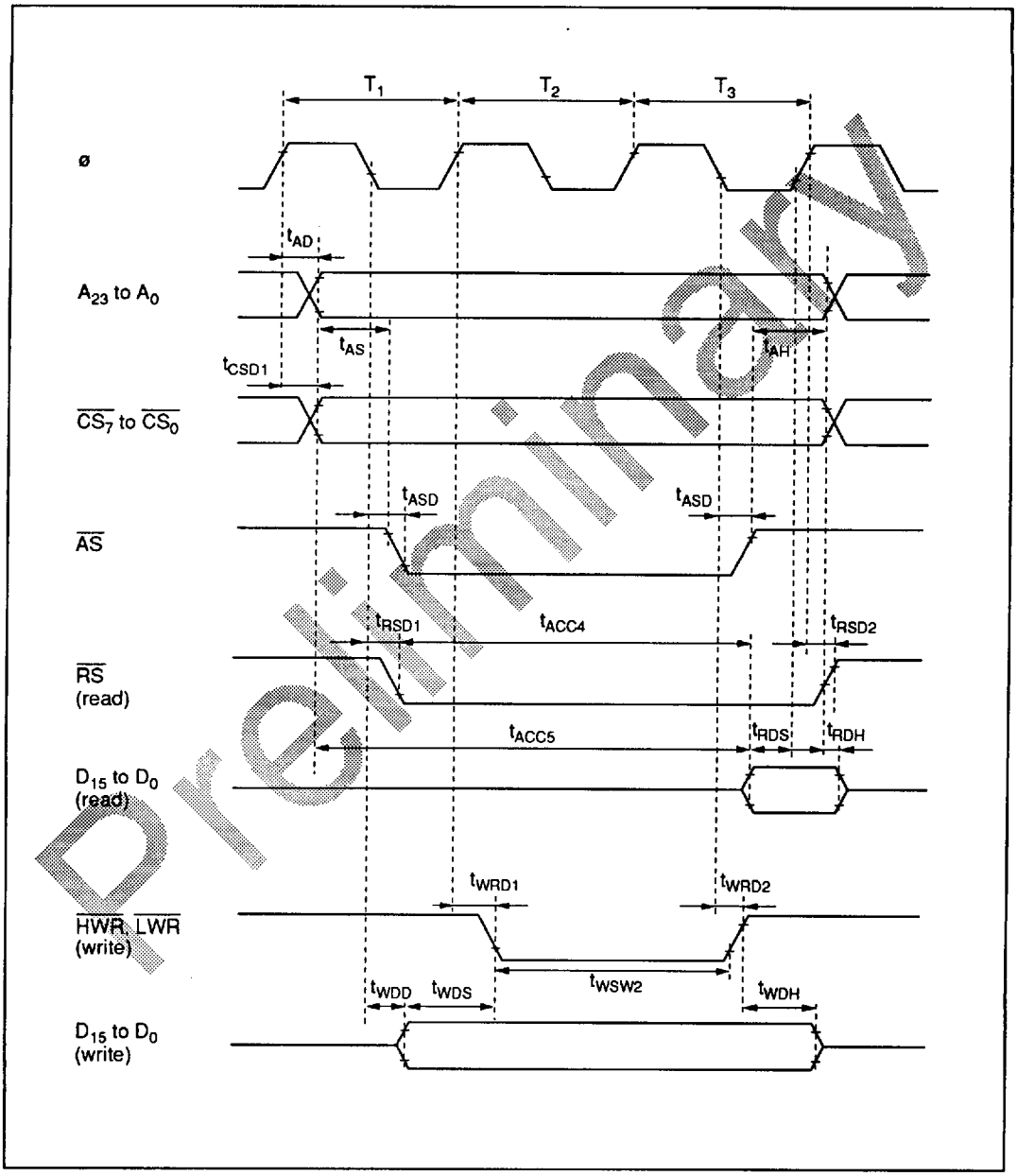

Figure 22-9 Basic Bus Timing: Three-State Access

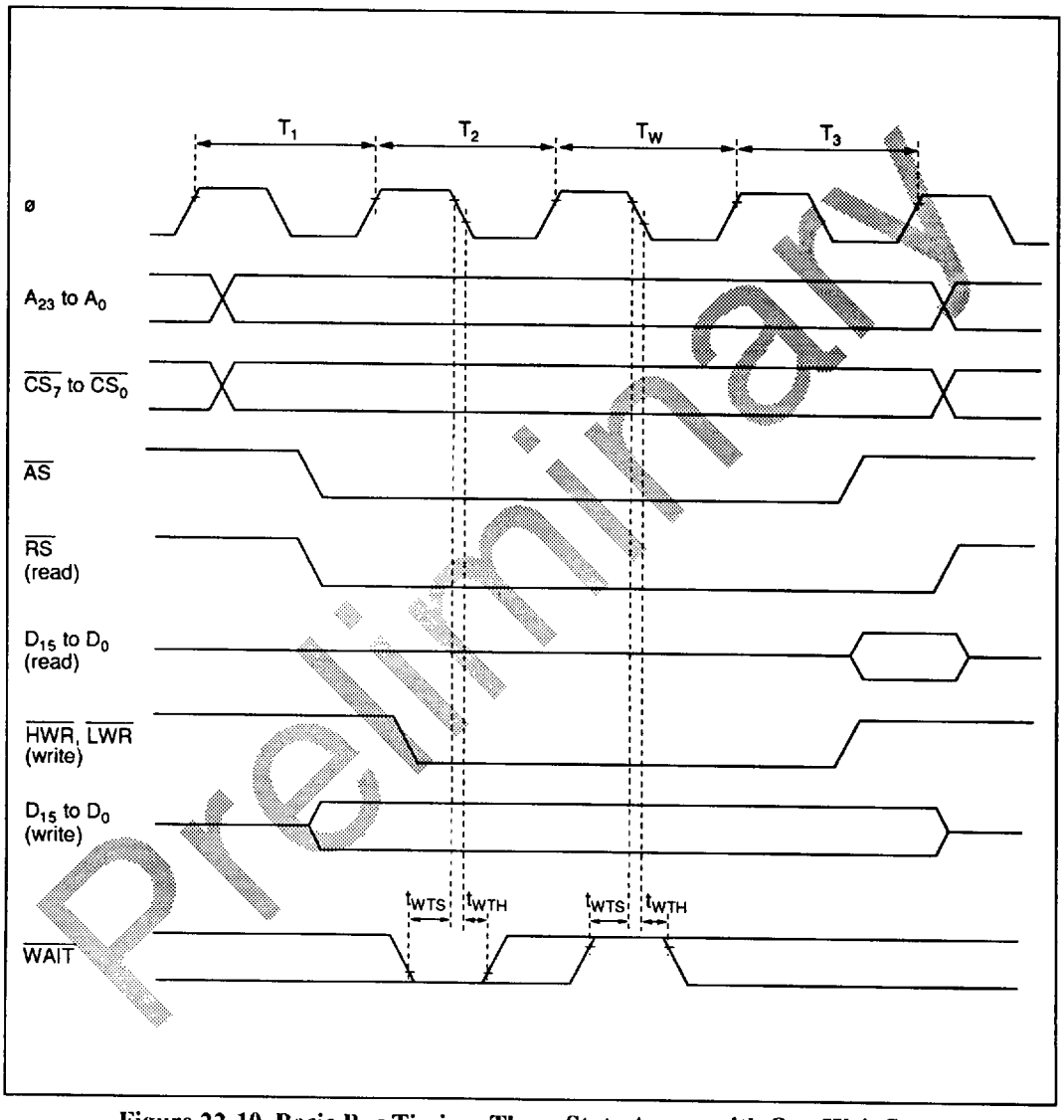

Figure 22-10 Basic Bus Timing: Three-State Access with One Wait State

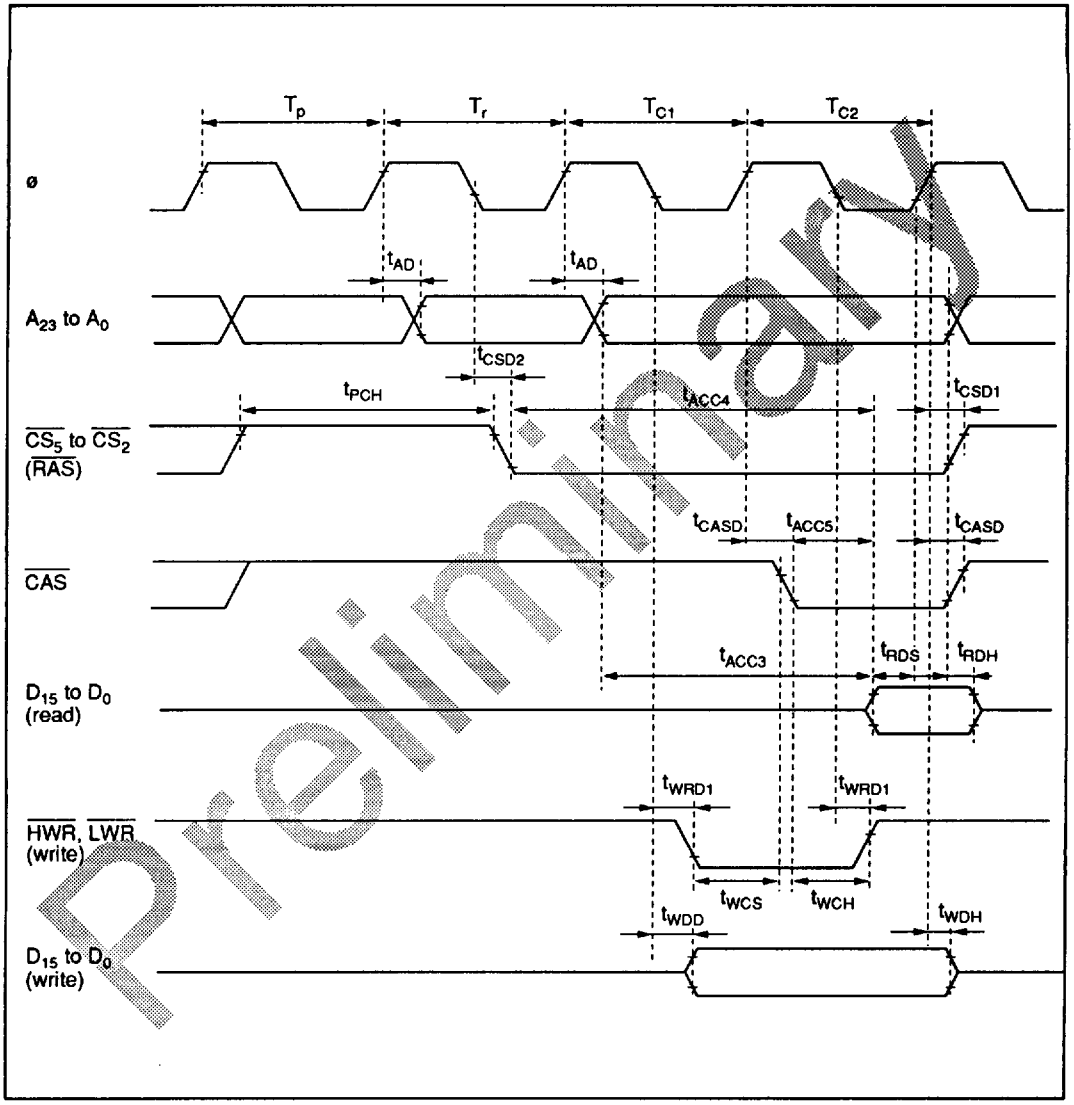

Figure 22-11 DRAM Bus Timing

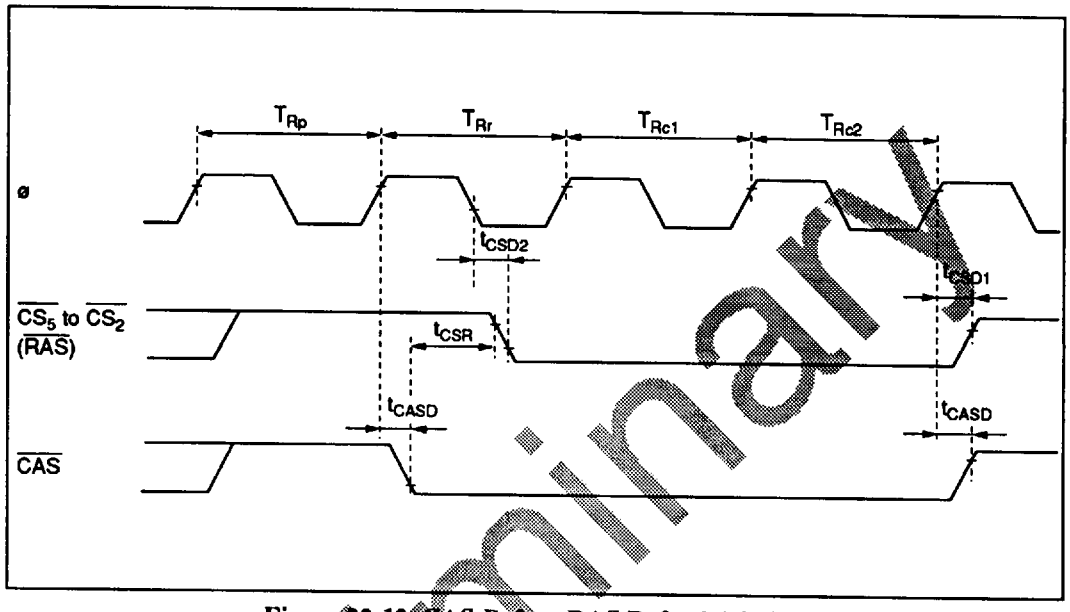

Figure 22-12 CAS-Before-RAS Refresh Timing

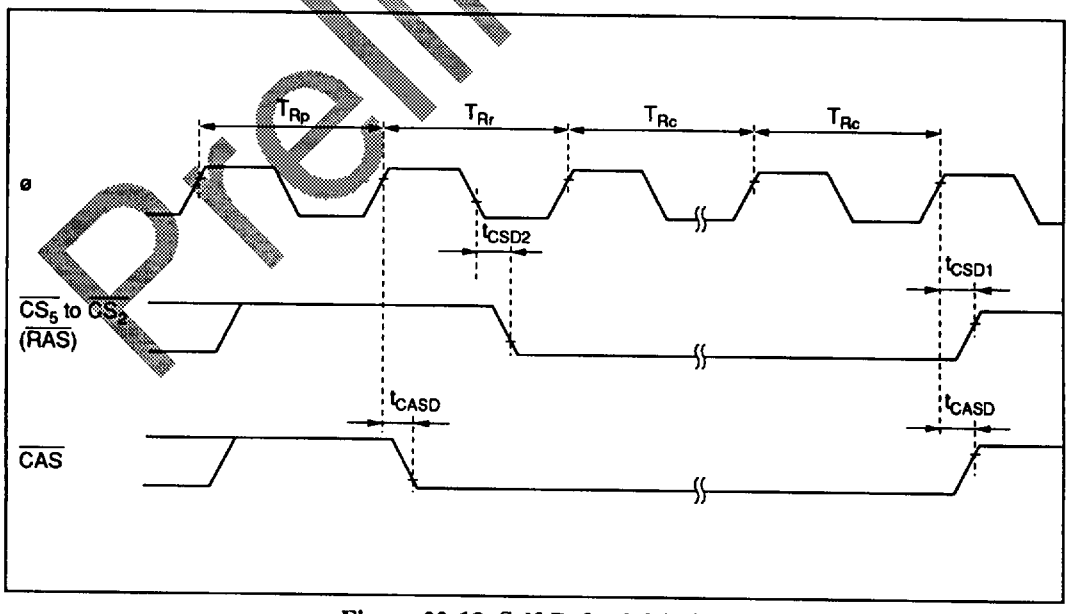

Figure 22-13 Self-Refresh Timing

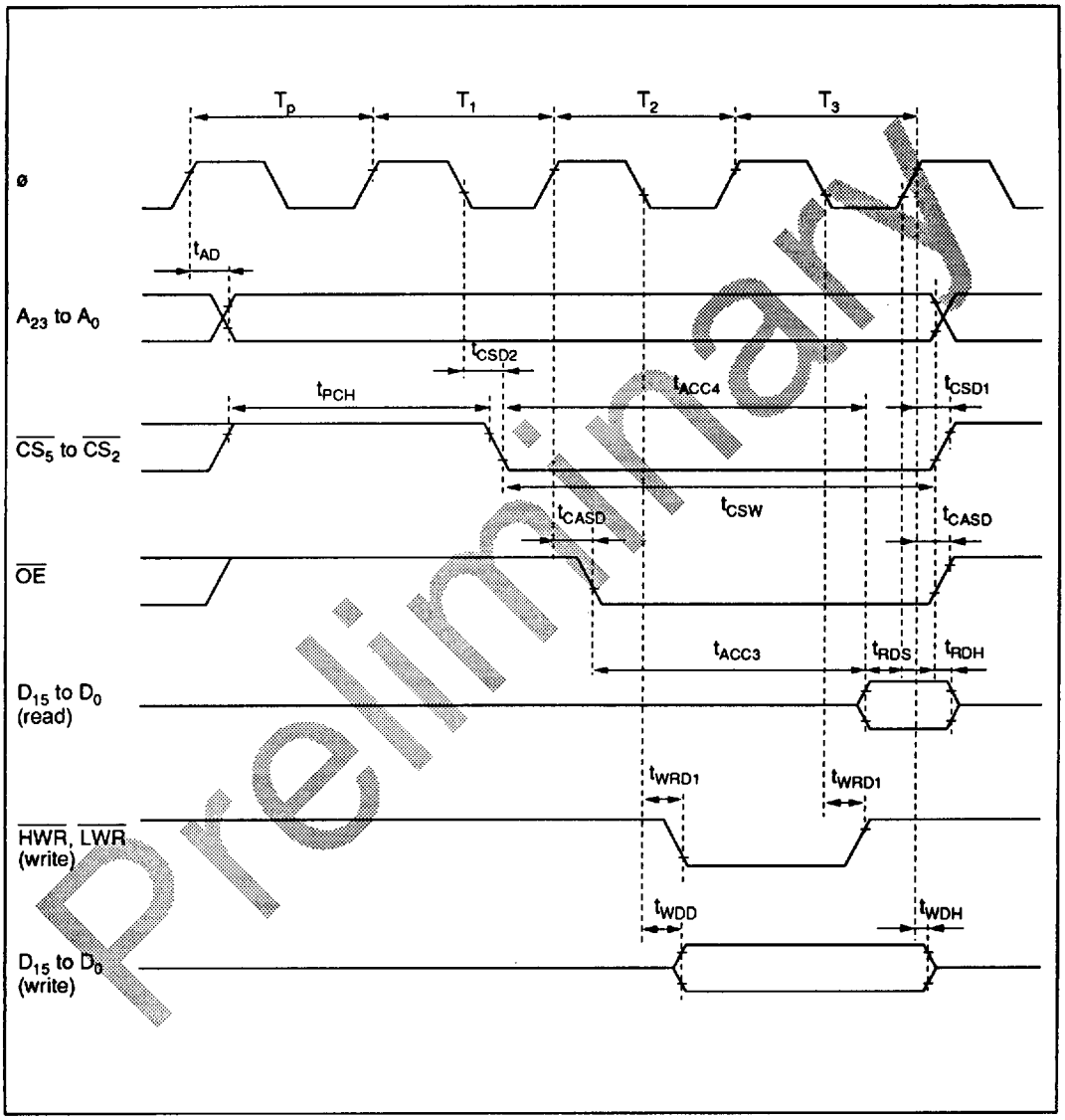

Figure 22-14 PSRAM Bus Timing

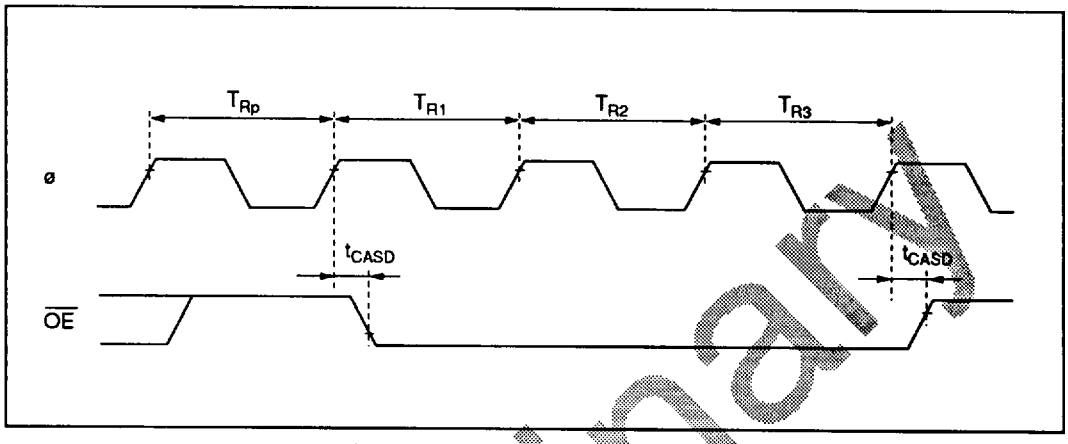

Figure 22-15 Auto Refresh Timing

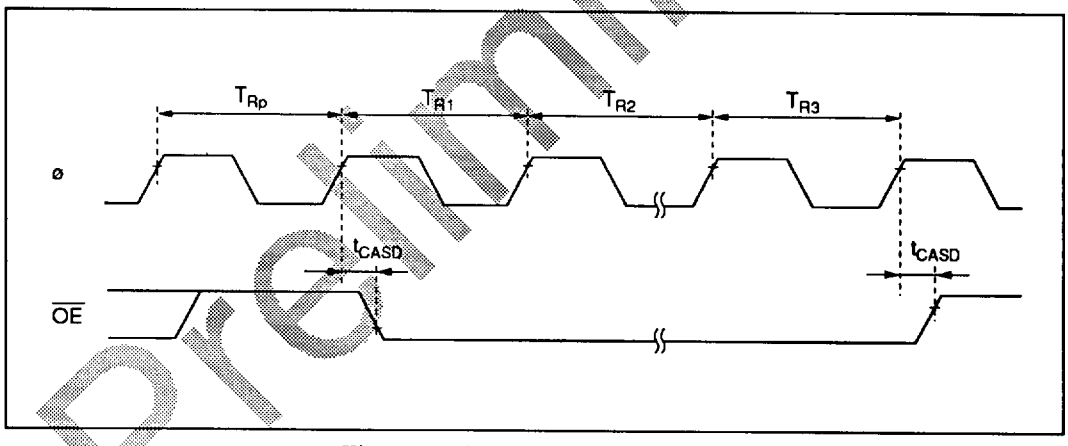

Figure 22-16 Self-Refresh Timing

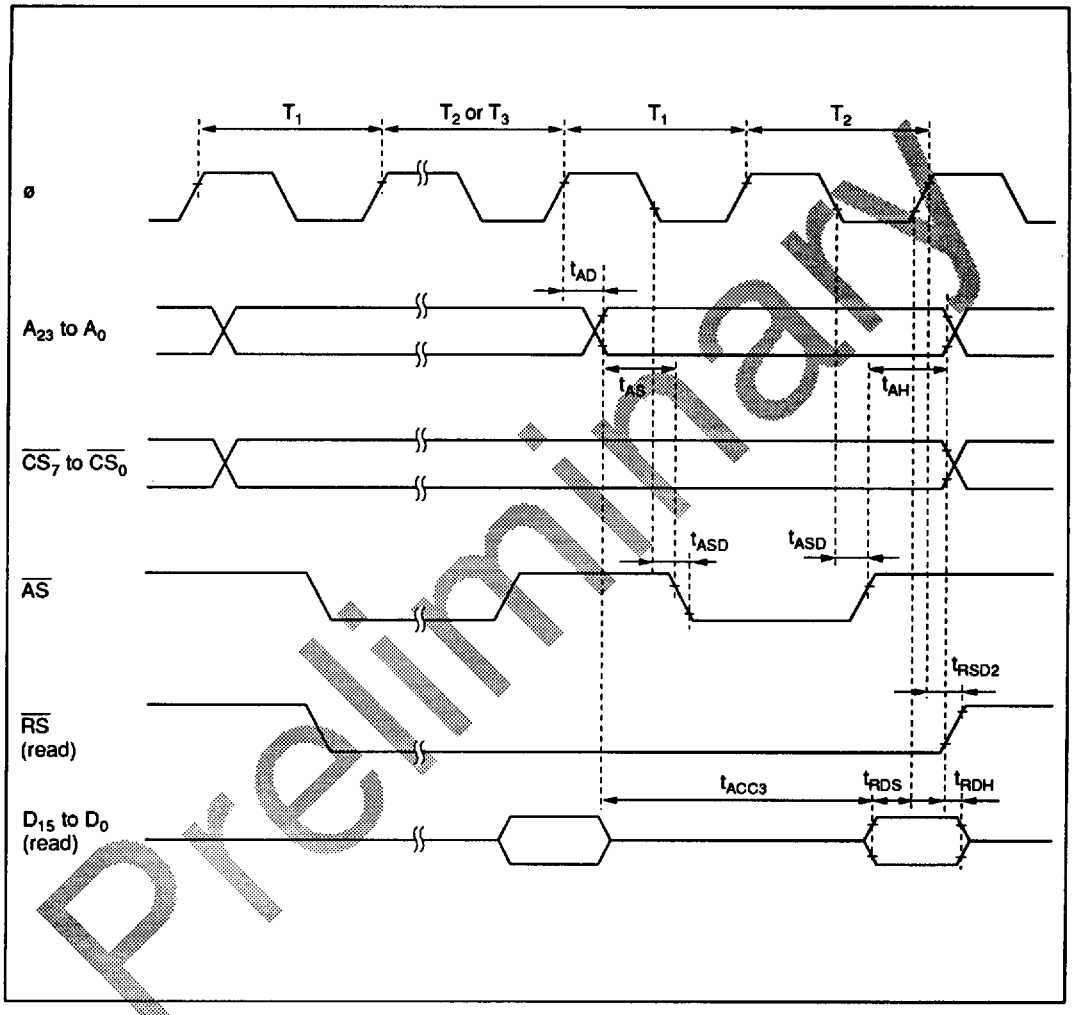

Figure 22-17 Burst ROM Access Timing: Two-State Access

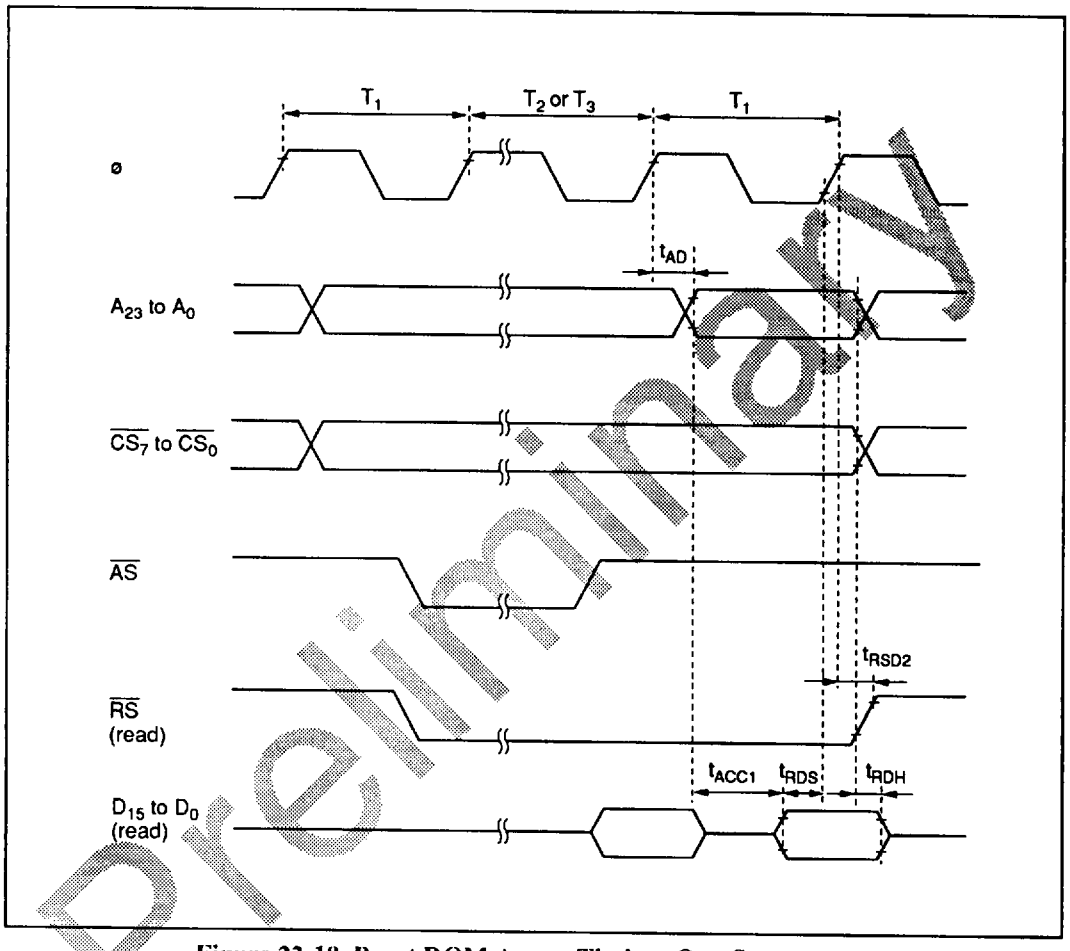

Figure 22-18 Burst ROM Access Timing: One-State Access

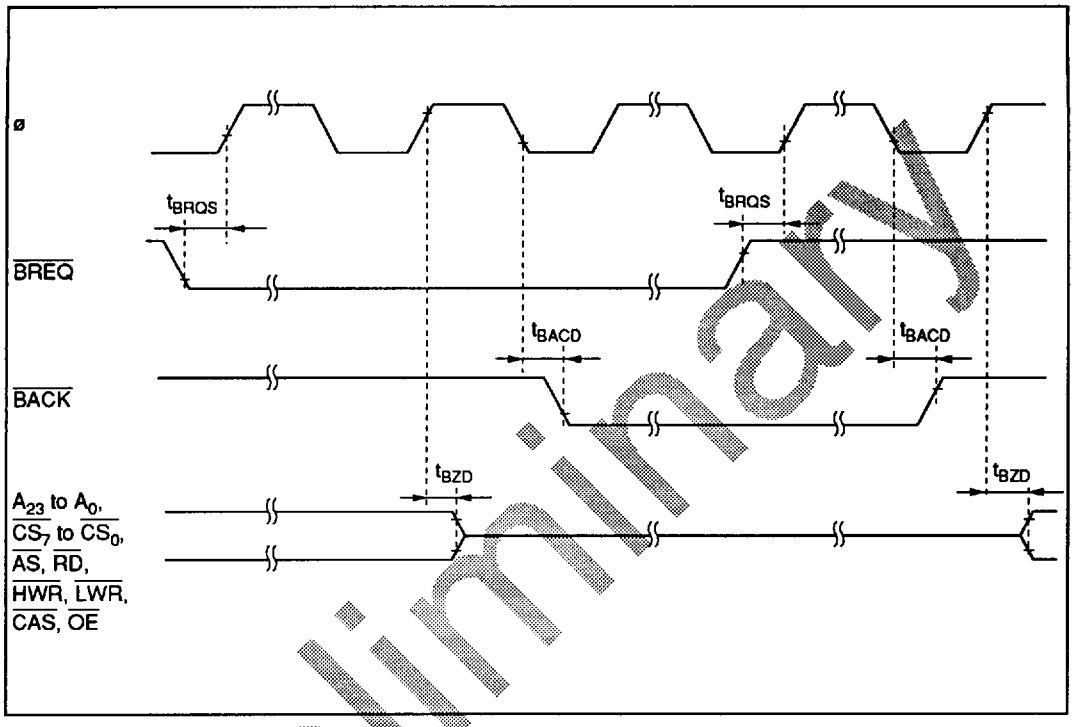

Figure 22-19 External Bus Release Timing

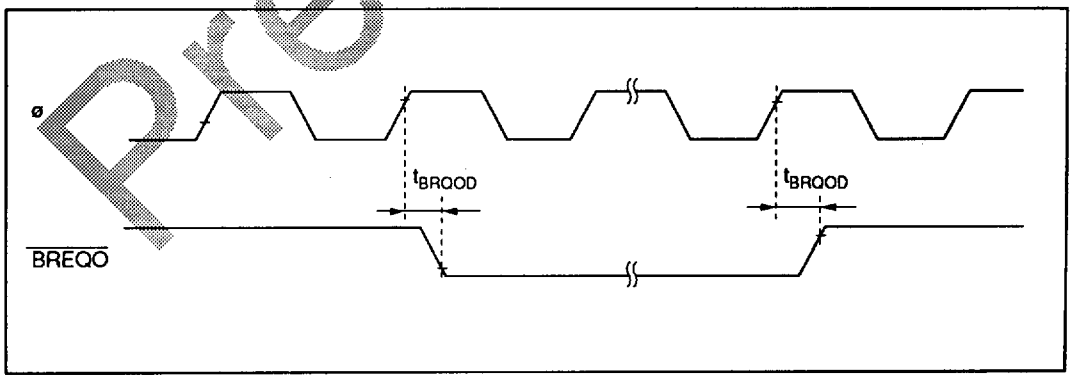

Figure 22-20 External Bus Request Output Timing

22.3.4 DMAC Timing

Table 22-7 lists the DMAC timing.

Table 22-7 DMAC Timing – Preliminary –

Condition A: $V_{CC} = AV_{CC} = 2.7$ V to 5.5 V, $V_{ref} = 2.7$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$V, ø = 2 to 10 MHz, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Condition B: $V_{CC} = AV_{CC} = 5.0$ V ± 10%, $V_{ref} = 4.5$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, ø = 2 to 20 MHz, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

		Condition A		Condition B			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
$\overline{\text{DREQ}}$ setup time	t_{DRQS}	40	—	30	—	ns	Figure 22-24
$\overline{\text{DREQ}}$ hold time	t_{DRQH}	10	—	10	—		
$\overline{\text{TEND}}$ delay time	t_{TED}	—	60	—	30		Figure 22-23
$\overline{\text{DACK}}$ delay time 1	t_{DACD1}	—	60	—	30	ns	Figure 22-21, Figure 22-22
$\overline{\text{DACK}}$ delay time 2	t_{DACD2}	—	60	—	30		

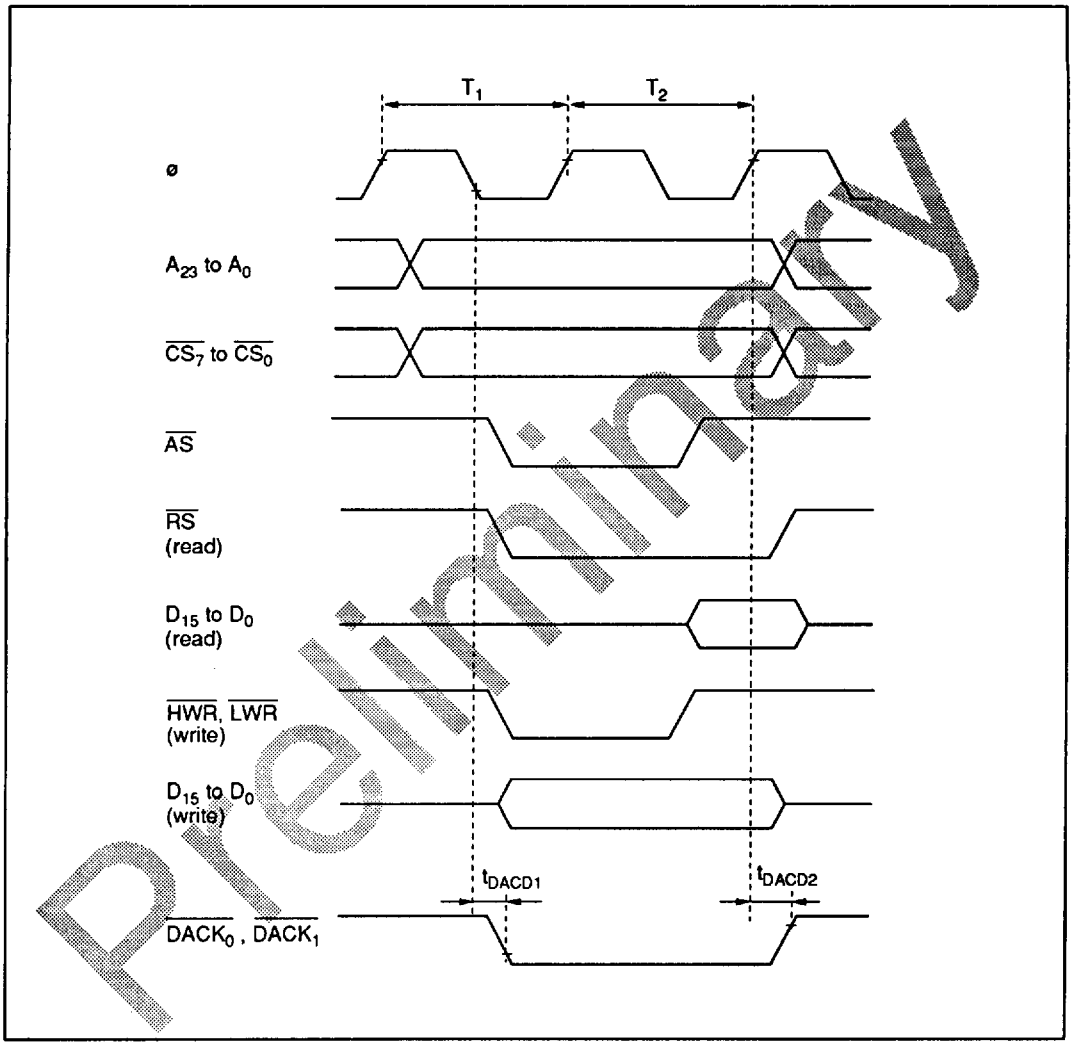

Figure 22-21 DMAC Single Address Transfer Timing: Two-State Access

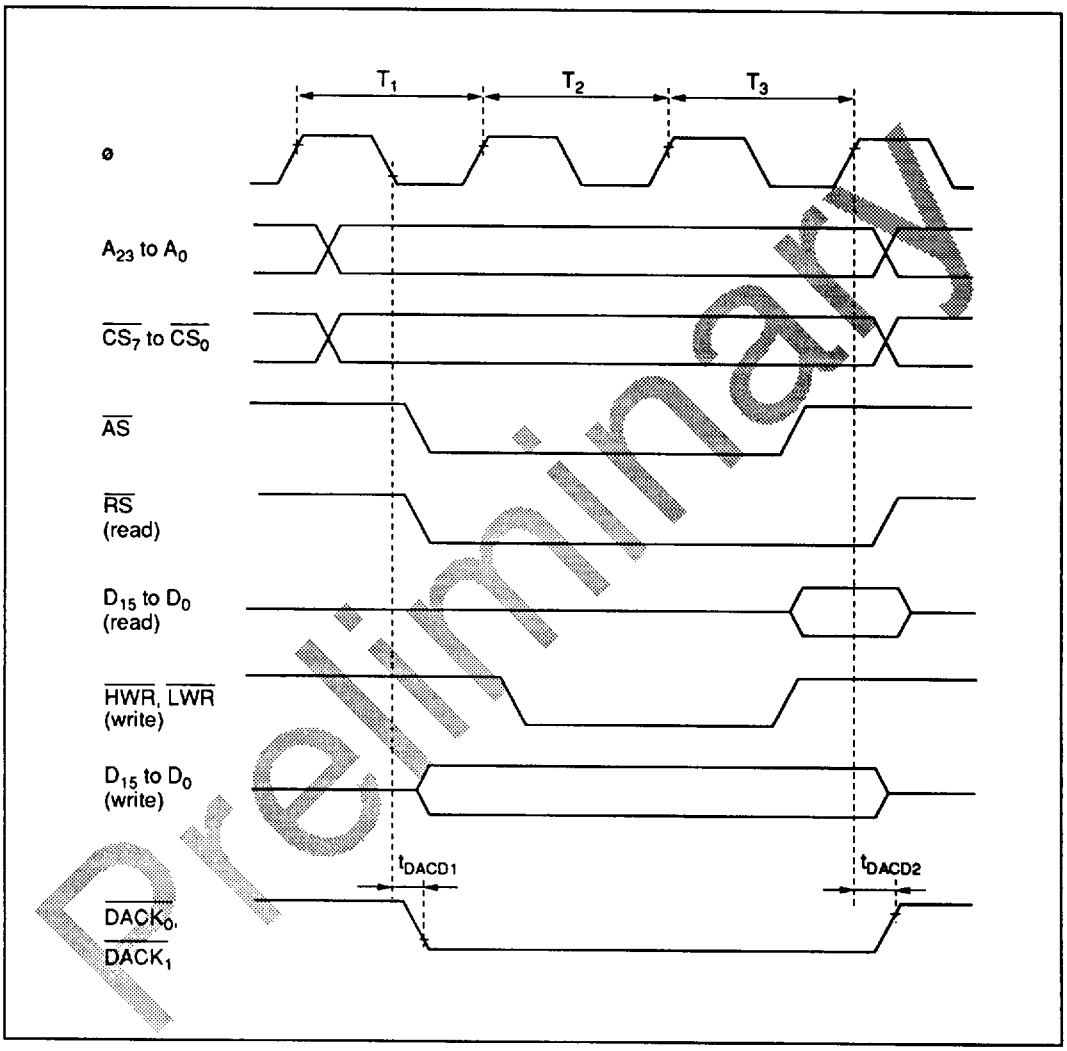

Figure 22-22 DMAC Single Address Transfer Timing: Three-State Access

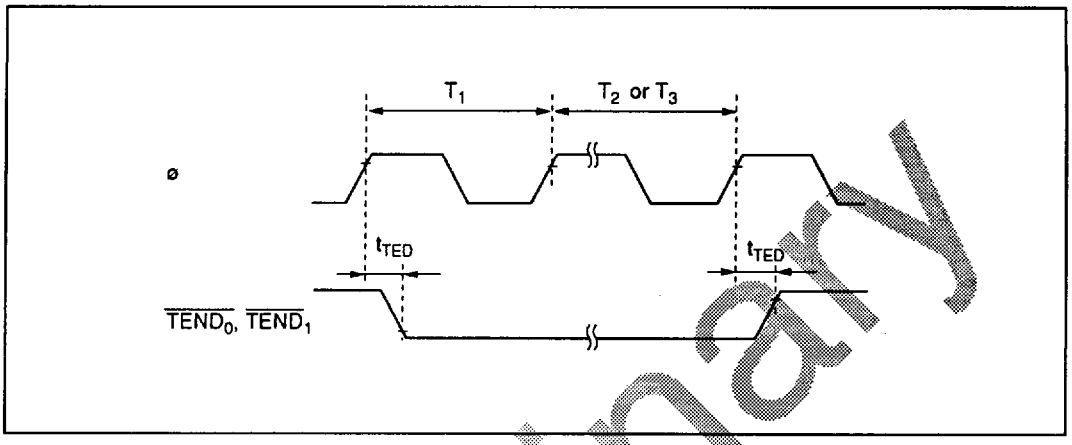

Figure 22-23 DMAC $\overline{\text{TEND}}$ Output Timing

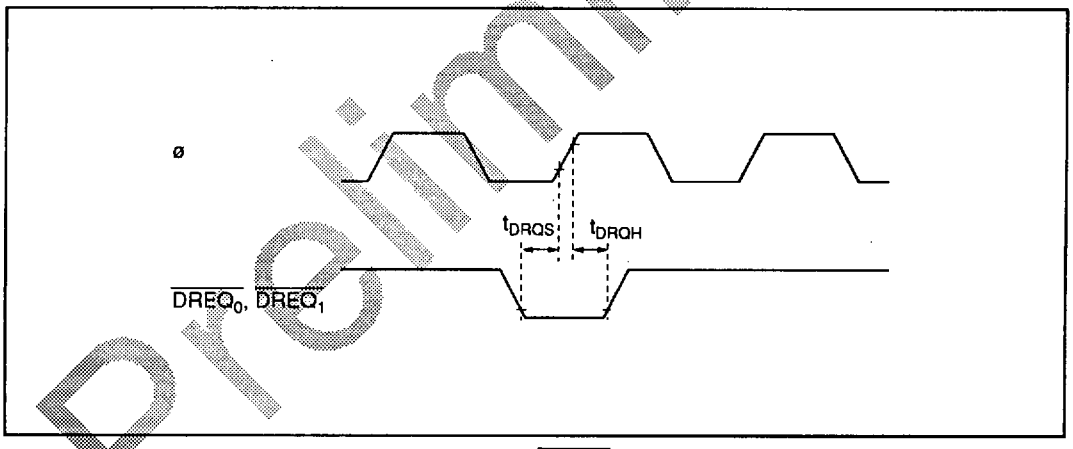

Figure 22-24 DMAC $\overline{\text{DREQ}}$ Intput Timing

22.3.5 Timing of On-Chip Supporting Modules

Table 22-8 lists the timing of on-chip supporting modules.

Table 22-8 Timing of On-Chip Supporting Modules – Preliminary –

Condition A: $V_{CC} = AV_{CC} = 2.7$ V to 5.5 V, $V_{ref} = 2.7$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, ø = 2 to 10 MHz, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Condition B: $V_{CC} = AV_{CC} = 5.0$ V ± 10%, $V_{ref} = 4.5$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, ø = 2 to 20 MHz, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

				Condition A		Condition B			
Item			**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
PORT	Output data delay time		t_{PWD}	—	100	—	50	ns	Figure 22-25
	Input data setup time		t_{PRS}	50	—	30	—		
	Input data hold time		t_{PRH}	50	—	30	—		
PPG	Pulse output delay time		t_{POD}	—	100	—	50	ns	Figure 22-26
TPU	Timer output delay time		t_{TOCD}	—	100	—	50	ns	Figure 22-27
	Timer input setup time		t_{TICS}	50	—	30	—		
	Timer clock input setup time		t_{TCKS}	50	—	30	—	ns	Figure 22-28
	Timer clock pulse width	Single edge	t_{TCKWH}	1.5	—	1.5	—	t_{cyc}	
		Both edges	t_{TCKWL}	2.5	—	2.5	—		
TMR	Timer output delay time		t_{TMOD}	—	100	—	50	ns	Figure 22-29
	Timer reset input setup time		t_{TMRS}	50	—	30	—	ns	Figure 22-31
	Timer clock input setup time		t_{TMCS}	50	—	30	—	ns	Figure 22-30

Table 22-8 Timing of On-Chip Supporting Modules (cont) – Preliminary –

Condition A: $V_{CC} = AV_{CC} = 2.7$ V to 5.5 V, $V_{ref} = 2.7$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, $\phi = 2$ to 10 MHz, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Condition B: $V_{CC} = AV_{CC} = 5.0$ V ± 10%, $V_{ref} = 4.5$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, $\phi = 2$ to 20 MHz, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Item			Symbol	Condition A Min	Condition A Max	Condition B Min	Condition B Max	Unit	Test Conditions
TMR	Timer clock pulse width	Single edge	t_{TMCWH}	1.5	—	1.5	—	t_{cyc}	Figure 22-30
		Both edges	t_{TMCWL}	2.5	—	2.5	—		
WDT	Overflow output delay time		t_{WOVD}	—	100	—	50	ns	Figure 22-32
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	4	—	t_{cyc}	Figure 22-33
		Synchronous		6	—	6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	1.5	—	1.5	t_{cyc}	
	Input clock fall time		t_{SCKf}	—	1.5	—	1.5		
	Transmit data delay time		t_{TXD}	—	100	—	50	ns	Figure 22-34
	Receive data setup time (synchronous)		t_{RXS}	100	—	50	—	ns	
	Receive data hold time (synchronous)		t_{RXH}	100	—	50	—	ns	
A/D converter	Trigger input setup time		t_{RGS}	50	—	30	—	t_{ns}	Figure 22-35

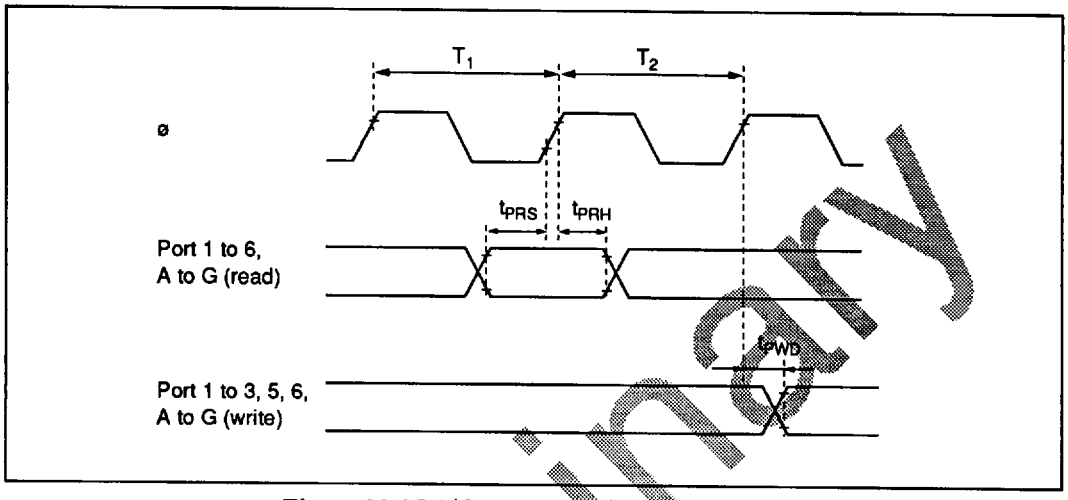

Figure 22-25 I/O Port Input/Output Timing

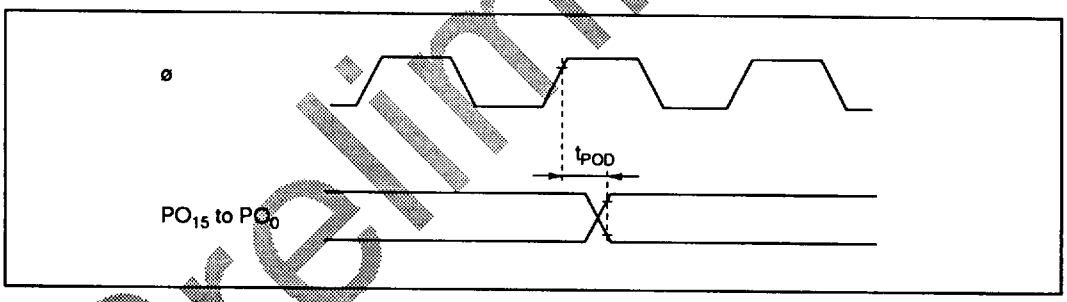

Figure 22-26 PPG Output Timing

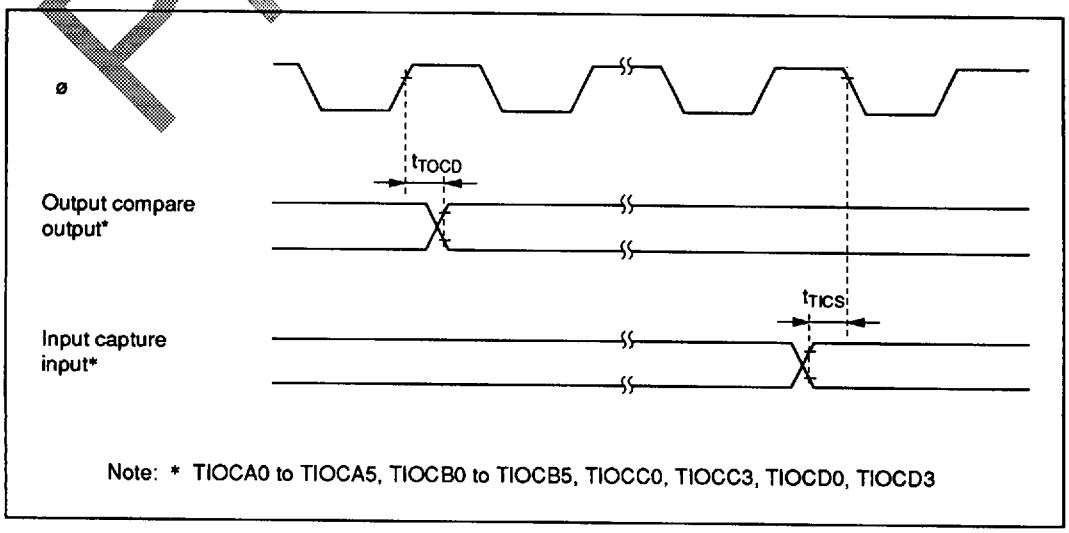

Figure 22-27 TPU Input/Output Timing

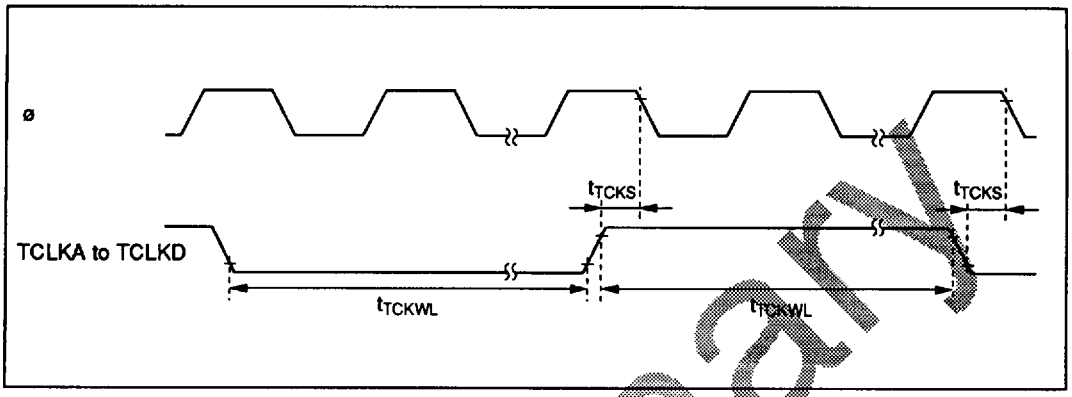

Figure 22-28 TPU Clock Input Timing

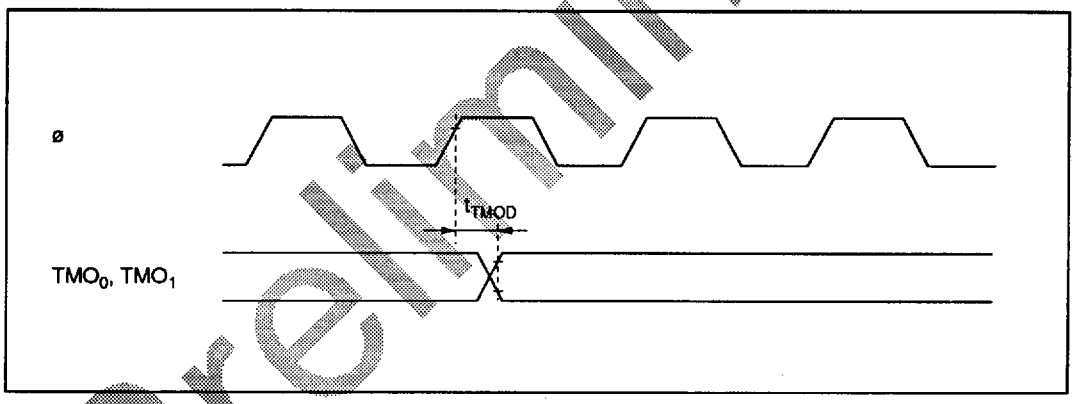

Figure 22-29 8-Bit Timer Output Timing

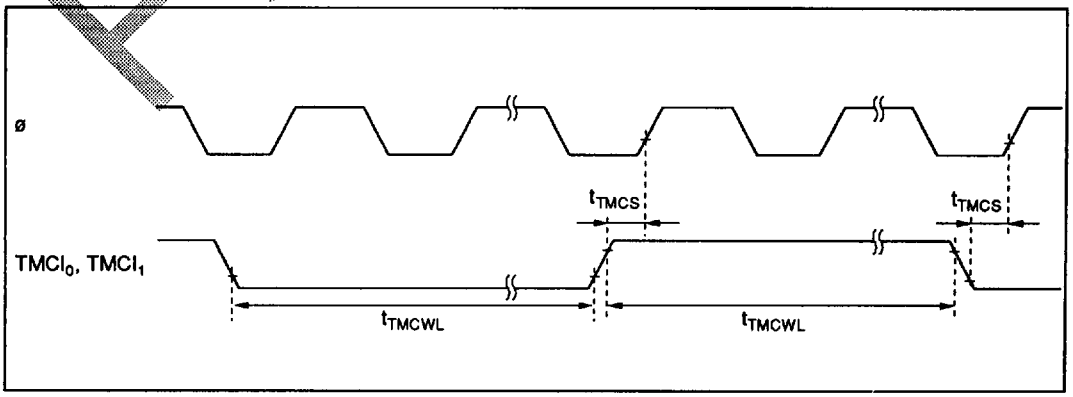

Figure 22-30 8-Bit Timer Clock Input Timing

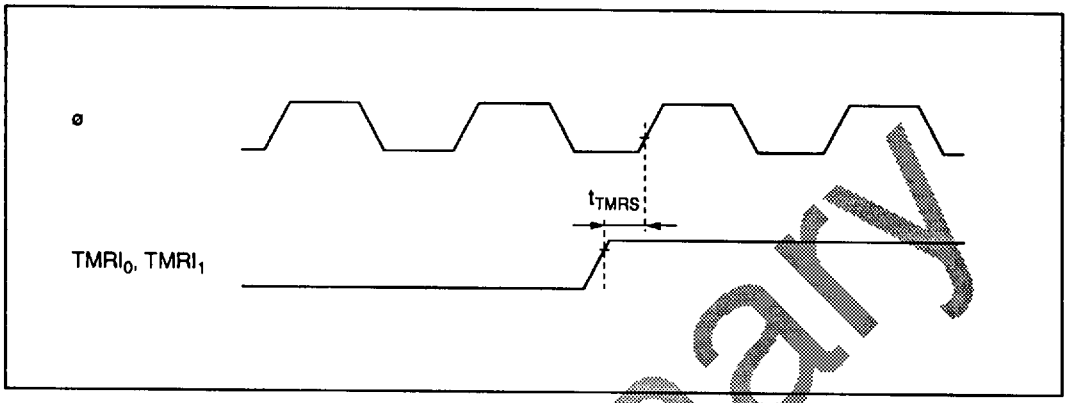

Figure 22-31 8-Bit Timer Reset Input Timing

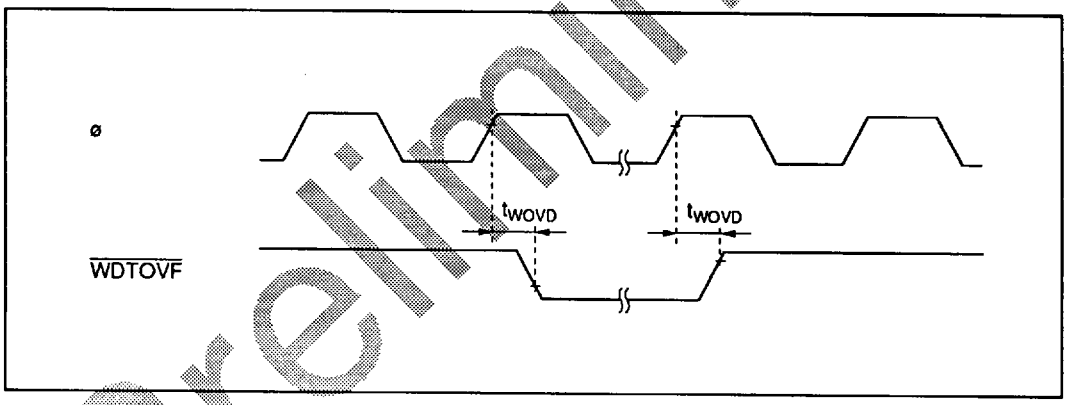

Figure 22-32 WDT Output Timing

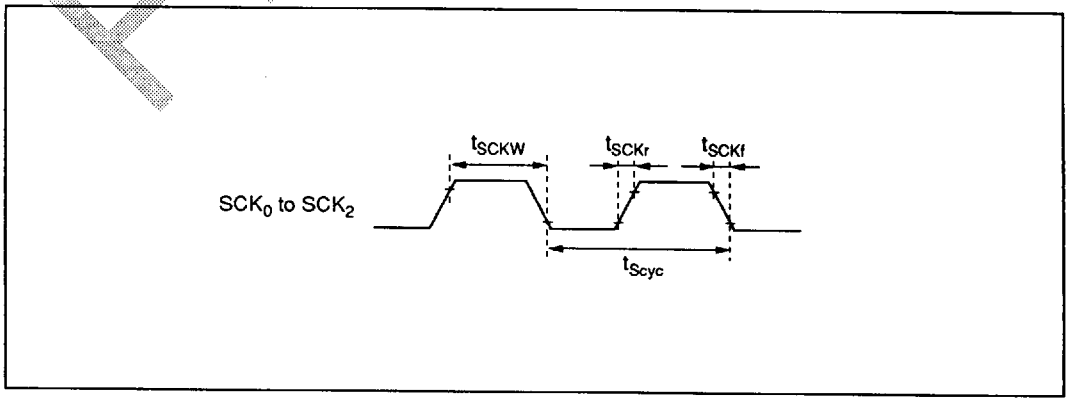

Figure 22-33 SCK Clock Input Timing

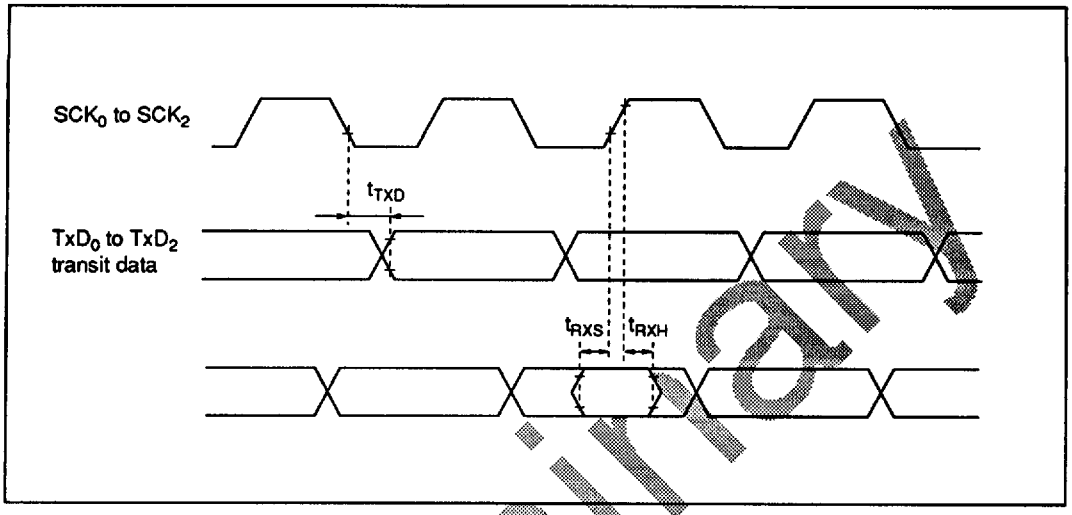

Figure 22-34 SCI Input/Output Timing Synchronous Mode

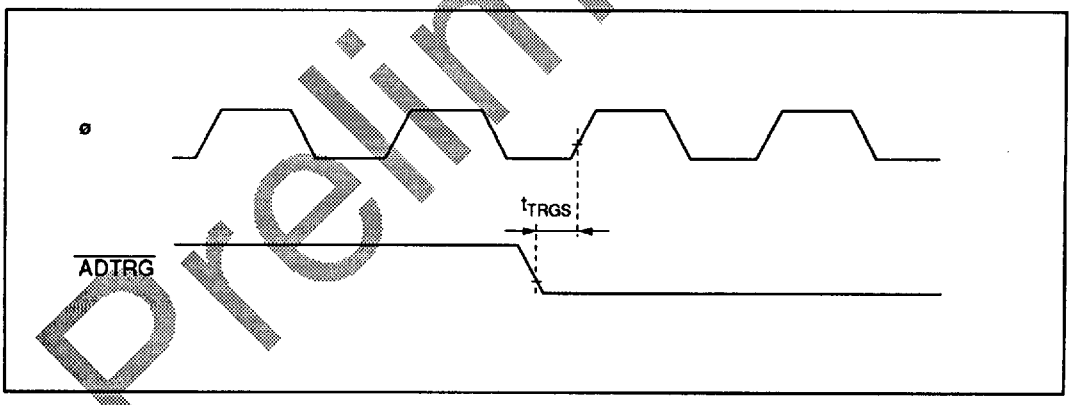

Figure 22-35 A/D Converter External Trigger Input Timing

22.4 A/D Conversion Characteristics

Table 22-9 lists the A/D conversion characteristics.

Table 22.9 A/D Conversion Characteristics – Preliminary –

Condition A: $V_{CC} = AV_{CC} = 2.7$ V to 5.5 V, $V_{ref} = 2.7$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, ø = 2 to 10 MHz, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Condition B: $V_{CC} = AV_{CC} = 5.0$ V ± 10%, $V_{ref} = 4.5$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, ø = 2 to 20 MHz, $T_a = -20$ to +75°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

	Condition A			Condition B			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	bits
Conversion time	—	—	TBD	—	—	TBD	µs
Analog input capacitance	—	—	TBD	—	—	TBD	pF
Permissible signal-source impedance	—	—	TBD	—	—	TBD	kΩ
	—	—	TBD	—	—	TBD	
Nonlinearity error	—	—	TBD	—	—	TBD	LSB
Offset error	—	—	TBD	—	—	TBD	LSB
Full-scale error	—	—	TBD	—	—	TBD	LSB
Quantization	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	TBD	—	—	TBD	LSB