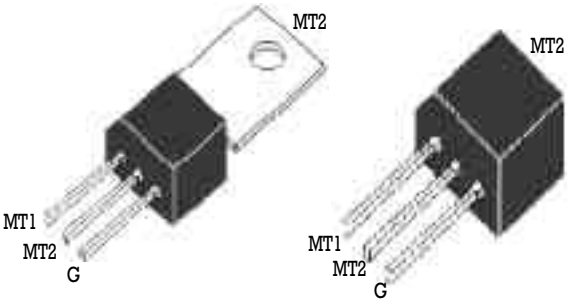
# LOGIC LEVEL TRIAC

TO202-1 (E) TO202-3 (F)




**On-State Current**
4 Amp

**Gate Trigger Current**
< 5 mA to < 10 mA

**Off-State Voltage**
200 V ÷ 600 V

This series of **TRIAC**s uses a high performance PNPN technology.

These parts are intended for general purpose AC switching applications with highly inductive loads.

## Absolute Maximum Ratings, according to IEC publication No. 134

| SYMBOL | PARAMETER | CONDITIONS | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{T(RMS)}$ | RMS On-state Current | All Conduction Angle, $T_c$ = 110 °C | 4 | | A |
| $I_{TSM}$ | Non-repetitive On-State Current | Half Cycle, 60 Hz | 21 | | A |
| $I_{TSM}$ | Non-repetitive On-State Current | Half Cycle, 50 Hz | 20 | | A |
| $I^2t$ | Fusing Current | $t_p$ = 10 ms, Half Cycle | 2.2 | | $A^2s$ |
| $I_{GM}$ | Peak Gate Current | 20 µs max. | | 1.2 | A |
| $P_{GM}$ | Peak Gate Dissipation | 20 µs max. | | 2 | W |
| $P_{G(AV)}$ | Gate Dissipation | 20 ms max. | | 0.2 | W |
| di/dt | Critical rate of rise of on-state current | $I_G$ = 2 x $I_{GT}$ Tr ≤ 200 ns, F = 120 Hz $T_j$ = 125 °C | 20 | | A/µs |
| $T_j$ | Operating Temperature | | -40 | +125 | °C |
| $T_{stg}$ | Storage Temperature | | -40 | +150 | °C |
| $T_{sld}$ | Soldering Temperature | 1.6 mm from case, 10s max. | | 260 | °C |

| SYMBOL | PARAMETER | CONDITIONS | VOLTAGE | | | Unit |
|---|---|---|---|---|---|---|
| | | | B | D | M | |
| $V_{DRM}$ $V_{RRM}$ | Repetitive Peak Off State Voltage | $R_{GK}$ = 1 KΩ | 200 | 400 | 600 | V |

# LOGIC LEVEL TRIAC

## Electrical Characteristics

| SYMBOL | PARAMETER | CONDITIONS | Quadrant | | SENSITIVITY | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | 05 | 09 | |
| $I_{GT}$ | Gate Trigger Current | $V_D$ = 12 $V_{DC}$ , $R_L$ = 30Ω, $T_j$ = 25 °C | Q1÷Q3 | MAX | 5 | 10 | mA |
| | | | Q4 | MAX | 5 | 10 | mA |
| $I_{DRM}$ /$I_{RRM}$ | Off-State Leakage Current | $V_D$ = $V_{DRM}$ , $T_j$ = 125 °C | | MAX | 0.5 | | mA |
| | | $V_R$ = $V_{RRM}$ , $T_j$ = 25 °C | | MAX | 5 | | µA |
| $V_{to}$ | Threshold Voltage | $T_j$ = 125 °C | | MAX | 0.95 | | V |
| $R_d$ | Dynamic Resistance | $T_j$ = 125 °C | | MAX | 180 | | mΩ |
| $V_{TM}$ * | On-state Voltage | $I_T$ = 5.5 Amp, tp = 380 µs, $T_j$ = 25 °C | | MAX | 2 | | V |
| $V_{GT}$ | Gate Trigger Voltage | $V_D$ = 12 $V_{DC}$ , $R_L$ = 30Ω, $T_j$ = 25 °C | Q1÷Q4 | MAX | 1.3 | | V |
| $V_{GD}$ | Gate Non Trigger Voltage | $V_D$ = $V_{DRM}$ , $R_L$ = 3.3KΩ, $T_j$ = 125 °C | Q1÷Q4 | MIN | 0.2 | | V |
| $I_H$* | Holding Current | $I_T$ = 50 mA $T_j$ = 25 °C | | MAX | 7 | 10 | mA |
| $I_L$ | Latching Current | $I_G$ = 1.2 $I_{GT}$, $T_j$ = 25 °C | Q1,Q3,Q4 | MAX | 10 | 15 | mA |
| | | | Q2 | MAX | 15 | 25 | |
| dv / dt* | Critical Rate of Voltage Rise | $V_D$ = 0.67 x $V_{DRM}$ , Gate open $T_j$ = 125 °C | | MIN | 20 | 100 | V/µs |
| (dv/dt)c* | Critidal rise rate of commutating off-state Voltage | (di/dt)c= 1.8 A/ms $T_j$ = 110 °C | | MIN | 1 | 2 | V/µs |
| $R_{th(j-l)}$ | Thermal Resistance Junction-Leads for AC | | | | 15 | | °C/W |
| $R_{th(j-a)}$ | Thermal Resistance Junction-Ambient | | | | 100 | | °C/W |

(*) For either polarity of electrode MT2 voltage with reference to electrode MT1.

## PART NUMBER INFORMATION

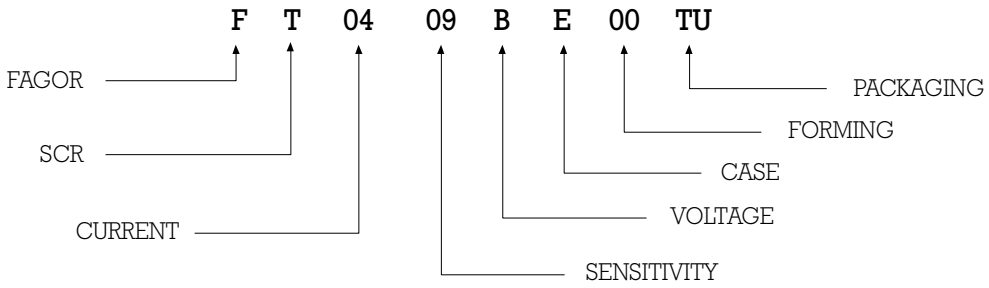


Fig. 1: Maximum average power disipation versus RMS on-state current (full cycle)

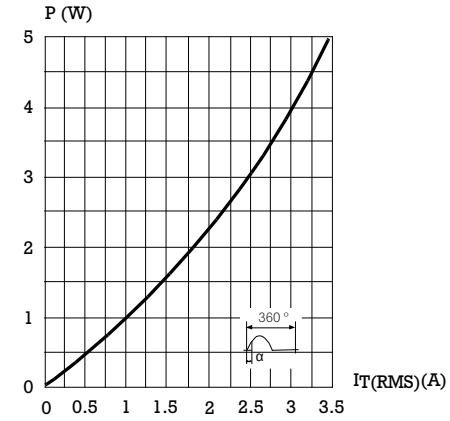



Fig. 2: RMS on-state current versus ambient temperature (full cycle)

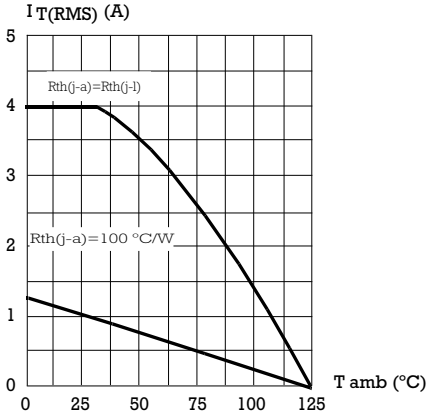



Fig. 3: Relative variation of thermal impedance junction to ambient versus pulse duration.

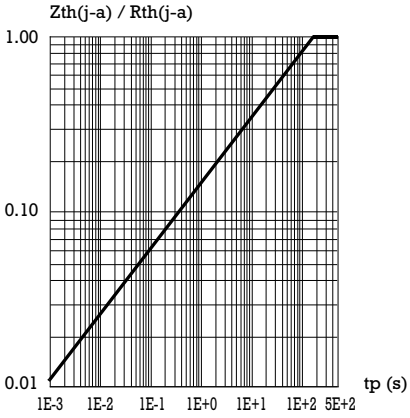



Fig. 4: Relative variation of gate trigger current, holding and latching current versus junction temperature.

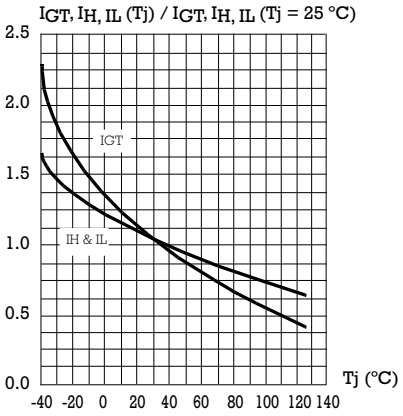



Fig. 5: Non repetitive surge peak on-state current versus number of cycles.

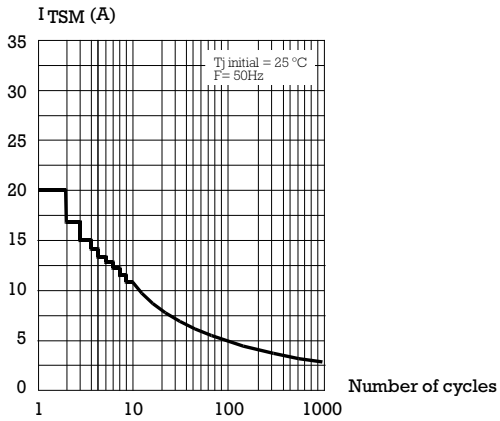



Fig. 6: Non repetitive surge peak on-state current for a sinusoidal pulse with width: tp ≤ 10 ms, and corresponding value of $I^2t$.

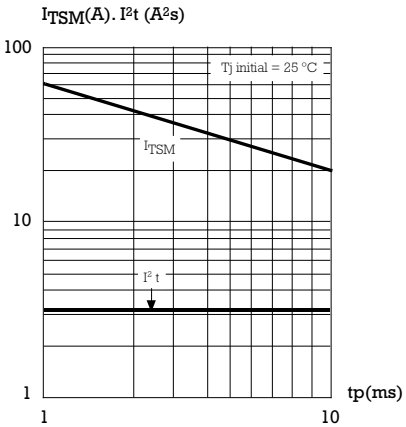
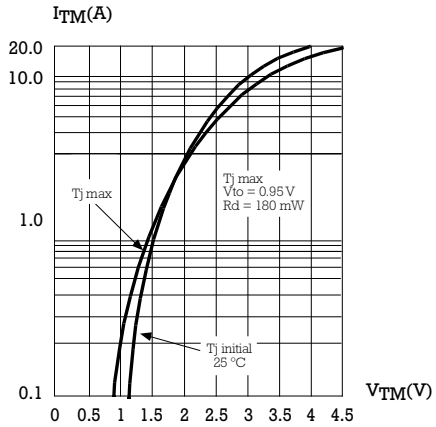
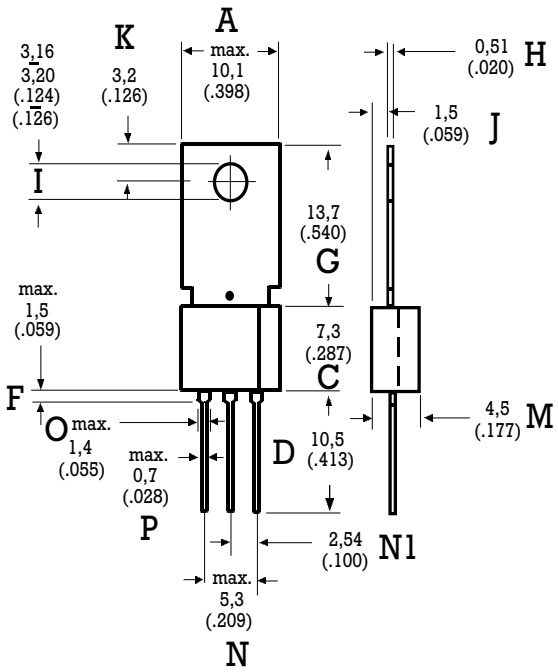


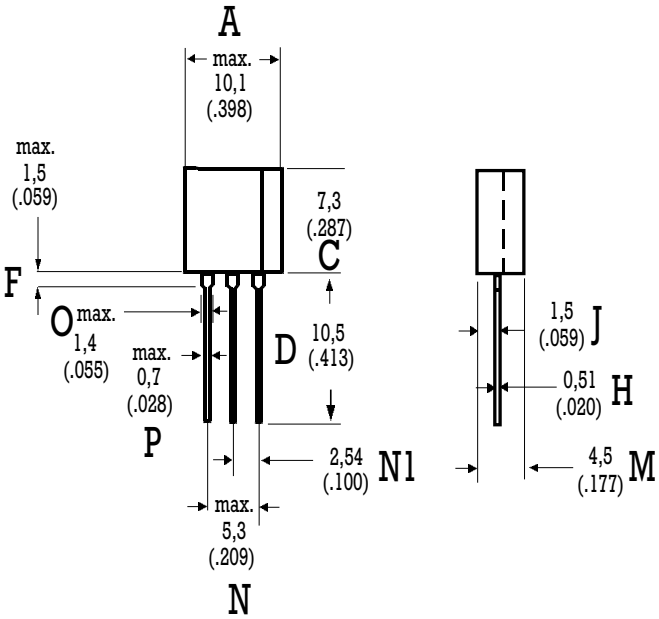
Fig. 7: On-state characteristics (maximum values)




## PACKAGE MECHANICAL DATA TO 202-1 TO 202-3

### TO 202-1




### TO 202-3