128Kx32 CMOS EEPROM Multi-Chip Module

Features

128Kx32 bit CMOS

Electrically Eraseable Programmable Read Only Memory

- Access Times: 120, 150, and 200ns
- Individual Byte Selects
- Output Enable Function
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

68 lead PLCC package No. 99

- Multiple Ground Pins for Maximum Noise Immunity

Single +5V (±10%) Supply Operation

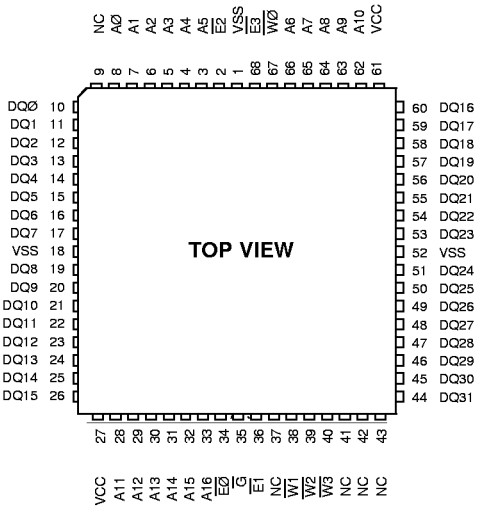
The EDI5LM32128C is a high performance, four megabit density EEPROM organized as 128Kx32 bits. The device has four 128Kx8 EEPROMs mounted in a 68 J-lead plastic package.

Four Chip Enables are provided to independently enable each of the four bytes. Reading or writing can be executed on an individual byte or any combination of bytes through proper use of the chip or write enables.

Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

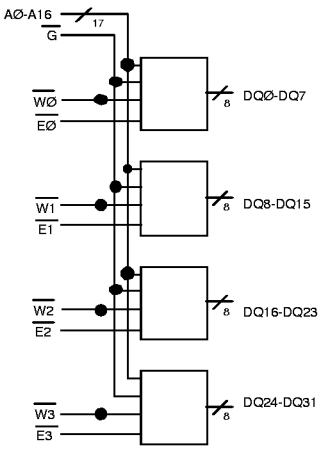
The 68 lead J-lead package enables 4 megabits of memory to be placed in less than 0.96 square inches of space.

Pin Configurations and Block Diagram



Pin Names

AØ-A16	Address Inputs
$\overline{EØ}$-$\overline{E3}$	Chip Enables
$\overline{WØ}$-$\overline{W3}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ31	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



Device Operation

This wide word multi chip module is a byte oriented device. All software commands are loaded on a byte specific basis. DQ0-DQ7, DQ8-DQ15, DQ16-DQ23, and DQ24-DQ31 are the bytes requiring command input for device mode selection. To select the same operating mode for all bytes the byte commands must be repeated for each individual byte. This may be done in parallel. All references to software commands in this specification will refer to byte commands. These may be repeated for each byte in the module data word as required for the desired operating mode.

Read:

The EDI5LM32128C is accessed like an SRAM. When E\ and G\ are low and W\ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever the E\ or G\ is high. This dual line control give designers flexibility in preventing bus contention.

Byte Write:

A byte write is performed by applying a low pulse on the W\ or E\ input with E\ or W\ low (respectively) and G\ high. The address is latched on the falling edge of E\ or W\, whichever occurs last. The data is latched by the first rising edge of E\ or W\. Once a byte write has been started, it will automatically time itself to completion.

Page Write:

The page write operation of the EDI5LM32128C allows one to one hundred twenty-eight bytes of data to be written into the device during a single internal programming period. Page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by one to one hundred twenty seven additional bytes. Each successive byte must be written within 150µs (TBLC) of the previous byte. If the TBLC limit is exceeded the EDI5C32128C will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A7-A16 inputs. For each W\ high to low transition during the page write operation, A7-A16 must be the same.

The AØ to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

Data\ Polling:

The EDI5LM32128C features DATA\ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on DQ7, DQ15, DQ23 or DQ31. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. DATA\ Polling may begin at any time during the program cycle.

Toggle Bit:

In addition to DATA\ Polling the EDI5LM32128C provides another method for determining the end of a write cycle. During a write cycle, successive attempts to read data from the device will result in DQ6, DQ14, DQ22 or DQ 30 toggling between one and zero. Once the write cycle has been completed, DQ6, DQ14, DQ22 or DQ 30 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a write cycle.

Hardware Data Protection:

Hardware features protect against inadvertent writes to the EDI5LM32128C in the following ways:

a] VCC Sense – if VCC is below 3.8V (typical), the write function is inhibited.

b] VCC Power on delay – once VCC has reached the 3.8V, the device will automatically time out 5ms (typical) before allowing a write.

c] Write inhibit – holding G\ low, E\ high or W\ high inhibits program cycles.

d] Noise filter – pulses of less than 15ns (typical) on the W\ or E\ inputs will not initiate a write cycle.

Software Data Protection:

A software controlled data protection feature is available on the EDI5LM32128C. Once the software protection is enabled a software algorithm must be issued to the device before a write may be performed. The software protection feature may be enabled or disabled by the user; when shipped, the software data protection feature is disabled. To enable the software data protection, a series of three write commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three write commands must begin each write cycle in order for the writes to occur. All software write commands must obey the page program timing specifications. Once set, the software data protection feature remains active unless the disable commands are issued. Power transitions will not reset the software data protection feature. However, the software feature will guard against inadvertent program cycles during power transitions.

Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.6V to +6.25V
Operating Temperature TA (Ambient)	
Commercial	0 ℃ to +70 ℃
Industrial	-40 ℃ to +85 ℃
Military	-55 ℃ to +125 ℃
Storage Temperature	-55 ℃ to +125 ℃
Power Dissipation	1.5 Watts
Output Current.	40 mA
Junction Temperature, TJ	150 ℃

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.0	--		V
Input Low Voltage	VIL	--	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

(note: For TEHQZ,TGHQZ and TWLQZ, Figure 2)

Figure 1

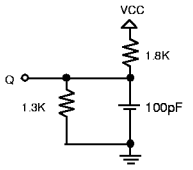
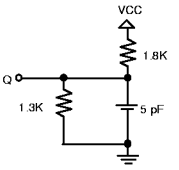


Figure 2



DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ	Max	Units
Operating Power Supply Current – x32	ICC1	$\overline{W}$= VIL, II/O = 0mA (4) $\overline{E}$ = VIL, f = 5MHz			250	mA
Operating Power Supply Current – x16	ICC1	$\overline{W}$ = VIL, II/O = 0mA (2) $\overline{E}$ = VIL, (2) $\overline{E}$ ≥VCC -0.2V, f = 5MHz			150	mA
Operating Power Supply Current – x8	ICC1	$\overline{W}$ = VIL, II/O = 0mA (1) $\overline{E}$ = VIL, (3) $\overline{E}$≥VCC-0.2V, f = 5MHz			100	mA
Standby (TTL) Power Supply Current	ICC2	(All) $\overline{E}$ ≥VIH to VCC			12	mA
Full Standby Power Supply Current	ICC3	(All) $\overline{E}$ ≥VCC-0.2V VIN ≥VCC-0.2V or VIN ≤0.2V			1.5	mA
Input Leakage Current	ILI	VIN = 0V to VCC	-10	--	10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC	-10	--	10	µA
Output High Volltage	VOH	IOH = -400µA	2.4			V
Output Low Voltage	VOL	IOL = 2.1mA			0.45	V

Truth Table

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Address	I/O
VIL	VIL	VIH	Read	A	DOUT
VIL	VIH	VIL	PRGM (1)	A	DIN
VIH	X	X	Standby	X	High Z
X	X	VIH	WRITE INHIB		
X	VIL	X	WRITE INHIB		
X	VIH	X	Output Disable		High Z

Notes: 1. Refer to AC Program Waveform

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	50	pF
Data Lines	CD/Q	20	pF
Chip & Write EnableLines $\overline{E}$, $\overline{W}$		20	pF
Output EnableLine	$\overline{G}$	50	pF

These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

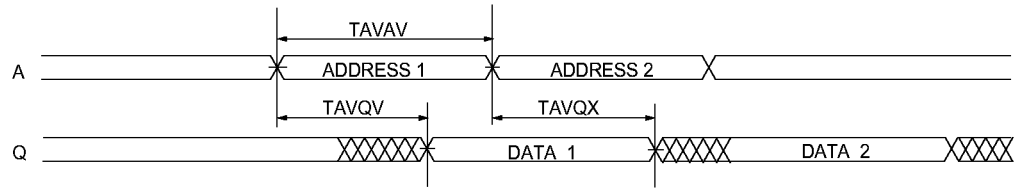
	Symbol		120ns		150ns		200ns			
Parameter	**JEDEC**	**Alt**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Address to Output Delay	TAVQV	TAA, TACC		120		150		200	ns	
Chip Enable to Output Delay	TELQV	TACS, TCE		120		150		200	ns	
Chip Enable or Output Enable	TEHQZ									
to Output Float	TGHQZ	TCHZ, TDF		50		55		55	ns	2, 3
Output Hold from Address,	TAXQX									
Output Enable or Chip Enable,	TEHQX									
whichever comes first	TGHQX	TOH	0		0		0		ns	
Output Enable to Output Delay	TGLQV	TOE	0	50	0	55	0	55	ns	1
Chip Enable High Pulse Width	TEHEL		50		50		50		ns	

Notes: 1. Output Enable, G\, may be delayed up to TELQV - TGLQV after the falling edge of E\ without impact on TELQV or by TAVQV - TGLQV after an address change without impact on TAVQV.
2. TEHQZ is specified from G\ or E\, whichever occurs first (CL = 5 pF).
3. Parameter guaranteed, but not tested.

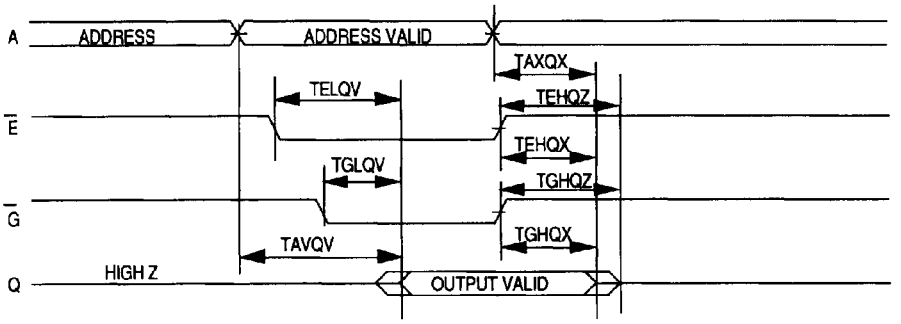
AC Characteristics Write Cycle

	Symbol				
Parameter	**JEDEC**	**Alt**	**Min**	**Max**	**Units**
Write Cycle Time	TAVAV	TWC		10	ms
Address, Output Enable	TAVEL				
Set-up Time	TAVWL				
	TGHWL	TAS			
	TGHEL	TOES	0		ns
Address Hold Time	TWLAX				
	TELAX	TAH	50		ns
Chip Select Set-up Time	TELWL				
	TWLEL	TCS	0		ns
Chip Select Hold Time	TWHEH				
	TEHWH	TCH	0		ns
Write Pulse Width	TWLWH				
	TELEH	TWP	100		ns
Data Set-up Time	TDVWH				
	TDVEH	TDS	50		ns
Data, Output	TWHDX				
Enable Hold Time	TEHDX				
	TEHGL	TDH			
	TWHGL	TOEH	0		ns

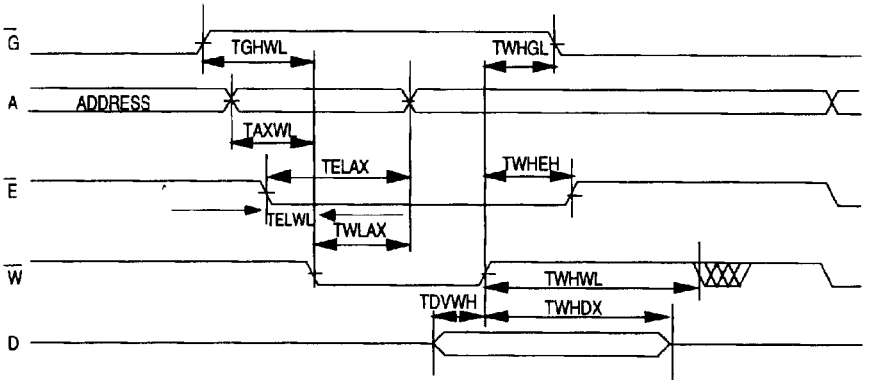
Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



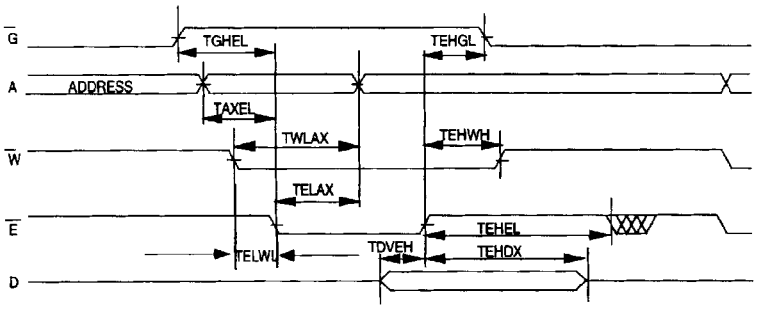
AC Read Cycle - $\overline{E}$ Controlled



AC Write Cycle, Write Controlled



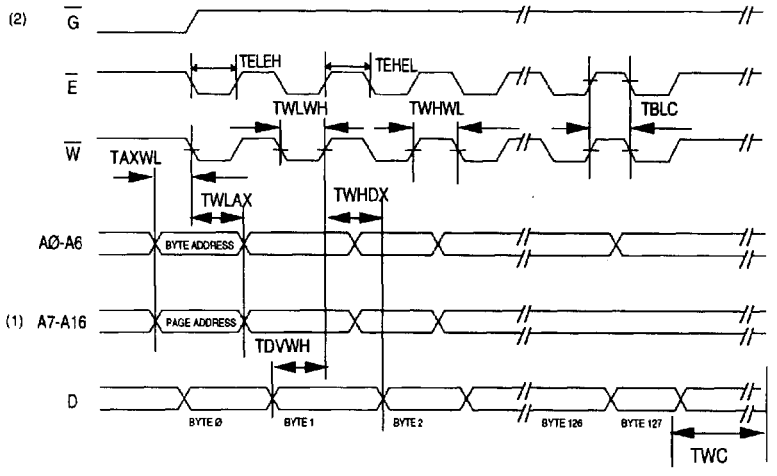
AC Write Cycle, Chip Enable Controlled



Page Mode Write Characteristics

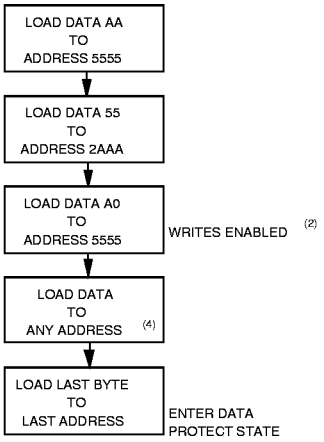
Parameter	Symbol JEDEC	Alt.	Min	Max	Units
Write Cycle Time		TWC		10	ms
Byte Load Cycle Time		TBLC		150	µs (3)
Address Set-up Time	TAXWL	TAS	0		ns
Address Hold Time	TWLAX	TAH	50		ns
Data Set-up Time	TDVWH	TDS	50		ns
Data Hold Time	TWHDX	TDH	0		ns
Write Pulse Width	TWLWH TELEH	TWP	100		ns
Write Pulse Width High	TWHWL	TWPH	50		ns
Chip Enable Pulse Width High	TEHEL	TWPH	50		ns

Page Mode Write Cycle



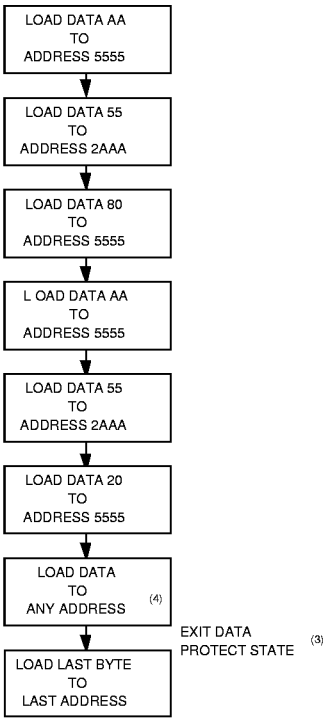
Notes: 1. A7 through A16 must specify the same page address during each high to low transition of W\ or E\.
2. G\ must be high when W\ and E\ are both low.
3. If TBLC> TBLC (MAX) for either W or E, A program cycle is initiated and additional Byte Loads are inhibited.

Software Data Protection Enable Algorithm (1)

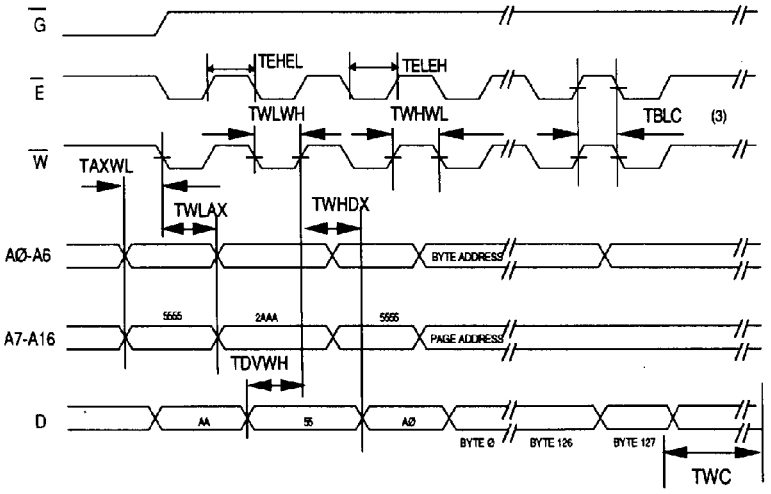


Notes for Software Program Code:
1. Data Format: DQ7-DQØ (Hex);
   Address Format: A16-AØ (Hex).
2. Data Protect state will be activated at the end of program cycle.
3. Data Protect state will be deactivated at the end of program period.
4. 1 to 128 bytes of data are loaded.

Software Data Protection Disable Algorithm (1)



Software Data Protected Page Mode Write Cycle



Notes: 1. A7 through A16 must specify the same page address during each high to low transition of W\ (or E\) after the software code has been entered.
2. G\ must be high when W\ and E\ are both low.
3. If TBLC> TBLC (MAX) for either W or E, A program cycle is initiated and additional Byte loads are inhibited.

AC Characteristics Write Cycle

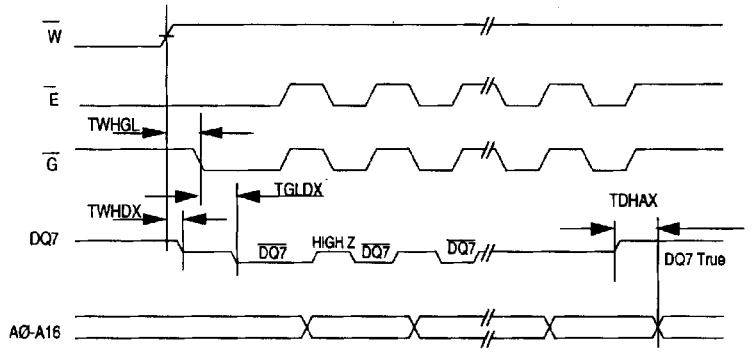
Parameter	Symbol JEDEC	Alt.	Min	Max	Units
Data Hold Time	TWHDX	TDH	10		ns
Output Enable Hold Time	TWHGL	TOEH	10		ns
Output Enable to Output Delay	TGLDX	TOE		100	ns
Write Recovery Time	TDHAX	TWR	0		ns

Note: 1. Parameters guaranteed, but not tested.

Parameter	Symbol JEDEC	Alt.	Min	Max	Units
Data Hold Time	TWHDX	TDH	10		ns
Output Enable Hold Time	TWHGL TEHGL	TOEH	10		ns
Output Enable to Output Delay	TGLDX	TOE		100	ns
Output Enable High Pulse	TGHGL	TOEHP	150		ns
Write Recovery Time		TWR	0		ns

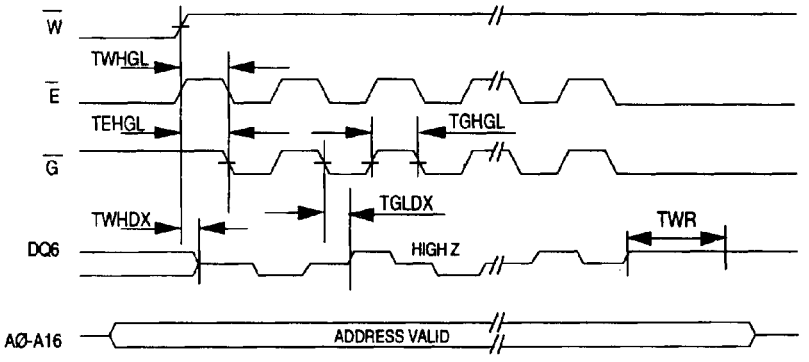
Note: 1. Parameters guaranteed, but not tested.

Data Polling Cycle



Note: Any address in the page being programmed may be used. DQ7 will be the compliment of the true data for the selected address in the page.

Toggle Bit Waveform



Notes: Toggling either G\ or E\ or both G\ and E\ will operate toggle bit.
Beginning and ending state of DQ6 will vary.
Any address location may be used, but the address should not vary.

Ordering Information

Part No.	Speed ns	Package No.
EDI5LM32128C120AM	120	99
EDI5LM32128C150AM	150	99
EDI5LM32128C200AM	200	99

For Commercial or Industrial grade product C or I, repspectively replaces M or Q in part number, e.g. EDI5C32128C120JM becomes EDI5C32128C120JI. (Industrial Temp Range).

Package Description

Package No. 99
68 Lead PLCC
JEDEC MO-47AE