COMPOSITE CELL LOGIC (CCL) SEMI-CUSTOM FAMILY

T-42-11-05

DESIGN FEATURES

- Customer designed LSI
- Two cell libraries—EPL and ISL
- TTL compatible—each cell is functionally similar to the equivalent 7400 Logic Device
- Two-layer metal interconnects
- PNP or diode inputs
- Open-collector, active pullup, or three-state outputs
- 80-milliampere sink-current capability for output cells
- Accommodate custom cell design
- Most standard packages available
- −55°C to +150°C junction temperature
- +5V (±10%) supply voltage; conditions permitting, on-chip derivation of V_{BB} (+1.5V)

PRODUCT DESCRIPTION

Composite Cell Logic (CCL) provides a standard-cell approach to semi-custom bipolar logic. Besides the inherent advantages of LSI and proprietary design, CCL offers the designer a fast turnaround time, a high probability of first-pass success, and a die size that exactly meets all functional requirements of the logic. The CCL approach is particularly well suited to design applications where circuit complexities fall within a range of 100-to-1000 gates.

Figure 1 shows the CCL device together with two standard cells that might be used in the design process. At present, the available cells form two libraries—the Extended Performance Library (EPL) and the Integrated Schottky Library (ISL). Typically, the EPL cell (Figure 2) is used where speed is a critical factor—the speed of EPL cells is comparable to that of Schottky T^2L logic. *Note. Refer to table elsewhere in this data sheet for nominal figures pertaining to circuit propagation speeds of Schottky, Low-Power Schottky, T^2L, and Low-Power T^2L.* All EPL cells are input-expandable with no added delay, are highly immune to internal/external noise, and use active pullups to reduce sensitivity to lead capacitance and the effects of wire-ANDing.

The packing density of an ISL cell (Figure 3) is two to three times greater than that for EPL and the power required is only one-tenth ($^1/_{10}$) to one-twentieth ($^1/_{20}$) as great. The speed of ISL is slightly faster than that of Low-Power Schottky logic. For some circuits, the propagation speeds for ISL and EPL are nearly the same; for other circuits, there are appreciable differences. The speed-comparison table shown later in this data sheet provides a worthwhile guide for overall circuit design.

Output cells of both libraries can sink up to 80-milliamperes of current and both EPL and ISL cells use a 16-micron grid for easy conversion to "Automatic Place and Route" techniques—see Table 1 for a technical summary of both libraries.

Designing with CCL requires a cooperative effort between Signetics and the Customer. The contribution of each party and the overall development sequence are shown in Figure 4.

Table 1. TECHNICAL SUMMARY OF EPL AND ISL LIBRARIES

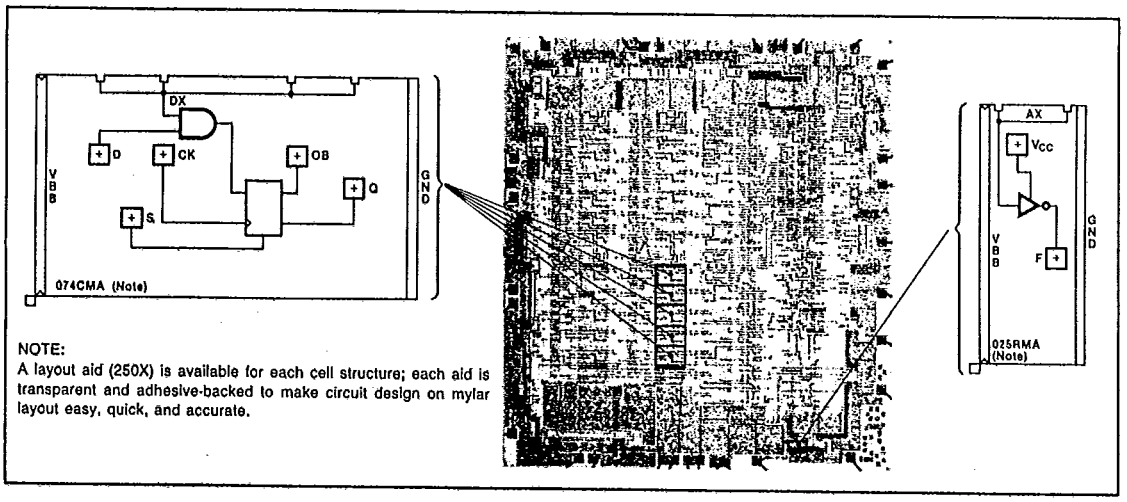
PARAMETER	EPL		ISL
Output structure	Active pullup		Open collector
Input structure	Schottky diode		Schottky diode
Worst-case noise margin	300mV (F.O. = 15)		70mV (F.O. = 15)
Junction temperature range	−55° to +155°C		−55° to +155°C
Power supply	+5V (±10%)		+1.5V (±10%)
	MEDIUM POWER	LOW POWER	
Max average speed (in ns)			
F.O. = 1 (T_J = 150°C)	4.5	5.5	6
F.O. = 6 (T_J = 150°C)	5.5	7.5	6 or 9*
Max average power (in mW):			
T_J = 150°C	5.6	2.6	0.3
Packing density gates/mm**	14 to 42		26 to 78

*Average speed of 6ns requires the use of a resistor pullup cell (optional).

**See Note 5 in Selection Guide regarding derivation of maximum values.

ORDERING INFORMATION

Contact Local Sales Representative



NOTE:
A layout aid (250X) is available for each cell structure; each aid is transparent and adhesive-backed to make circuit design on mylar layout easy, quick, and accurate.

Figure 1. Composite Cell Logic Showing Typical Cell Placement with the Use of Layout Aids.

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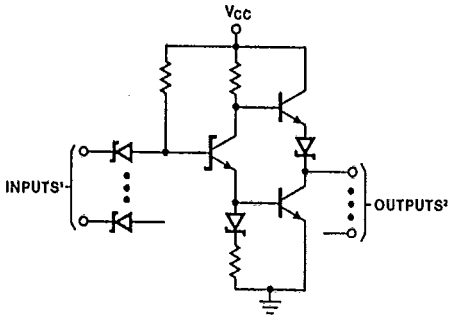
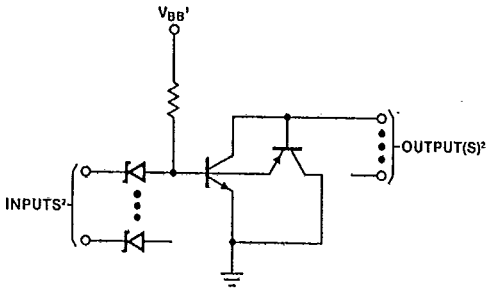


1. Each input is driven by an active pullup; thus, the Fan-In is basically unrestricted.
2. Outputs of standard cells are limited to a Fan-Out of 15; however, special-purpose clock buffer cells have Fan-Outs of up to 100.

Figure 2. Typical EPL Cell.



1. V_{BB} can be derived on-chip; however, if power dissipation is a critical factor, it can also be developed off-chip.
2. For standard cells, up to six inputs and/or outputs can be supported; special-purpose clock buffer cells may have up to 64 outputs.

Figure 3. Typical ISL Cell.

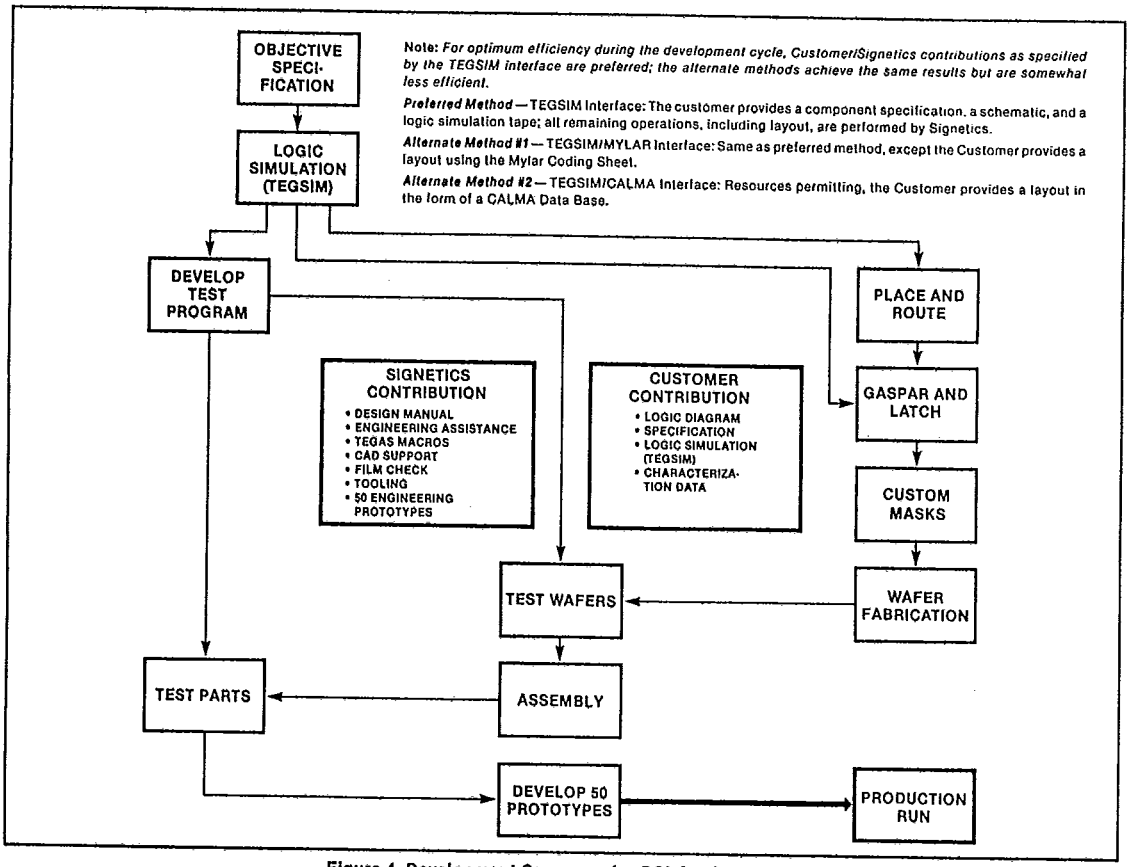


Figure 4. Development Sequence for CCL Logic Design

COMPOSITE CELL LOGIC (CCL)

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TYPICAL PERFORMANCE CHARACTERISTICS

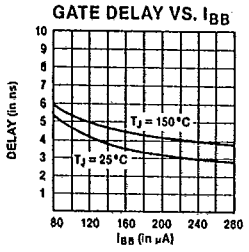
Note: *The information shown in Table 1 and that in the following pages is intended only as a design reference. To improve circuit performance, subject values may change. For guaranteed values, refer to the individual Cell Data Sheets in the CCL Design Manual.*

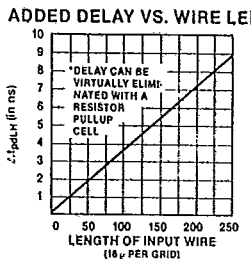
The overall performance of EPL cell structures is determined by the following parameters:

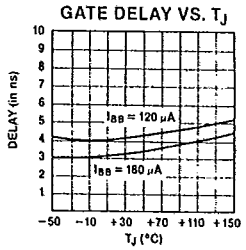
- Discrete gate delays
- Junction temperature (T_J)
- Gate current (I_{BB}) and gate voltage (V_{BB})

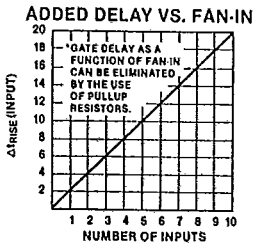
Gate delays are subject to several variables as shown in the accompanying graphs.

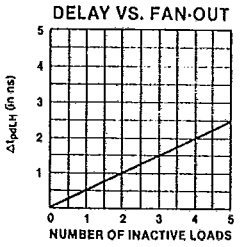
ISL LIBRARY

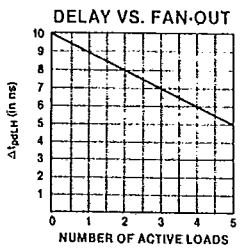




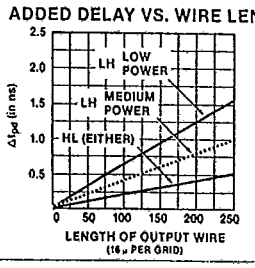


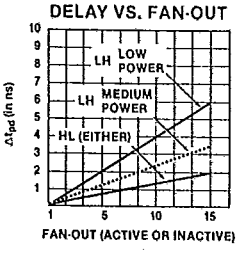


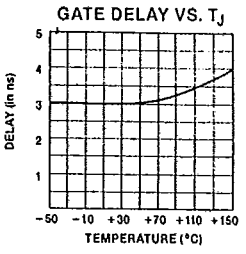




EPL LIBRARY







CALCULATION OF POWER DISSIPATION

At maximum junction temperature (T_J), the maximum power dissipation (P_d) for any given CCL configuration is determined by the following equation:

Maximum Power Dissipation $(P_d) = (T_J - T_A)/\theta_{Ja}$

where,

T_J = +150°C
T_A = Ambient temperature
P_d = Circuit power dissipation in watts
θ_{Ja} = Package thermal resistance in °C/W

thus,

$$P_d\,(ISL) = \frac{\text{total internal cells}}{(0.3\text{mW} \times \text{number of ISL gates used})} + \frac{\text{total I/O cells}}{\Sigma(I_{CC}\,\text{max})(V_{CC}\,\text{max})} + \frac{\text{total output cells}}{\Sigma(V_{OL}\,\text{max})(I_{OL}\,\text{max})}$$

$$P_d\,(EPL) = \frac{\text{internal} + \text{I/O cells}}{\Sigma(I_{CC}\,\text{max})(V_{CC}\,\text{max})} + \frac{\text{total output cells}}{\Sigma(V_{OL}\,\text{max})(I_{OL}\,\text{max})}$$

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Selection Guide and Design Limits for EPL Cells[1,2]

CELL IDENT	CELL DESCRIPTION	CELL AREA[3] (MIL²)	I_{CC} MAX[4] (in mA)	t_{pdHL} MAX[4] (in ns)	t_{pdLH} MAX[4] (in ns)	FAN-OUT[5]
OR GATES						
ILX32	2-wide expandable OR, internal	55.55	1.40	7	12	15 UL
ILX52	2-wide expandable OR, internal	95.23	2.21	5	12	15 UL
IMX52	4-wide expandable OR, internal	95.23	4.75	4	8	15 UL
AND GATES						
ILX07	Expandable AND, internal	47.62	0.88	8	11	15 UL
IMX07	Expandable AND, internal	47.62	2.00	5	7	15 UL
RHX11	Expandable AND, input CLK driver	87.30	7.00	12	7	100 UL
RLX07	Expandable AND, input	47.62	0.97	8	13	15 UL
RLX11	Expandable AND, input CLK driver	71.42	1.85	7	7	40 UL
RMX07	Expandable AND, input	47.62	1.80	5	8	15 UL
RMX11	Expandable AND, input CLK driver	49.36	4.10	4	5	40 UL
TLX07	Expandable AND, output	63.49	1.50	12	9	8mA
TSX07	Expandable AND, output	87.30	8.30	9	8	24mA
NOR GATES (AND/OR inverters)						
ILX02	2-wide expandable NOR, internal	47.62	1.06	5	8	15 UL
ILX24	4-wide expandable NOR, internal	95.23	1.90	3	7	15 UL
IMX02	2-wide expandable NOR, internal	47.62	2.50	4	5	15 UL
IMX24	4-wide expandable NOR, internal	95.23	4.40	4	4	15 UL
TLX24	4-wide expandable NOR, output	95.23	2.15	7	9	8mA
TSX24	4-wide expandable NOR, output	142.85	10.10	8	5	24mA
TZX02A	3-state, 2-wide expandable NOR gate (8mA/16mA)	83.33	10.10	8	5	24mA
NAND GATES						
ILX04	Expandable, internal	31.74	0.60	4	7	15 UL
IMX04	Expandable, internal	31.74	1.40	4	5	15 UL
RLX04	Expandable, input	47.62	0.60	3	10	15 UL
RHX37	Expandable, input CLK driver	95.23	6.50	4	4	100 UL
RLX37	Expandable, input, CLK driver	63.49	1.20	4	5	40 UL
RMX04	Expandable, input	47.62	1.14	4	5	15 UL
RMX37	Expandable, input, CLK driver	71.42	2.60	4	5	55 UL
THX04	Expandable, 40mA output	238.08	13.00	11	16	80mA
TLX03	Expandable, open-collector, output	31.74	1.18	11	19	8mA
TLX04	Expandable, 8mA output	63.49	1.20	8	6	8mA
TSX03	Expandable open-collector, 20mA output	55.55	7.30	11	8	24mA
TSX04	Expandable, 20mA output	87.30	7.30	8	4	24mA
ZLXQB	Non-expandable NAND, 8mA input	71.42	1.50	8	8	8mA
ZLX04	3-state expandable NAND, 8mA output	95.23	3.00	8	7	8mA
ZSX04	3-state expandable NAND, 20mA output	119.04	12.30	11	5	24mA
EXCLUSIVE OR/NOR GATES						
ILX26	2-wide expandable XNOR, internal	103.70	2.10	19	22	15 UL
ILX86	2-wide expandable XOR, internal	111.10	1.80	17	19	15 UL
IMX26	2-wide expandable XNOR, internal	103.17	4.40	13	13	15 UL
IMX86	2-wide expandable XOR, internal	95.23	3.80	11	13	15 UL
FLIP-FLOPS						
ILX74	Negative edge-triggered "D" flip-flop, internal	261.89	2.80	17	12	15 UL
ILX75	Gated "D" latch, internal	142.85	1.80	4	16	15 UL
ILX79	NAND latch, internal	79.36	0.88	4	8	15 UL
IMX74	Negative edge-triggered "D" flip-flop, internal	258.70	5.90	8	8	15 UL
IMX75	Gated "D" latch, internal	142.85	3.70	6	12	15 UL
IMX79	NAND latch, internal	79.36	2.00	4	5	15 UL

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Selection Guide and Design Limits for EPL Cells[1,2] (Continued)

CELL IDENT	CELL DESCRIPTION	CELL AREA[3] (MIL²)	I_{CC} MAX[4] (in mA)	t_{pdHL} MAX[4] (in ns)	t_{pdLH} MAX[4] (in ns)	FAN-OUT[5]
SCHMITT TRIGGER						
RMX14	Inverting, input	87.30	1.90	3	5	15 UL
HIGH-IMPEDANCE RECEIVER						
RH640	HI-Z Rcvr, input	119.04	5.20	14	11	15 UL
POWER-UP CLEAR						
POWER	Power-up/clear	166.66	7.80	—	—	15 UL
DIODE EXPANSION						
Twenty-six (26) diode expansion cells are available ranging in die size from 7.94 Mil² to 71.42 Mil².						
DUMMY LOAD and/or PULLUPS						
Dummy loads or pull-up cells are not required for the EPL Library.						

Notes:
1. To improve performance and to meet changing needs, the EPL library is updated on a continuing basis via additions, deletions, and/or modifications; for the current status of any given cell, contact the nearest Signetics Sales Office.
2. Custom EPL cells are available on a "qualification" basis.
3. To convert Mil² to Micron², multiply Mil-value by 645.16.
4. Design limits are based on standard modeling with similar circuits used in Signetics standard bipolar LSI products. Actual simulation limits are maintained to be consistent with characterization updates for the CCL libraries.
5. A fan-out Unit Load (UL) corresponds to a load factor of approximately 220 microamperes.

Selection Guide and Design Limits for ISL Cells[1,2]

CELL IDENT	CELL DESCRIPTION	CELL AREA[3] (MIL²)	I_{CC} MAX[4,5] (in mA)	I_{BB}[5,6] (in UL)	t_{pdHL} MAX[5,7] (in ns)	t_{pdLH} MAX[5,7] (in ns)	FAN-OUT[6]
MSI CELLS							
151ILA	8-to-1 multiplexer	371.46	N/A	15	Refer to individual Data Sheets in CCL Design Manual for these parameters.		
161CLA	4-bit counter	TBD	N/A	60			
194ILA	4-bit left-right shift register	1317.4	N/A	40			
283ILA	4-bit adder	857.1	N/A	55			
934CLA	4-bit ALU	1650.7	N/A	30			
OR GATES							
20RIL	2-wide expandable OR, internal	31.7	N/A	3	14	12	6 UL
30RIL	3-wide expandable OR, internal	44.5	N/A	4	16	12	6 UL
40NIL	4-wide NOR/OR, internal	50.8	N/A	5	18	12	5 or 6 UL
40RIL	4-wide expandable OR, internal	50.8	N/A	5	18	12	6 UL
60RIL	6-wide expandable OR, internal	114.3	N/A	7	22	12	6 UL
AND GATES							
007IH	CLK buffer expandable AND, internal	63.5	1.8	N/A	19	18	64 UL
007IL	Expandable AND, internal	25.4	N/A	2	12	12	6 UL
007RH	CLK buffer expandable AND, input	57.1	1.8	N/A	19	18	64 UL
007RM	Expandable AND, input	63.5	1.2	N/A	7	9	15 UL
007TL	Expandable AND, output (8mA)	63.5	2.0	N/A	13	15	8mA
007TS	Expandable AND, output (20mA)	95.23	8.3	N/A	12	14	24mA
009IL	2-input expandable AND, internal	25.4	N/A	2	12	14	6 UL
015IL	3-input expandable AND, internal	31.7	N/A	2	12	16	6 UL

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Selection Guide and Design Limits for ISL Cells[1,2] (Continued)

CELL IDENT	CELL DESCRIPTION	CELL AREA[3] (MIL²)	I_{CC} MAX[4,5] (in mA)	I_{BB}[5,6] (in UL)	t_{pdHL} MAX[5,7] (in ns)	t_{pdLH} MAX[5,7] (in ns)	FAN-OUT[6]
NOR GATES (AND/OR INVERTERS)							
002TL	2-wide NOR, output (8mA)	63.5	2.0	N/A	13	9	8mA
002ZK	3-state 2-wide NOR, output (8/16mA)	133.3	3.9	N/A	20	10	16mA
027TL	3-wide NOR, output (8mA)	76.2	2.5	N/A	13	10	8mA
2NRCL	2-wide NOR, clock buffer driver	25.4	Note 8	Note 8	2	12	6 UL
2NRIH	2-wide expandable NOR, clock buffer	57.1	1.8	N/A	16	18	64 UL
2NRIL	2-wide expandable NOR, internal	25.4	N/A	2	2	12	6 UL
3NRIL	3-wide expandable NOR, internal	31.7	N/A	3	2	14	6 UL
40NIL	4-wide NOR/OR, internal	50.8	N/A	5	18	12	6 UL
4NRIL	4-wide expandable NOR, internal	44.4	N/A	4	2	16	6 UL
6NRIL	6-wide expandable NOR, internal	95.2	N/A	6	2	20	6 UL
NAND GATES							
003IL	2-input expandable, internal	19	N/A	1	4	10	6 UL
004IH	Clock buffer, expandable, internal	50.8	1.3	N/A	15	13	64 UL
004RH	Clock buffer, expandable, input	63.5	1.3	N/A	15	13	64 UL
004RM	Expandable, input	57.1	1.6	N/A	3	10	15 UL
004TB	Expandable, output (12mA/24mA)	76.2	3.4	N/A	17	7	24mA
004TL	Expandable, output (8mA)	57.1	1.5	N/A	13	7	8mA
004TS	Expandable, output (20mA)	76.2	7.3	N/A	14	6	24mA
004ZL	3-state expandable NAND (8mA)	69.84	2.4	N/A	14	8	8mA
005QL	Clock buffer driven, expandable, internal	19	Note 8	Note 8	2	10	6 UL
005IH	Expandable, internal, fan-out = 18	31.7	N/A	3	2	14	18 UL
005IL	Expandable, internal	19	N/A	1	2	10	6 UL
005IM	Expandable, internal, fan-out = 12	19	N/A	2	2	12	12 UL
005RM	Expandable, input	69.8	1.6	3	3	13	15 UL
005TB	Expandable, output (80mA) open collector	171.42	8.2	N/A	15	25	70mA
005TL	Expandable, output (8mA) open collector	31.7	3.3	N/A	13	17	8mA
012IL	3-input expandable, internal	25.4	N/A	1	6	10	6 UL
368ZL	3-state expandable NAND (12mA/24mA)	76.19	3.4	N/A	17	7	24mA
EXCLUSIVE OR/NOR GATES							
136IL	2-wide expandable XOR, internal	44.4	N/A	4	14	14	6 UL
266IL	2-wide expandable XOR, internal	38.1	N/A	3	12	12	6 UL
FLIP-FLOPS							
NRLIL	NOR latch, internal	57.1	N/A	4	2	14	5 UL
TOGCM	Clock buffer driven, toggle FF, internal	152.4	N/A	8	24	18	9 UL
074CL	Clock buffer driven "D", internal (fan-out = 6)	95.2	N/A	4	22	16	5 UL
074CM	Clock buffer driven "D", internal (fan-out = 12)	133.3	N/A	6	24	18	10 UL
074IL	Positive edge-triggered "D", internal	114.3	N/A	6	22	16	5 UL
075IL	Gated latch, internal	76.2	N/A	5	4	16	5 UL
279IL	NAND latch, internal	38.1	N/A	2	4	10	5 UL
POWER-UP CLEAR							
PWRRL	Power-Up/Clear	19	0.7	N/A	—	—	6 UL
DUMMY LOADS							
REFIL	Internal dummy load	12.7	N/A	1	—	—	—
REFIL	Output dummy load	19.0	0.26	N/A	—	—	—
DIODE EXPANSION							
Thirty-five (35) diode expansion cells are available ranging in die size from 6.35 Mil² to 19.05 Mil².							

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Notes:
1. To improve performance and to meet changing needs, the ISL library is updated on a continuing basis via additions, deletions, and/or modifications; for the current status of any given cell, contact the nearest Signetics Sales Office.
2. Custom ISL cells are available on a "qualification" basis.
3. To convert Mil² to Micron², multiply Mil-value by 645.16.
4. Maximum values of I_{CC} do not always occur at the same temperature for all ISL cells, thus I_{CC} should not be used for calculation of power dissipation for a discrete cell. The tabularized values can properly be used for worst-case power supply design.
5. Design limits are based on standard modeling with similar circuits used in Signetics standard bipolar LSI products. Actual simulation limits are maintained to be consistent with characterization updates for the CCL libraries.
6. A Unit Load (UL) for I_{BB} corresponds to a load factor of approximately 190 microamperes; a fan-out unit load corresponds to a load factor of approximately 220 microamperes.
7. The propagation-delay measurements were taken at 150°C with both fan-out and fan-in equal to 1.
8. The internal Clock Buffer ISL cells listed below are driven by any one of the special driver cells; to compute I_{CC} requirements, refer to appropriate data sheet(s) in CCL Design Manual.

Driven Cells	
Internal NOR	—C12NRCLA
Internal D Flip-Flop (Fan-Out = 5)	—C1074CLA
Internal D Flip-Flop (Fan-Out = 10)	—C1074CMA
Internal Toggle Flip-Flop	—CIT06CMA
Internal NAND	—C1005CLA

Driver Cells (Fan-Out = 64)	
Internal AND	—C1007IHA
Input AND	—C1007RHA
Input NOR	—C12NRIHA
Internal NAND	—C1004IHA
Input NAND	—C1004RHA

Table 2. Comparison of CCL to 74S/74LS Functions

LOGIC FUNCTION	PARAMETERS[1,3,6]	LOGIC DEVICES		CCL (ISL CELLS)[2]	CCL (EPL CELLS)	
		74SXX	74LSXX		LOW POWER	MED. POWER
NAND (5400)	Power (in mW)	35.7	4.13	0.31	2.56	5.61
	t_{ON} (in ns)	5.0	15.0	2.00	3.00	3.00
	t_{OFF} (in ns)	4.5	15.00	10.00	6.00	3.00
AND (5408)	Power (in mW)	61.2	9.35	0	0	0
	t_{ON} (in ns)	7.5	20.00	0	0	0
	t_{OFF} (in ns)	7.0	15.00	2.00[4]	0	0
NOR (5402)	Power (in mW)	50.9	5.91	0.63	4.68	10.45
	t_{ON} (in ns)	5.5	15.00	2.00	3.00	3.00
	t_{OFF} (in ns)	5.5	15.00	12.00	7.00	3.00
OR (5432)	Power (in mW)	68.7	11.00	0.94	6.90	23.90
	t_{ON} (in ns)	7.00	22.00	14.00	4.00	3.00
	t_{OFF} (in ns)	7.00	22.00	12.00	8.00	5.00
EXCLUSIVE OR (5486)	Power (in mW)	103.00	13.75	1.25	9.24	19.00
	t_{ON} (in ns)	10.00	22.00	14.00	13.00	8.00
	t_{OFF} (in ns)	10.50	30.00	14.00	15.00	8.00
EXCLUSIVE NOR (54266)	Power (in mW)	N/A	17.90	0.94	10.70	22.00
	t_{ON} (in ns)	N/A	30.00	14.00	14.00	9.00
	t_{OFF} (in ns)	N/A	30.00	14.00	18.00	11.00
AND/OR INVERTERS (5451)	Power (in mW)	54.70	6.05	0.63	4.68	10.45
	t_{ON} (in ns)	5.50	20.00	2.00	3.00	3.00
	t_{OFF} (in ns)	5.50	20.00	12.00	7.00	3.00
D FLIP-FLOP (5474)	Power (in mW)	137.50	22.00	1.88	15.40	37.10
	t_{ON} (in ns)	13.50	40.00	22.00	12.00	8.00
	t_{OFF} (in ns)	6.00	25.00	18.00	11.00	8.00
	F_{max} (in MHz)	75.00	25.00	30.00	25.00[5]	50.00[5]

Notes:
1. Unless otherwise noted, all switching parameters (t_{ON} and t_{OFF}) are at 25°C/5V max.
2. Switching parameters for ISL cells are at 150°C max.
3. Power = $\frac{I_{CC_0} + I_{CC_1}}{2} \times V_{CC}$ max.
4. t_{OFF} is 2 ns for each input; t_{OFF} can be reduced to 0 ns with a pullup cell.
5. F_{max} is at 150°C min.
6. ISL and CCL parameter values derived from design limits—refer to Note 4 under "Selection Guide and Design Limits for EPL Cells."

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COMPOSITE CELL LOGIC (CCL)

SEMI-CUSTOM FAMILY

T-42-11-05

ABSOLUTE MAXIMUM RATINGS

PARAMETER	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V
V_{BB}	ISL gate supply voltage	+7.0	V
E_{IN}	Input voltage, continuous	−0.5 to +5.5	V
I_{IN}	Input current, continuous	−30 to +1.0	mA
V_O	Voltage applied to open-collector output in off-state	−0.5 to +7.0	V
T_A	Ambient temperature, operating	−55 to +125	°C
T_{STG}	Storage temperature	−65 to +150	°C

AC AND DC ELECTRICAL CHARACTERISTICS

Conditions[1]: V_{CC} = 5.0V (±10%)
V_{BB} = 1.5V (±10%)
T_J = 0°C to +150°C

PARAMETER		TEST CONDITIONS[2]		DESIGN LIMITS[3] MIN	TYP	MAX	UNIT
EPL GATE (INTERNAL)							
$I_{CC/G}$	Power supply current per gate			0.18	0.29	0.47	mA
I_{LF}	Input load factor				1		UL
F_O	Fan-Out				15		
t_{pdAV}	Average gate propagation delay = $\frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = 1 EPL gate; Fan-out = 1 EPL gate			3	5.5	ns
t_{pdLH}	Propagation delay from low-to-high state	Fan-in = 1 EPL gate; Fan-out = 1 EPL gate			4	7	ns
t_{pdHL}	Propagation delay from high-to-low state				2	4	ns
ISL GATE (INTERNAL)							
$I_{BB/G}$	Power supply current per gate			110	150	190	µA
I_{LF}	Input load factor				1		UL
F_O	Fan-out				6		UL
t_{pdAV}	Average gate propagation delay = $\frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = 1 ISL gate; Fan-out = 1 ISL gate			3	6	ns
t_{pdLH}	Propagation delay from low-to-high state	Fan-in = 1 ISL gate; Fan-out = 1 ISL gate			5	10	ns
t_{pdHL}	Propagation delay from high-to-low state				1	2	ns
EPL/ISL INPUT CELLS							
V_{TH}	Input threshold voltage			0.8		2.0	V
V_{CD}	Input clamp diode voltage	I_{IN} = −18mA				−1.2	V
I_{IL}	Input low current	V_{IN} = 0.4V	PNP input			−20	mA
			Diode input			−400	
I_{IH}	Input high current	V_{IN} = 2.7V				20	µA
I_I	Maximum input high current	V_{IN} = 5.5V				100	
F_O	Fan-out (ISL library)	Standard cell				6	UL
		Clock buffer cell				64	
	Fan-out (EPL library)	Standard cell				15	
		Clock buffer cell				55	
		Clock buffer cell				100	

COMPOSITE CELL LOGIC (CCL) SEMI-CUSTOM FAMILY

T-42-11-05

AC AND DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		TEST CONDITIONS[2]		DESIGN LIMITS[3] MIN	TYP	MAX	UNIT
EPL/ISL THREE-STATE OUTPUT BUFFERS							
I_{LF}	Input load factor	EPL				1 or 9	UL
		ISL				2 or 4	
V_{OL}	Output low voltage	Military: 4mA				400	mV
		Commercial: 8mA				500	
		Military: 12 mA				400	mV
		Commercial: 24 mA				500	
V_{OH}	Output high voltage	Military: $I_{OH} = -400\ \mu A$		2.5			V
		Commercial: $I_{OH} = -400\ \mu A$		2.7			
I_{OS}	Output short circuit current	$V_{OUT} = 0V$		−15		−100	mA
I_{OLZ}	Three-state off current (output low)	$V_{OUT} = 0.4V$				−20	μA
I_{OHZ}	Three-state off current (output high)	$V_{OUT} = 2.4V$				20	μA
EPL/ISL OPEN-COLLECTOR OUTPUT BUFFERS							
I_{LF}	Input load factor	EPL	8 mA output			1	UL
			20 mA output			3	
			80 mA output			5	
		ISL				2 or 4	
V_{OL}	Output low voltage	I_{OL}	8 mA output			500	mV
			20 mA			500	
			70 mA			500	
			80 mA			800	
I_{OH}	Output leakage current	V_{OUT}	80 mA Cells 2.75			60	μA
			5.5V			250	
			8/20 mA Cells 5.5V			100	
ACTIVE PULLUP OUTPUT BUFFER							
I_{LF}	Input load factor	EPL				1 or 3	UL
		ISL				2 or 4	
V_{OL}	Output low voltage	$I_{OL} = 8$ mA or 20 mA				500	mV
V_{OH}	Output high voltage	Military	$I_{OH} = -400\ \mu A$ or -1.0 mA	2.5			V
		Commercial	$I_{OH} = -400\ \mu A$ or -1.0 mA	2.7			
I_{OS}	Output short circuit current	$V_{OUT} = 0V$	8 mA output	−15		−100	mA
			20 mA output	−40		−100	

Notes:
1. Maximum power dissipation is determined from individual cell data sheets; the figures are then summed to calculate total power for the chip. The total power must be less than the Maximum Power Dissipation (P_d) calculated earlier in this data sheet.
2. For test circuits and timing waveforms, refer to individual cell data sheets in the CCL Design Guide.
3. Design limits are based on standard modeling with similar circuits used in Signetics standard bipolar LSI products. Actual simulation limits are maintained to be consistent with characterization updates for the CCL libraries.

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