intech
ADVANCED ANALOG

ADC-1600
Four Microsecond 16-Bit Analog to Digital Converter

DESCRIPTION

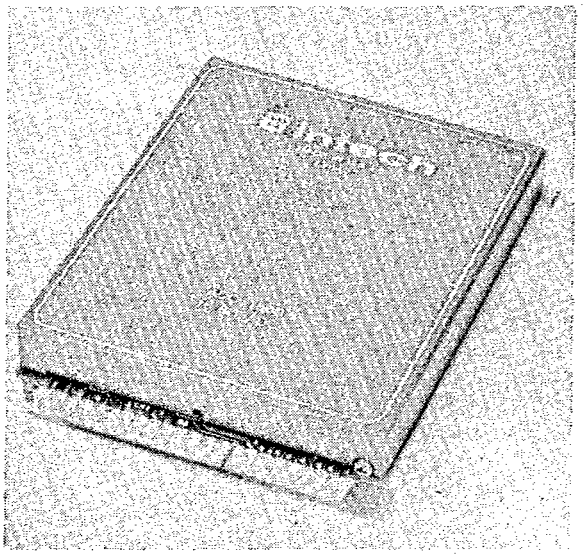
The ADC-1600 is a state of the art, very high speed sixteen bit analog to digital converter. This device will resolve an input signal to a corresponding digital word in as fast as four microseconds.

FEATURES

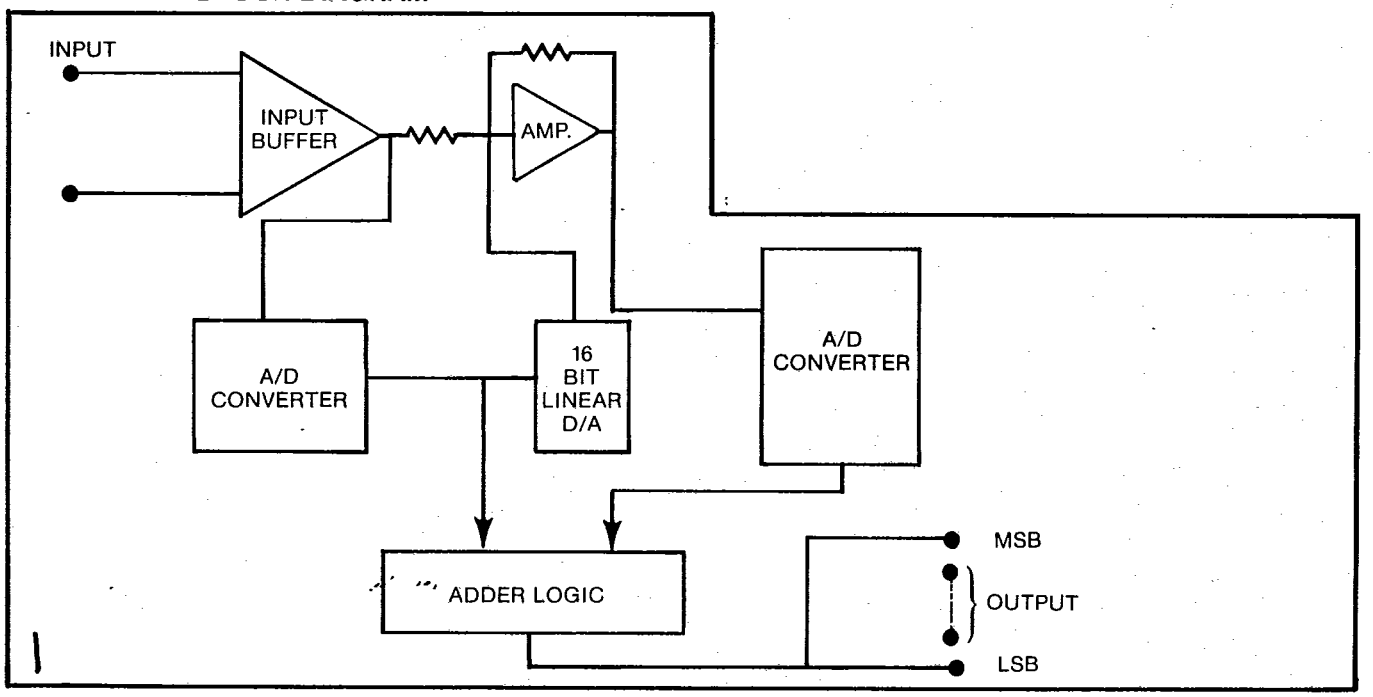
- 16 bits resolution
- Converts as fast as 4 μs
- TRI-STATE outputs (byte segmented)

OPERATION

A negative going pulse with a minimum width of 50 nanoseconds to start convert input (Pin 18) will initiate the conversion cycle. This pulse must be TTL compatible and capable of driving one load. On the leading edge of the start convert pulse the busy output will switch to a HI state and conversion will start automatically. At the end of conversion, the busy output goes from HI to LO. At this time, the conversion is completed and the latched parallel digital word is updated.



FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS
(Typical @ 25°C, ±15V and +5V Supplies Unless Otherwise Specified)

Parameter ADC-1600-	4-0S-S 4-0S-D	4-2S-S	4-5S-S	Units
RESOLUTION	16	16	16	bits
ACCURACY				
Quantizing Error	±½	±½	±½	LSB
Nonlinearity Error	±15	±15	±15	ppm
Input Signal Resolution	15	15	15	ppm
Noise (Ref. to input)	100	300	240	μV p-p
STABILITY				
Offset vs. Temperature	±7	±7	±7	ppm/°C
Gain vs. Temperature	±7	±7	±7	ppm/°C
Nonlinearity vs. Temperature	±2	±2	±2	ppm/°C
Power Supply Sensitivity	±.002	±.002	±.002	%/% Δ Vs
Long Term Stability	±30	±30	±30	ppm/mo.
Warm-Up Time	5	5	5	minutes
CONVERSION TIME				
S/H in Sample Mode	4	4	4	μs
S/H Functioning	N/A	6	9	μs
ANALOG INPUT				
Input Voltage Range	±10	±10	±10	Volts
Input Overload	±15	±15	±15	Volts
Input Impedence	1000	1000	1000	MΩ
LOGIC INPUTS				
Start Convert—TTL negative pulse, 50 ns min. width, 1TTL load. Conversion starts automatically.				
Sample & Hold (TTL Controlled)—LO for sample mode; HI for hold mode; 1 TTL load.				
"One TTL load is—1.6 mA max. @ LO (+0.4 V) and 40 μA max. @ HI (+2.4 Volts)				
DIGITAL OUTPUTS				
Parallel Data Outputs:	TTL Compatible			
Latched	5 TTL Fanout, Byte Segmented TRI-STATE			
States	LO = 0 TO +.4; HI = +2.4 to +5			Volts
Busy Output	HI during Conversion; LO otherwise			
Code	Obin or Cobin*			
TEMPERATURE RANGE				
Operating	0 to +70	0 to +70	0 to +70	°C
Storage	-10 to +85	-10 to +85	-10 to +85	°C
POWER SUPPLY				
Voltage	±15, ±3	±15, ±3	±15, ±3	Volts, %
	+5, ±5	+5, ±5	+5, ±5	Volts, %
Current				
+15V Supply	255	315	315	mA
-15V Supply	240	300	300	mA
+5V Supply	350	350	350	mA
Shielding	RFI Six-Sides EMI Five-Sides			
Reference	Internal			

*code is normally Obin specify suffix-1 for Cobin.

SAMPLE & HOLD

The Sample and Hold is controlled by a TTL Logic Control Signal which must be externally generated. When the Control Signal is LO, the S&H acts as a unity gain amplifier, tracking the Input Voltage, when HI the S&H holds and freezes the input signal.

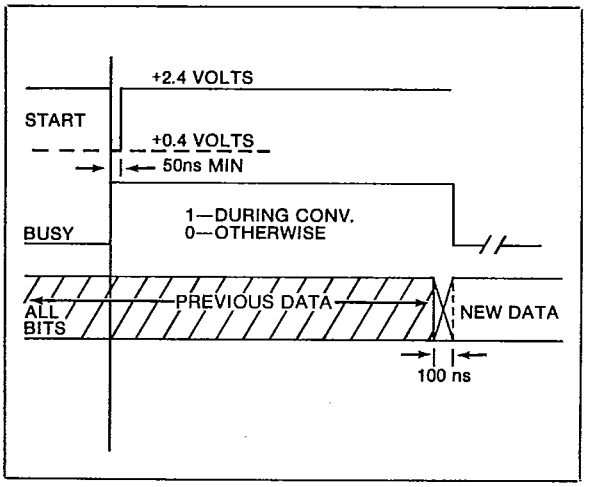
HANDLING OF GROUNDS

Proper grounding procedures are essential for maximum efficiency, minimization of noise and interference. There are three grounds in the ADC-1600, common ground, analog ground, and logic ground. The common ground is the +15V and −15V return. The analog ground is the input signal return. The logic ground is the +5V logic supply return which carries switching currents that may interfere with proper operation of the ADC-1600 if not hooked up back at the supplies as shown in figure 2. The case of the ADC-1600 is connected to the Pin "9", at the connector and should be connected to analog ground. All the connections should be utilized.

OUTPUTS

The latched outputs are byte segmented and may be enabled separately for connection to a TRI-STATE BUSS. A HI State on the enable pin causes the 8 outputs (8 MSB's or 8 LSB's) to appear as a high impedence. A low state enables the outputs. Converter operation is independent of these output controls.

TIMING DIAGRAM



PIN DESIGNATION

1	+15V	A	+15V
2	-15V	B	-15V
3	COMMON	C	COMMON
4	MSB ENABLE	D	LSB ENABLE "LO to ENABLE"
5	ANALOG GROUND	E	N/C
6	V IN	F	N/C
7	N/C	H	N/C
8	N/C	J	N/C
9	CASE	K	N/C
10	N/C	L	Bit 4
11	N/C	M	Bit 5
12	N/C	N	Bit 6
13	N/C	P	Bit 7
14	N/C	R	Bit 8
15	SAMPLE & HOLD CONTROL	S	Bit 9
16	+5 Volts	T	Bit 10
17	LOGIC GROUND	U	Bit 11
18	START	V	Bit 12
19	STATUS	W	Bit 13
20	MSB	X	Bit 14
21	Bit 2	Y	Bit 15
22	Bit 3	Z	LSB

CODING TABLE—OFFSET BINARY

	MSB 1	2	3 14	15	16
+(FS-1 LSB) = +9.9997V	1	1	1	1	1
0V	1	0	0	0	0
-FS = -10.000V	0	0	0	0	0

Resolution	#Steps	$\frac{1}{2^n}$	LSB for 10V Span
16 bits	65,535	0.0000153	152.6 μV

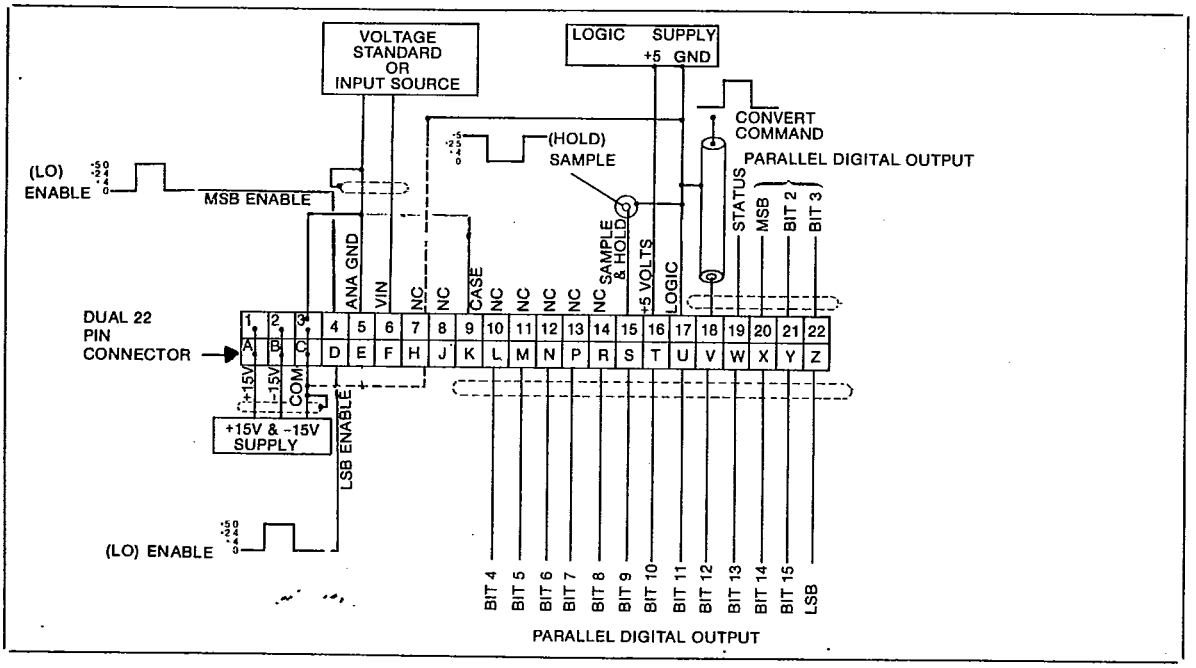
CODING TABLE—COMPLEMENTARY OFFSET BINARY

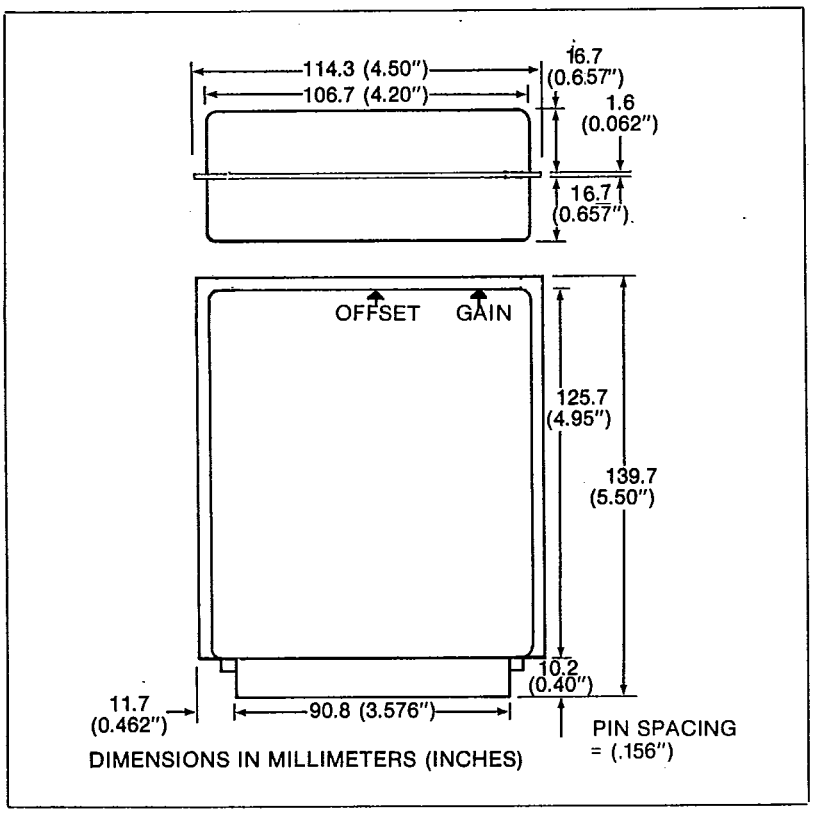
Analog Input (FS = full scale)	MSB 1	Data Output (Bits) 2	3 14	15	LSB 16
+(FS-1 LSB) = +9.9997V	0	0	0	0	0
+½ FS= +5.000V	0	0	1	1	1
+1 LSB =+305 μV	0	1	1	1	0
0 = 0V	0	1	1	1	1
-1 LSB = -305 μV	1	0	0	0	0
-½ FS = -5.000V	1	0	1	1	1
-FS = -10.000V	1	1	1	1	1

The least-significant-bit (LSB) weight is:

Resolution	#Steps 2^n	$\frac{1}{2^n}$	LSB for 10V Span
16 bits	65,535	0.0000153	152.6 μV

RECOMMENDED HOOK-UP





ORDERING INFORMATION
SPECIFY - - - - - - - ADC-1600-4

SAMPLE & HOLD OPTION	Enter
No sample & hold	0S
2 μs, .006%	2S
5 μs, .0007%	5S

INPUT OPTION*	Enter
Differential	D
Single ended	S

CODE OPTION	Enter
Cobin	1

*NOTE: Differential inputs are available only if no S/H is necessary.
There is no additional charge for differential VS. single ended input.

WITHOUT SAMPLE & HOLD		WITH SAMPLE & HOLD	
MODEL	CONV. TIME	MODEL	CONV. TIME
ADC-1600-4-0S-S	4 μsec.	ADC-1600-4-2S-S	6 μsec.
ADC-1600-4-0S-D	4 μsec.	ADC-1600-4-5S-S	9 μsec.

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