

P4C1981/P4C1981L, P4C1982/P4C1982L ULTRA HIGH SPEED 16K x 4 CMOS STATIC RAMS

T-46-23-10

★ FEATURES

- Full CMOS, 6T Cell
- High Speed (Equal Access and Cycle Times)
 - 12/15/20/25ns (Commercial)
 - 20/25/35/45/55ns (Military)
- Low Power Operation (Commercial/Military)
 - 715 mW Active - 12, 15
 - 550/660 mW Active - 20, 25, 35, 45, 55
 - 193/220 mW Standby (TTL Input)
 - 83/110 mW Standby (CMOS Input) P4C1981/82
 - 5.5 mW Standby (CMOS Input) P4C1981L/82L (Military)
- Output Enable and Dual Chip Enable Functions
- 5V ± 10% Power Supply
- Data Retention with 2.0V Supply, 10 μA Typical Current (P4C1981L/1982L Military)
- Separate Inputs and Outputs
 - P4C1981/L Input Data at Outputs during Write
 - P4C1982/L Outputs in High Z during Write
- Fully TTL Compatible Inputs and Outputs
- Produced with PACE Technology™
- Standard Pinout (JEDEC Approved)
 - 28-Pin 300 mil DIP, SOJ
 - 28-Pin 350 x 550 mil LCC

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★ DESCRIPTION

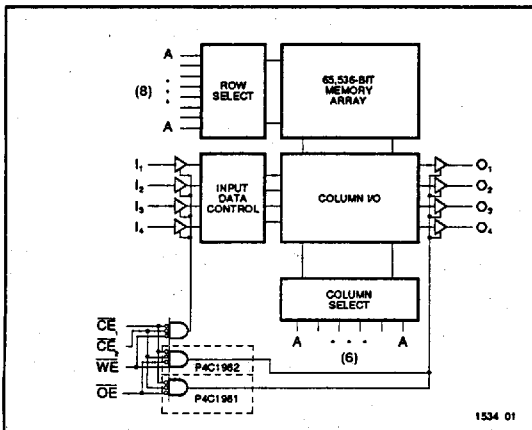
The P4C1982/L and P4C1981/L are 65,536-bit (16K x 4) ultra high speed static RAMs similar to the P4C198, but with separate data I/O pins. The P4C1981/L feature a transparent write operation when \overline{OE} is low; the outputs of the P4C1982/L are in high impedance during the write cycle. All devices have low power standby modes. The RAMs operate from a single 5V ± 10% tolerance power supply. With battery backup, data integrity is maintained for supply voltages down to 2.0V. Current drain is typically 10 μA from 2.0V supply.

CMOS is used to reduce power consumption to a low 715 mW active, 193 mW standby. For the P4C1982L and P4C1981L, power is only 5.5 mW standby with CMOS input levels. The P4C1982/L and P4C1981/L are members of a family of PACE RAM™ products offering super fast access times never before available at these complexity levels in TTL-compatible bipolar or CMOS technologies. The P4C1982/L and P4C1981/L are manufactured with PACE Technology.

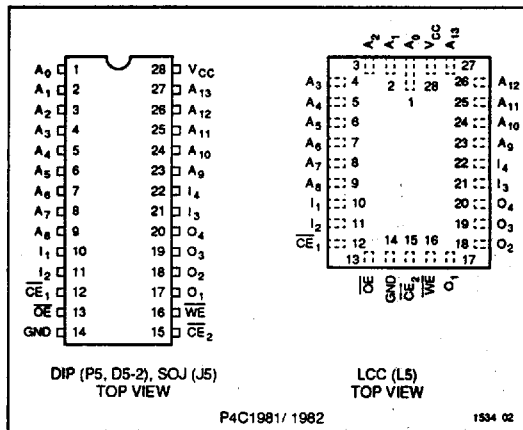
Access times as fast as 12 nanoseconds are available, permitting greatly enhanced system operating speeds.

The P4C1982/L and P4C1981/L are available in 28-pin 300 mil DIP and SOJ, and in 28-pin 350x550 mil LCC packages providing excellent board level densities.

★ FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Means Quality, Service and Speed

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P4C1981/1981L, P4C1982/1982L

MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{CC}	Power Supply Pin with Respect to GND	-0.5 to +7	V
V _{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to V _{CC} +0.5	V
T _A	Operating Temperature	-55 to +125	°C

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Symbol	Parameter	Value	Unit
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current	50	mA

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RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade ⁽²⁾	Ambient Temperature	GND	V _{CC}
Military	-55 to +125°C	0V	5.0V ± 10%

1534 Tbl 03

Grade ⁽²⁾	Ambient Temperature	GND	V _{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

1534 Tbl 04

DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage⁽²⁾

Sym.	Parameter	Test Conditions	P4C1981 P4C1982		P4C1981L P4C1982L		Unit	
			Min	Max	Min	Max		
V _{IH}	Input High Voltage		2.2	V _{CC} +0.5	2.2	V _{CC} +0.5	V	
V _{IL}	Input Low Voltage		-0.5 ⁽³⁾	0.8	-0.5 ⁽³⁾	0.8	V	
V _{HC}	CMOS Input High Voltage		V _{CC} -0.2	V _{CC} +0.5	V _{CC} -0.2	V _{CC} +0.5	V	
V _{LC}	CMOS Input Low Voltage		-0.5 ⁽³⁾	0.2	-0.5 ⁽³⁾	0.2	V	
V _{CD}	Input Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA	—	-1.2	—	-1.2	V	
V _{OL}	Output Low Voltage (TTL Load)	I _{OL} = +8 mA, V _{CC} = Min.		0.4		0.4	V	
V _{OH}	Output High Voltage (TTL Load)	I _{OH} = -4 mA, V _{CC} = Min.	2.4	—	2.4	—	V	
I _{LI}	Input Leakage Current	V _{CC} = Max. V _{IN} = GND to V _{CC}	Mil. Com'l.	-10 -5	+10 +5	-5 n/a	+5 n/a	µA
I _{LO}	Output Leakage Current	V _{CC} = Max., CE ₁ , CE ₂ = V _{IH} V _{OUT} = GND to V _{CC}	Mil. Com'l.	-10 -5	+10 +5	-5 n/a	+5 n/a	µA

n/a = Not Applicable

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CAPACITANCES⁽⁴⁾

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	pF

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Symbol	Parameter	Conditions	Typ.	Unit
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	pF

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Notes:

- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with V_{IL} and I_{IL} not more negative than -3.0V and -100mA, respectively, are permissible for pulse widths up to 20 ns.
- This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS

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Over recommended operating temperature and supply voltage⁽²⁾

Symbol	Parameter	Test Conditions	P4C1981 P4C1982		P4C1981L P4C1982L		Unit
			Min	Max	Min	Max	
I_{CC}	Dynamic Operating Current - 12, 15	$V_{CC} = \text{Max.}, f = \text{Max.},$ Outputs Open Mil. Com'l.	—	n/a 130	—	n/a n/a	mA
I_{CC}	Dynamic Operating Current - 20, 25, 35, 45, 55	$V_{CC} = \text{Max.}, f = \text{Max.},$ Outputs Open Mil. Com'l.	—	120 100	—	120 n/a	mA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE}_1, \overline{CE}_2 \geq V_{IH},$ $V_{CC} = \text{Max.},$ $f = \text{Max.},$ Outputs Open Mil. Com'l.	—	40 35	—	40 n/a	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE}_1, \overline{CE}_2 \geq V_{HC},$ $V_{CC} = \text{Max.},$ $f = 0,$ Outputs Open, $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$ Mil. Com'l.	—	20 15	—	1.0 n/a	mA

n/a = Not Applicable

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DATA RETENTION CHARACTERISTICS (P4C1981L/1982L Military Temperature Only)

Symbol	Parameter	Test Condition	Min	Typ.* $V_{CC} =$		Max $V_{CC} =$		Unit
				2.0V	3.0V	2.0V	3.0V	
V_{DR}	V_{CC} for Data Retention		2.0					V
I_{CCDR}	Data Retention Current			10	15	600	900	μA
t_{CDR}	Chip Deselect to Data Retention Time	\overline{CE}_1 or $\overline{CE}_2 \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or	0					ns
t_R^\dagger	Operation Recovery Time	$V_{IN} \leq 0.2V$	t_{RC}^\S					ns

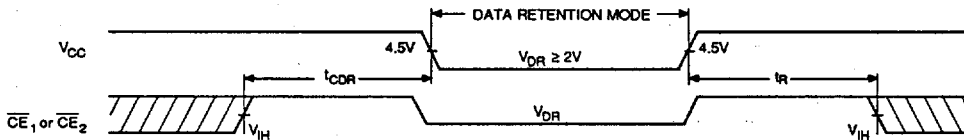
* $T_A = +25^\circ\text{C}$

t_{RC}^\S = Read Cycle Time

† This parameter is guaranteed but not tested.

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DATA RETENTION WAVEFORM



1534 03

AC CHARACTERISTICS—READ CYCLE

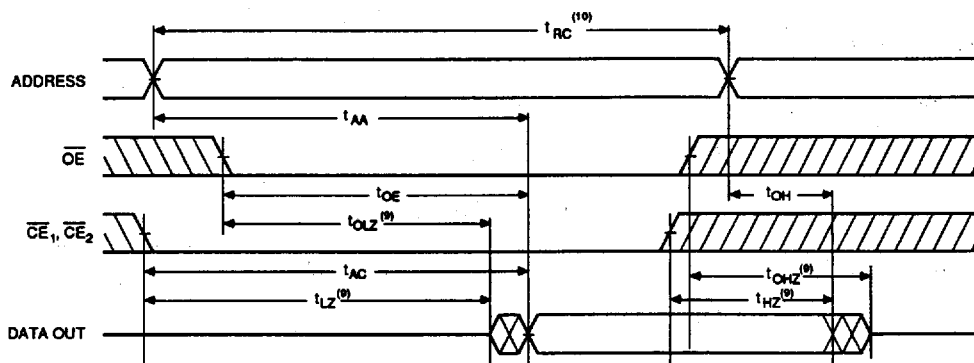
($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

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Sym.	Parameter	-12		-15		-20		-25		-35		-45		-55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	12		15		20		25		35		45		55		ns
t_{AA}	Address Access Time		12		15		20		25		35		45		55	ns
t_{AC}	Chip Enable Access Time		12		15		20		25		35		45		55	ns
t_{OH}	Output Hold from Address Change	1		2		3		3		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		2		2		3		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		6		7		10		10		15		15		20	ns
t_{OE}	Output Enable Low to Data Valid		7		9		12		15		21		27		35	ns
t_{OLZ}	Output Enable to Output in Low Z	2		2		2		2		3		3		3		ns
t_{OHZ}	Output Disable to Output in High Z		6		6		8		10		14		15		20	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		0		0		ns
t_{PD}	Chip Disable to Pwr Down Time		12		15		20		25		25		30		30	ns

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READ CYCLE NO.1 (OE controlled)⁽⁴⁾



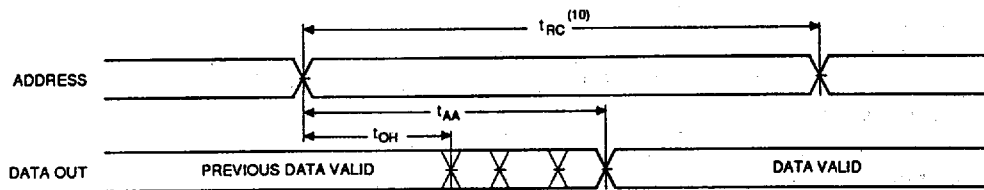
1534 04

Notes:

5. \overline{WE} is HIGH for READ cycle.
6. \overline{CE}_1 , \overline{CE}_2 and \overline{OE} are LOW for READ cycle.
7. \overline{OE} is LOW for the cycle.
8. ADDRESS must be valid prior to, or coincident with, \overline{CE}_1 , and \overline{CE}_2 transition LOW.
9. Transition is measured $\pm 200mV$ from steady state voltage prior to change, with loading as specified in Figure 1.
10. Read Cycle Time is measured from the last valid address to the first transitioning address.

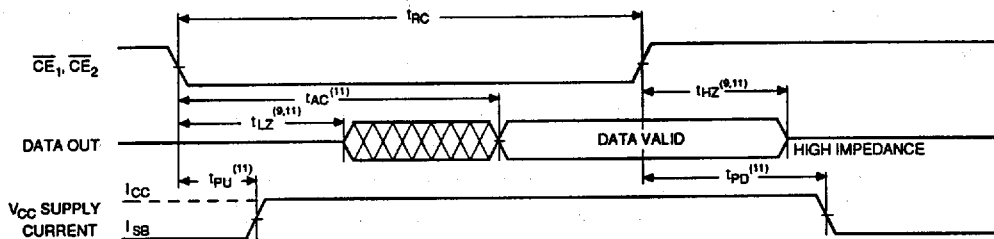
READ CYCLE NO.2 (ADDRESS controlled) (6,9)

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READ CYCLE NO.3 (\overline{CE}_1 , \overline{CE}_2 controlled) (6,7,9)



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Note:
 11. Transitions caused by a chip enable control have similar delays
 irrespective of whether \overline{CE}_1 or \overline{CE}_2 causes them.

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AC ELECTRICAL CHARACTERISTICS—WRITE CYCLE

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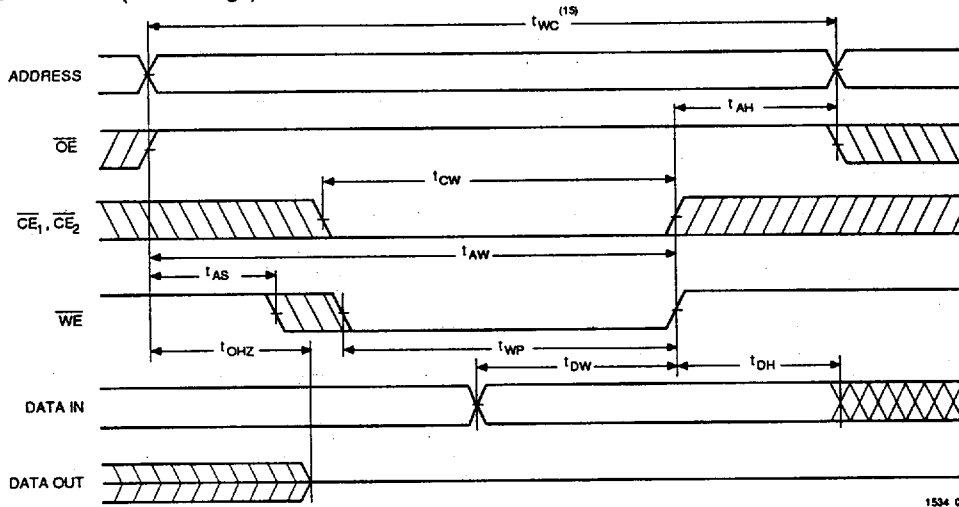
($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

Sym.	Parameter	-12		-15		-20		-25		-35		-45		-55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	12		13		15		20		30		40		50		ns
t_{CW}	Chip Enable Time to End of Write	8		10		15		20		30		35		40		ns
t_{AW}	Address Valid to End of Write	8		10		15		20		25		35		40		ns
t_{AS}	Address Set-up Time	0		0		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	9		10		15		20		25		35		40		ns
t_{AH}	Address Hold Time From End Of Write	0		0		0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	6		7		10		13		15		20		25		ns
t_{DH}	Data Hold Time	0		0		0		0		0		3		5		ns
t_{WZ}	Write Enable to Output in High Z (P4C1982)		6		7		8		10		10		15		20	ns
t_{OW}	Output Active from End of Write (P4C1982)	2		2		2		2		3		3		3		ns
t_{AWE}	Write Enable to Data-out Valid (P4C1981)		12		13		18		20		30		35		40	ns
t_{ADV}	Data-in Valid to Data-out Valid (P4C1981)		12		13		18		20		30		35		40	ns

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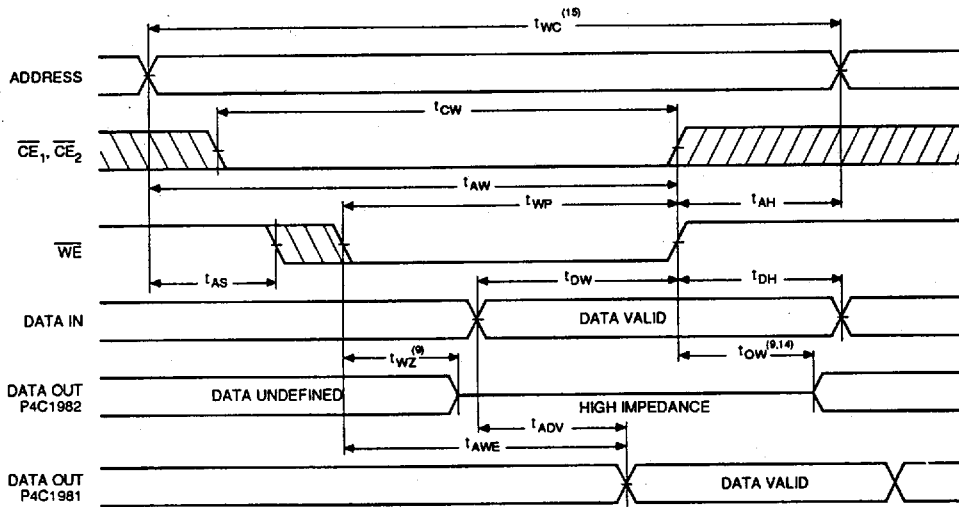
WRITE CYCLE NO. 1 (With \overline{OE} high)



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WRITE CYCLE NO. 2 (\overline{WE} CONTROLLED) (12,13)



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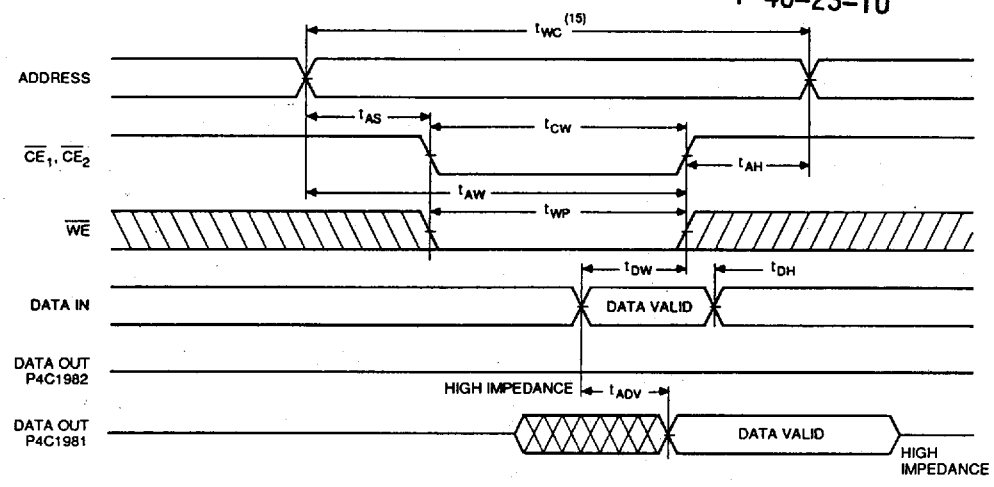
Notes:

- 12. \overline{CE}_1 , \overline{CE}_2 , and \overline{WE} must be LOW for WRITE cycle.
- 13. \overline{OE} is LOW for this WRITE cycle.
- 14. If \overline{CE}_1 or \overline{CE}_2 goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high impedance state.

- 15. Write Cycle Time is measured from the last valid address to the first transitioning address.

WRITE CYCLE NO. 3 ($\overline{CE}_1, \overline{CE}_2$ CONTROLLED) (11,12)

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

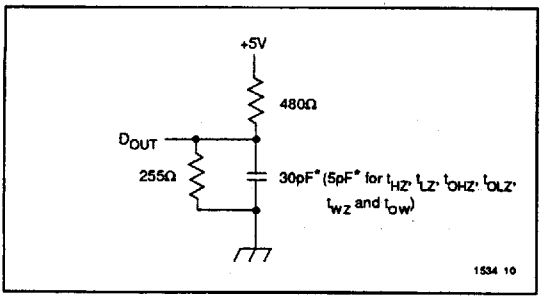
1534 TH 12

TRUTH TABLE

P4C1981/L (P4C1982/L)

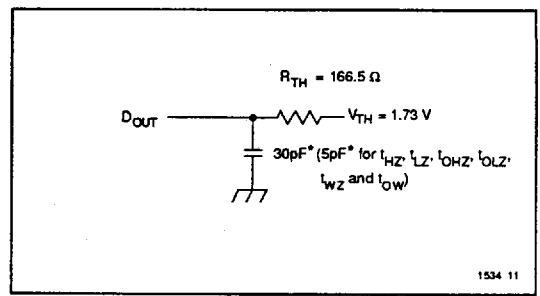
\overline{CE}_1	\overline{CE}_2	\overline{WE}	\overline{OE}	Mode	Output
H	X	X	X	Standby	High Z
X	H	X	X	Standby	High Z
L	L	H	H	Output Inhibit	High Z
L	L	H	L	READ	D_{OUT}
L	L	L	H	WRITE	High Z
L	L	L	L	WRITE	D_{IN} (High Z)

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Figure 1. Output Load



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Figure 2. Thevenin Equivalent

* including scope and test fixture.

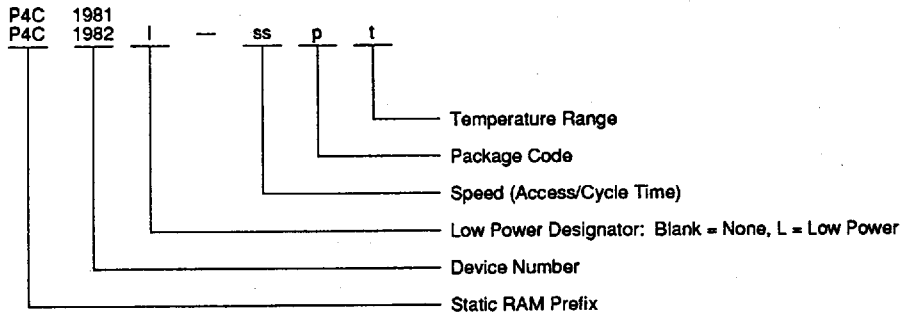
Note:

Because of the ultra-high speed of the P4C1981/L and P4C1982/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 μ F high frequency capacitor is also required between

V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50 Ω test environment should be terminated into a 50 Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116 Ω resistor must be used in series with D_{OUT} to match 166 Ω (Thevenin Resistance).

ORDERING INFORMATION

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- 1 = Ultra-low standby power designator L, if needed.
- ss = Speed (access/cycle time in ns), e.g., 25, 35
- p = Package code, i.e., P, J, D, L.
- t = Temperature range, i.e., C, M, MB.

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PACKAGE SUFFIX

Package Suffix	Description
P	Plastic DIP, 300 mil wide standard
J	Plastic SOJ, 300 mil wide standard
C	Sidebrazed DIP, 300 mil wide
L	Leadless Chip Carrier (ceramic)
D	CERDIP, 300 mil wide standard

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TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C to +70°C.
M	Military Temperature Range, -55°C to +125°C.
MB	Mil. Temp. with MIL-STD-883D Class B compliance

1534 TR 15

SELECTION GUIDE

The P4C1981 and P4C1982 are available in the following temperature, speed and package options. The P4C1981L and P4C1982L are only available with access times of 25 ns and slower for military temperatures.

Temperature Range	Package	Speed (ns)						
		12	15	20	25	35	45	55
Commercial	Plastic DIP	-12PC	-15PC	-20PC	-25PC	N/A	N/A	N/A
	Plastic SOJ	-12JC	-15JC	-20JC	-25JC	N/A	N/A	N/A
	CERDIP	-12DC	-15DC	-20DC	-25DC	N/A	N/A	N/A
	LCC	-12LC	-15LC	-20LC	-25LC	N/A	N/A	N/A
Military Temp.	CERDIP	N/A	N/A	-20DM	-25DM	-35DM	-45DM	-55DM
	LCC	N/A	N/A	-20LM	-25LM	-35LM	-45LM	-55LM
Military Processed*	CERDIP	N/A	N/A	-20DMB	-25DMB	-35DMB	-45DMB	-55DMB
	LCC	N/A	N/A	-20LMB	-25LMB	-35LMB	-45LMB	-55LMB

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* Military temperature range with MIL-STD-883 Revision D, Class B processing.
N/A = Not available