16-bit arithmetic logic unit

L429C01

general information

The L429C01 is designed as a high performance, 16-bit Arithmetic Logic Unit slices. It incorporates functions previously requiring a large number of bipolar bit slice, register, and ancillary functions into a single VLSI device. While containing many advanced features, the LOGIC L429C01 is designed to be downward compatible with existing bipolar designs. This is achieved by maintaining instruction compatibility at the microcode level to allow direct use of previously developed algorithms, while offering additional features for new designs.

As shown in the functional diagram in figure 1, the L429C01 consists of functions equivalent to four Am2901 bit slice ALU's and an Am2902 carry lookahead unit, as well as on-chip pipeline registers for all control and data inputs, in a single 64-pin device. All Status, Shift linkage, and Carry functions are fully cascadable to allow construction of 16-bit, 32-bit, or larger architectures. A detailed block diagram of the L429C01 is shown in figure 2. This configuration is useful in designs which register the D input externally to reduce effective D-port set-up time.

Compatibility with AMD Products. The L429C01 is designed to allow application of state of the art levels of integration to both new products and existing designs. They support updating of previous generations of bipolar designs by recasting existing functions in a higher level of integration, while maintaining full functional and software compatibility.

One of the differences between the LOGIC L429C01 and the older bipolar systems concerns the fact that all instruction and control inputs are latched at the rising edge of the clock. This relieves the designer of the need for external pipeline registers at the control PROM outputs.

features

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- **4 wide Am2901 ALU in a single package**
- **On-chip carry lookahead unit**
- **Full 16-bit data paths**
- **Low-power CMOS technology**
- **On-chip pipeline registers for all control inputs**
- **10 MHz military, 12 MHz commercial cycle time (16-bit machine)**
- **Fully software compatible with existing bipolar 2901 designs**

In addition to the control inputs, the D-port data lines D_0-D_{15} are latched internal to the L429C01. This alleviates the necessity for a pipeline register external to the ALU which is usually necessary to prevent excessively long D-port set-up times.

functional diagram

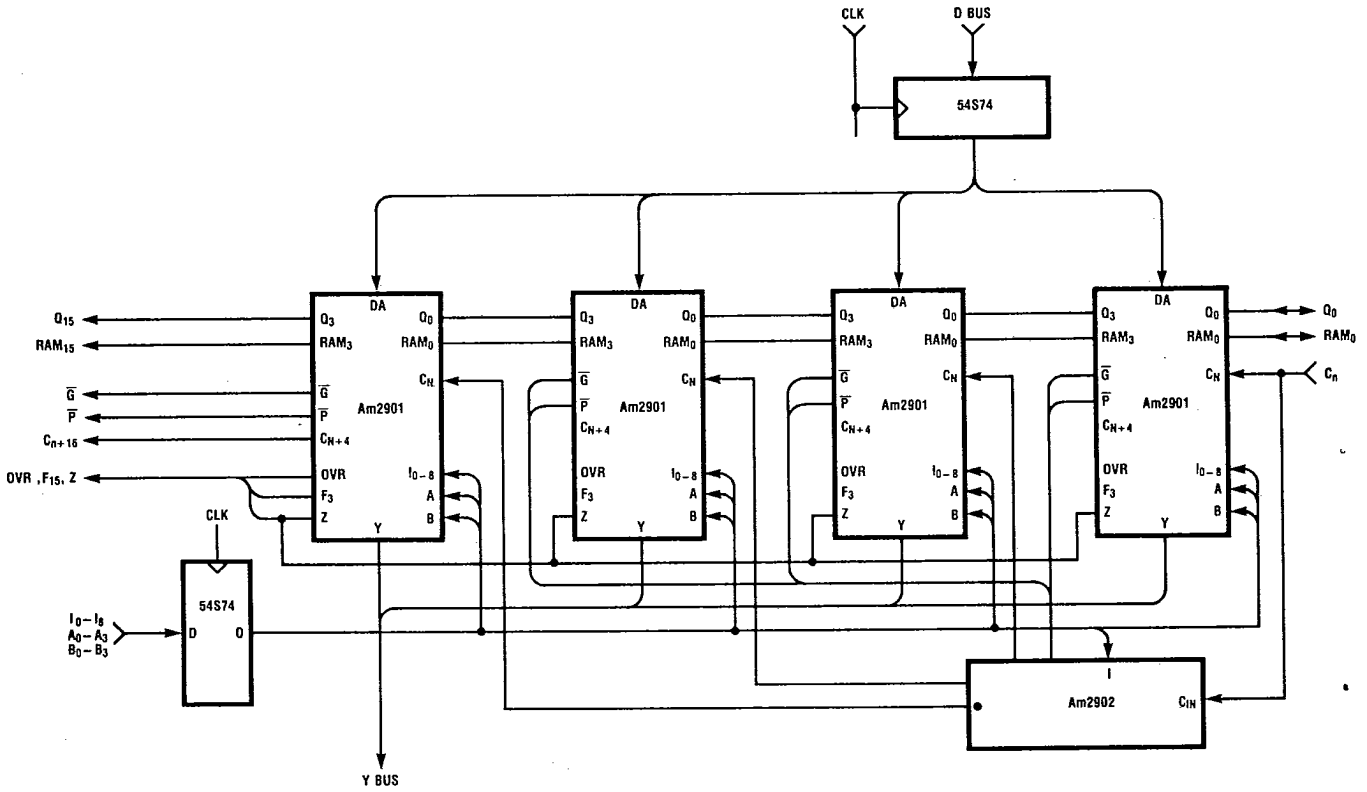

FIGURE 1

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general info con't.

The L429C01 has been designed to accomodate multiplexing of the B address inputs directly. This feature accomodates systems in which the Write address is generated independently and may differ from the B Read address on a given cycle (3 address architectures.) This is accomplished by an external multiplexer arranged so as to apply the Read and Write addresses sequentially during the appropriate portions of the clock cycle.

In the L429C01 device, the B address inputs are internally applied to two edge triggered D-type registers. One of these, the RAM write address register, is clocked on the falling edge of the clock input. The other register, containing the B-port read address, is clocked on the rising edge of the clock input.

pin configuration

PIN	FUNCTION
I_0-I_2	ALU Operand Select (= Am2901 I_0-I_2)
I_3-I_5	ALU Function Select (= Am2901 I_3-I_5)
I_6-I_8	RAM, Q Shifter, Y Port Control (= Am2901 I_6-I_8)
A_0-A_3	A-Port Address
B_0-B_3	B-Port Address
D_0-D_{15}	D-Port Data Lines
Y_0-Y_{15}	Y-Port Data Lines
RAM_0, RAM_{15}	Serial RAM Shift I/O Lines
Q_0, Q_{15}	Serial Q-Register Shift I/O Lines
C_n, C_{n+16}	Carry In, Carry Out
$\overline{P}$, $\overline{G}$	Block Carry Propagate, Generate
F_{15}	Function Generator MSB (Sign)
OVR	Function Generator Overflow Detect
Z	F = 0
$\overline{OE}_Y$	Y-Port Three-State Control
CLK	Clock
V_{CC}, GND	Power Supply

detailed block diagram

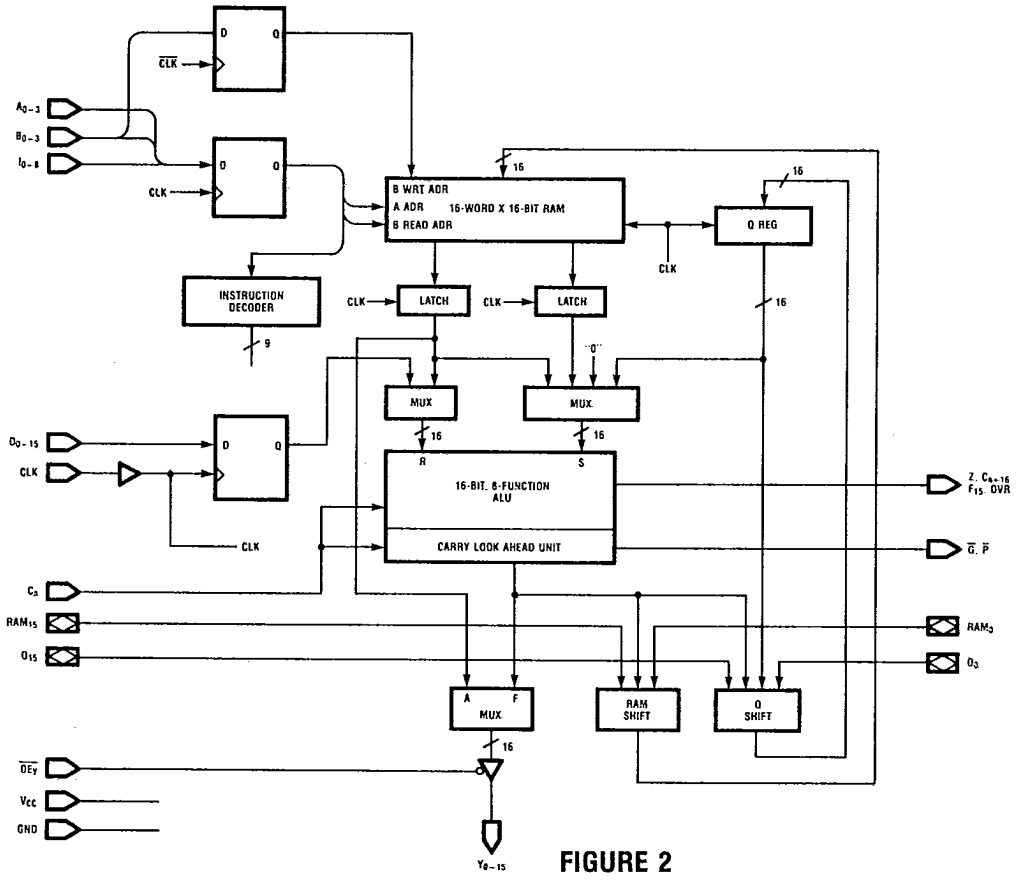

FIGURE 2

pin configuration

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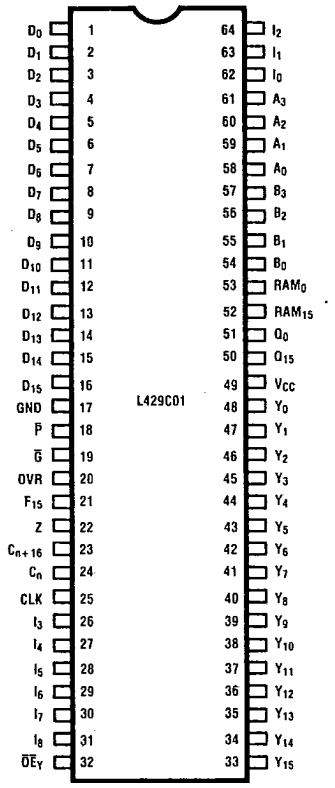
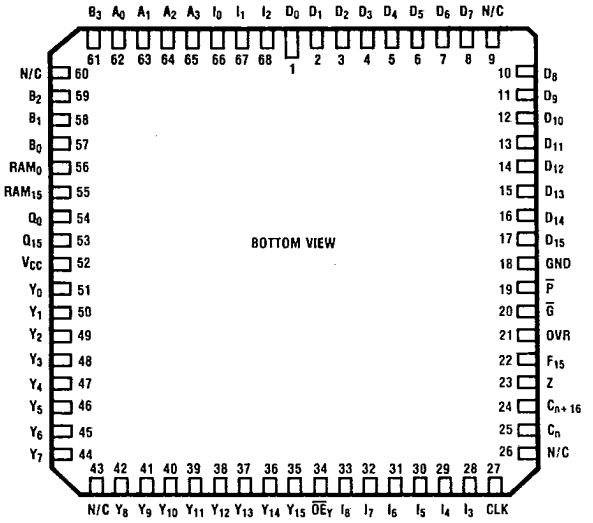


NOTE: PIN 1 IS MARKED FOR IDENTIFICATION.



(See page 133 for additional pinout information.)

L429C01 architecture

Operand Source Control

The L429C01 arithmetic element maintains complete instruction compatibility with Am2901 type devices. The RAM has a capacity of 16 words of 16 bits each. The RAM A-port address specifies the register to be read from the A-port, and the B-port address specifies the register to be read from the B-port, as well as the location to be written. The RAM A data is latched while the clock input is low, and is input to the ALU data source selector, as well as to the Y-port multiplexer. The B data is similarly latched, and is also a source for the ALU data source selector. Additional inputs to the selector include the D-port, the Q register, and logic "0." Table 1 shows the effective ALU source operands for all combinations of the source selector control input I_0–I_2. Control inputs I_0–I_2 perform identical functions to the I_0–I_2 pins on the Am2901 device.

ALU Operation

The ALU section performs the functions described in Table 2. The control inputs I_3–I_5 select between three arithmetic and five logical operations to be performed on the input operands. The I_3–I_5 lines perform the identical function to the I_3–I_5 lines of the Am2901. The four stages of the ALU have integral carry lookahead circuitry across 16 bits for high-speed operation. This circuitry is functionally equivalent to the Am2902 carry lookahead unit.

ALU Result Destination Control

The ALU result data destination is controlled by the I_6–I_8 inputs. The ALU result is denoted F_0–F_{15}, and may be routed to any of several destinations: The F_0–F_{15} data may be presented at the Y port of the L429C01 by enabling the Y three-state output. This output is controlled via the $\overline{OE}_Y$ input. A second destination for the ALU data is the internal RAM. F_0–F_{15} may be written to the RAM location indicated by the B address, either in its original format or shifted up or down one position. RAM data shifting is also controlled by the I_6–I_8 inputs. The final destination for ALU data is the Q register. Used primarily for microcoded multiplication and division algorithms, the Q register may be loaded in parallel with other destinations. Like the RAM, the Q input data may also be shifted under the control of the I_6–I_8 inputs. Table 3 gives the various shift actions and data destinations under control of the I_6–I_8 inputs. Fill data for RAM and Q shift operations is obtained from the RAM_0, RAM_{15}, Q_0, and Q_{15} I/O lines. These pins also provide access to data shifted out of the device. The state of these four device pins (input or output) and the data present on them is also shown in Table 3.

16-bit arithmetic logic unit

source operands and ALU functions

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The ALU is capable of performing five logic functions and three arithmetic functions. I_3, I_4 and I_5 controls the function to be performed on the selected operand(s). A total of eight operand pairs can be selected via the I_0, I_1 and I_2 microinstruction bits.

In the arithmetic mode, the ALU result is also determined by the Carry In (C_n) input. When doing the logic functions, the ALU does not care about C_n. Tables 5 and 6 show the detailed ALU's logic and arithmetic functions along with the operands selected.

function tables

Table 1. ALU Source Operand Control

MNEMONIC	MICRO CODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	OCTAL CODE	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Table 2. ALU Function Control

MNEMONIC	MICRO CODE				ALU FUNCTION	SYMBOL
	I_5	I_4	I_3	OCTAL CODE		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R∨S
AND	H	L	L	4	R AND S	R∧S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$∧S
EXOR	H	H	L	6	R EX-OR S	R⊻S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R⊻S}$

Table 3. ALU Destination Control

MNEMONIC	MICRO CODE				RAM FUNCTION		Q–REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
	I_8	I_7	I_6	OCTAL CODE	SHIFT	LOAD	SHIFT	LOAD		RAM_0	RAM_{15}	Q_0	Q_{15}
QREG	L	L	L	0	Z	None	None	F→Q	F	Z	Z	Z	Z
NOP	L	L	H	1	Z	None	Z	None	F	Z	Z	Z	Z
RAMA	L	H	L	2	None	F→B	Z	None	A	Z	Z	Z	Z
RAMF	L	H	H	3	None	F→B	Z	None	F	Z	Z	Z	Z
RAMQD	H	L	L	4	Down	F/2→B	Down	Q/2→Q	F	F_0	IN_{15}	Q_0	IN_{15}
RAMD	H	L	H	5	Down	F/2→B	Z	None	F	F_0	IN_{15}	Q_0	Z
RAMQU	H	H	L	6	Up	2F→B	Up	2Q→Q	F	IN_0	F_{15}	IN_0	Q_{15}
RAMU	H	H	H	7	Up	2F→B	Z	None	F	IN_0	F_{15}	Z	Q_{15}

B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.
Z = High-impedance state.
+ = Plus
− = Minus
∨ = OR
∧ = AND
⊻ = EX OR

function tables

Table 4. Source Operand and ALU Function Matrix

I_{543} OCTAL	ALU FUNCTION	I_{210} OCTAL 0	1	2	3	4	5	6	7
		ALU Source Operands							
		A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L R Plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	− D − 1 − D
2	C_n = L R Minus S C_n = H	A − Q − 1 A − Q	A − B − 1 A − B	− Q − 1 − Q	− B − 1 − B	− A − 1 − A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	A∨Q	A∨B	Q	B	A	D∨A	D∨Q	D
4	R AND S	A∧Q	A∧B	0	0	0	D∧A	D∧Q	0
5	$\overline{R}$ AND S	$\overline{A}$∧Q	$\overline{A}$∧B	Q	B	A	$\overline{D}$∧A	$\overline{D}$∧Q	0
6	R EX-OR S	A∀Q	A∀B	Q	B	A	D∀A	D∀Q	D
7	R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

Table 5. ALU Logic Mode Functions

OCTAL I_{543}	OCTAL I_{210}	GROUP	FUNCTION
4	0	AND	A∧Q
4	1		A∧B
4	5		D∧A
4	6		D∧Q
3	0	OR	A∨Q
3	1		A∨B
3	5		D∨A
3	6		D∨Q
6	0	EX−OR	A∀Q
6	1		A∀B
6	5		D∀A
6	6		D∀Q
7	0	EX−NOR	$\overline{A \forall Q}$
7	1		$\overline{A \forall B}$
7	5		$\overline{D \forall A}$
7	6		$\overline{D \forall Q}$
7	2	INVERT	$\overline{Q}$
7	3		$\overline{B}$
7	4		$\overline{A}$
7	7		$\overline{D}$
6	2	PASS	Q
6	3		B
6	4		A
6	7		D
3	2	PASS	Q
3	3		B
3	4		A
3	7		D
4	2	"ZERO"	0
4	3		0
4	4		0
4	7		0
5	0	MASK	$\overline{A}$∧Q
5	1		$\overline{A}$∧B
5	5		$\overline{D}$∧A
5	6		$\overline{D}$∧Q

Table 6. ALU Arithmetic Mode Functions

OCTAL I_{543}	OCTAL I_{210}	C_n = L GROUP	C_n = L FUNCTION	C_n = H GROUP	C_n = H FUNCTION
0	0	ADD	A + Q	ADD plus one	A + Q + 1
0	1		A + B		A + B + 1
0	5		D + A		D + A + 1
0	6		D + Q		D + Q + 1
0	2	PASS	Q	Increment	Q + 1
0	3		B		B + 1
0	4		A		A + 1
0	7		D		D + 1
1	2	Decrement	Q − 1	PASS	Q
1	3		B − 1		B
1	4		A − 1		A
2	7		D − 1		D
2	2	1's Comp.	− Q − 1	2's Comp. (Negate)	− Q
2	3		− B − 1		− B
2	4		− A − 1		− A
1	7		− D − 1		− D
1	0	Subtract (1's Comp)	Q − A − 1	Subtract (2's Comp)	Q − A
1	1		B − A − 1		B − A
1	5		A − D − 1		A − D
1	6		Q − D − 1		Q − D
2	0		A − Q − 1		A − Q
2	1		A − B − 1		A − B
2	5		D − A − 1		D − A
2	6		D − Q − 1		D − Q

logic functions

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G, P, C_{n+16} and OVR

The four signals G, P, C_{n+16} and OVR indicate the carry and overflow conditions when the L429C01 is doing addition or subtraction. Table 7 shows the logic expressions for the signals associated with the three ALU arithmetic functions.

function tables

Table 7. Logic Expressions for Carry and Overflow Conditions

I_{543}	FUNCTION	$\overline{P}$	$\overline{G}$	$C_n + 16$	OVR
0	R + S	$\overline{P_{0\text{-}15}}$	$\overline{G_{15} + P_{15}G_{14} + P_{15}P_{14}G_{13} + \ldots + P_{1\text{-}15}G_0}$	C_{16}	$C_{16} \forall C_{15}$
1	S − R	Same as R + S Equations, but Substitute $\overline{R}_i$ for R_i in Definitions			
2	R − S	Same as R + S Equations, but Substitute $\overline{S}_i$ for S_i in Definitions			

Definition: + = OR

$P_{0\text{-}15} = P_{15}P_{14}P_{13}P_{12}P_{11}P_{10}P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$

$P_0 = R_0 + S_0$

$P_1 = R_1 + S_1$

$P_2 = R_2 + S_2$

$P_3 = R_3 + S_3$, etc.

$G_{0\text{-}15} = G_{15}G_{14}G_{13}G_{12}G_{11}G_{10}G_9G_8G_7G_6G_5G_4G_3G_2G_1G_0$

$G_0 = R_0S_0$

$G_1 = R_1S_1$

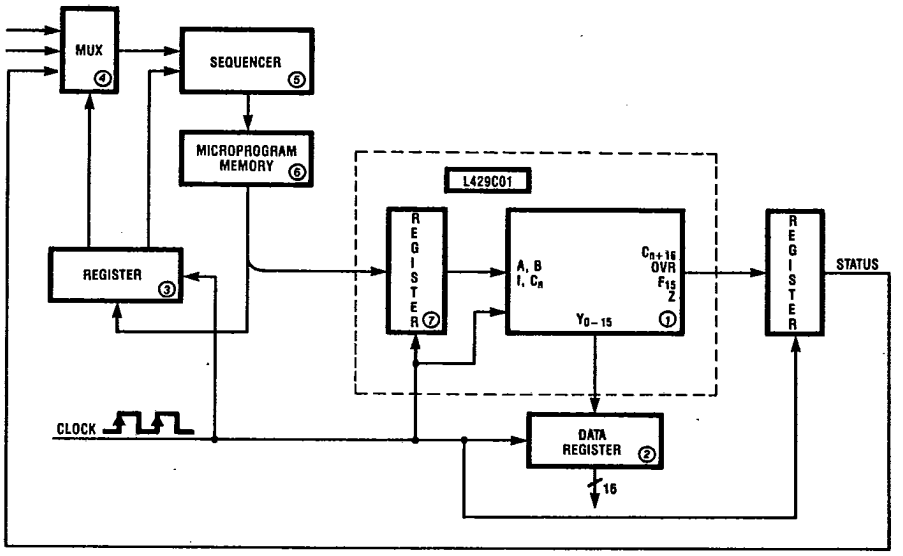
$G_2 = R_2S_2$

$G_3 = R_3S_3$, etc.

$C_{16} = G_{15} + P_{15}G_{14} + P_{15}G_{14} + P_{15}P_{14}G_{13} + \ldots + P_{0\text{-}15}C_n$

$C_{15} = G_{14} + P_{14}G_{13} + P_{14}P_{13}G_{12} + \ldots + P_{0\text{-}14}C_n$

MINIMUM CYCLE TIME CALCULATIONS FOR TYPICAL L429C01-BASED SYSTEM



DATA LOOP		
⑦ TO ① L429C01	CLOCK TO Y OUTPUT	90
② REGISTER	SET-UP TIME	3
		93 ns.

CONTROL LOOP		
③ REGISTER	CLOCK TO OUTPUT	11
④ MUX	SELECT TO OUTPUT	10.5
⑤ SEQUENCER	CONDITION CODE TO OUTPUT	30
⑥ PROM	ACCESS TIME	40
⑦ L429C01	A, B, I, C_n SET-UP TIME	6
		97.5 ns.

switching characteristics

I. L429C01 Guaranteed Performance—Commercial Range

A. Cycle time and clock characteristics

READ-MODIFY-WRITE CYCLE (FROM SELECTION OF A, B REGISTERS TO END OF CYCLE)	
Maximum Clock Frequency to Shift Q (50% Duty Cycle, I = 432 or 632)	
Minimum Clock Low Time	30
Minimum Clock High Time	45
Minimum Clock Period	75

B. Combinational propagation delays

FROM INPUT \ TO OUTPUT	Y	F_{15}	C_{n+16}	$\overline{G}$, $\overline{P}$	Z (F = 0)	OVR	RAM_0 RAM_{15}	Q_0 Q_{15}	UNITS
A, B Address	Address is Registered on the Clock's Rising Edge								ns
D	D Input is Registered on the Clock's Rising Edge								
C_n	40	30	20		32	28			
$I_0 - I_8$	Instruction is Registered on the Clock's Rising Edge								
A Bypass ALU (I = 2XX)	55								
Clock ⎍	90	80	74	70	84	78	80	28	

C. Set-up and hold times relative to clock (CLK) input

INPUT	CP: SET-UP TIME H→L	HOLD TIME H→L	SET-UP TIME L→H	HOLD TIME L→H	UNITS
A, B Source Address			6	4	ns
B Destination Address	6	4			
D			6	4	
C_n			22	0	
$I_0 - I_8$			6	4	
$RAM_{0,15}$ $Q_{0,15}$			18	0	

D. Output enable/disable times

$\overline{OE}_Y$ Low to Y Output Enable	20
$\overline{OE}_Y$ High to Y Output Disable	18

AC Test Conditions

Inputs: switched between 0V and 3V at 1 V/ns. All measurements made at 1.5V.

Outputs 510 ohms to +5V, 750 ohms to GND., 60 pF to GND.

II. L429C01 Guaranteed Performance—Military Range

A. Cycle time and clock characteristics

READ—MODIFY—WRITE CYCLE (FROM SELECTION OF A, B REGISTERS TO END OF CYCLE)	
Maximum Clock Frequency to Shift Q (50% Duty Cycle, I = 432 or 632)	
Minimum Clock Low Time	30
Minimum Clock High Time	45
Minimum Clock Period	75

B. Combinational propagation delays

FROM INPUT \ TO OUTPUT	Y	F_{15}	C_{n+16}	$\overline{G}$, $\overline{P}$	Z (F = 0)	OVR	RAM_0 RAM_{15}	Q_0 Q_{15}	UNITS
A, B Address	Address is Registered on the Clock's Rising Edge								ns
D	D Input is Registered on the Clocks Rising Edge								
C_n	45	32	24		36	32			
$I_0 - I_8$	Instruction is Registered on the Clock's Rising Edge								
A Bypass ALU (I = 2XX)	65								
Clock ⎍	105	92	84	82	94	88	90	32	

C. Set-up and hold times relative to clock (CLK) input

INPUT	CP: SET-UP TIME H→L	HOLD TIME H→L	SET-UP TIME L→H	HOLD TIME L→H	UNITS
A, B Source Address			8	4	ns
B Destination Address	8	4			
D			8	4	
C_n			25	0	
$I_0 - I_8$			8	4	
$RAM_{0,15}$, $Q_{0,15}$			20	0	

D. Output enable/disable times

$\overline{OE}_Y$ Low to Y Output Enable	22
$\overline{OE}_Y$ High to Y Output Disable	20

AC Test Conditions

Inputs: switched between 0V and 3V at 1V/ns. All measurements made at 1.5V.

Outputs load: 510 ohms to +5V, 750 ohms to GND., 60 pF to GND.

16-bit arithmetic logic unit

absolute maximum ratings

Supply Voltage	−0.5V to 7.0V
Input Voltage	0V to 5.5V
Output Voltage	0V to 5.5V
Operating Temperature (Ambient)	−55°C to 125°C
Storage Temperature	−65°C to 150°C

ordering information

ORDERING CODE	SPEED	PACKAGE TYPE	OPERATING RANGE
L429C01 PC	12 MHz	P4	COMMERCIAL
DC		D4	
GC		G1	
KC		K3	
PCR		P4	
DCR		D4	
GCR		G1	
L429C01 DM	10 MHz	D4	MILITARY
DME		D4	
KMB		K3	

recommended operating conditions

PARAMETER	DESCRIPTION		min	typ	max	unit
V_{CC}	Supply Voltage	Commercial	4.75	5.0	5.25	V
		Military	4.50	5.0	5.5	V
I_{OL}	Low Level Output Current		8.0			mA
I_{OH}	High Level Output Current		−2.0			mA
T_{AMB}	Operating Temperature	Commercial	0	25	70	°C
		Military	−55	25	125	°C

electrical characteristics

PARAMETER	DESCRIPTION		min	typ	max	unit
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{OL}	Low Level Output Voltage (I_{OL} = 8 mA)				0.5	V
V_{OH}	High Level Output Voltage (I_{OH} = −2 mA)		3.5			V
I_{IL}	Low Level Input Current (V_{IL} = 0.4 V)				10	μA
I_{IH}	High Level Input Current (V_{IH} = 2.4 V)				10	μA
I_{OZ}	Output Current (High-Impedance State)					μA
I_{CC}	Supply Current	(Quiescent)			0.5	mA
		(Dynamic)		10[1]	30[2]	mA

1) Typical I_{CC} conditions: 5 MHz clock rate, V_{IH} = 2.4V, V_{IL} = 0.4V, V_{CC} = 5V, T_A = 25°C, random input patterns
2) Maximum I_{CC} conditions: 5 MHz clock rate, V_{IH} = 2.0V, V_{IL} = 0.8V, V_{CC} = 5.5V, T_A = −55°C, all outputs toggling every cycle

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