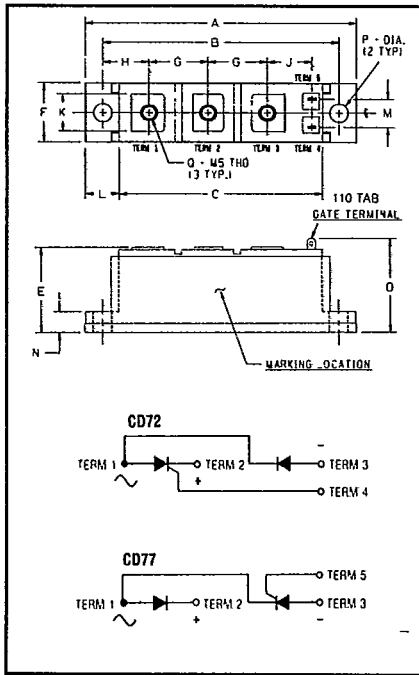




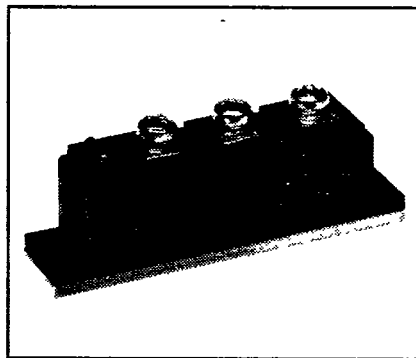
CD72 ___ 60 ___
 CD77 ___ 60 ___

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**Current Source Inverter
 POW-R-BLOK™ Modules
 60 Amperes/100-1200 Volts**



100-1200 Volts CD72 ___ 60 ___
 CD77 ___ 60 ___
Outline Drawing



CD72 ___ 60 ___
 CD77 ___ 60 ___
**Current Source Inverter
 POW-R-BLOK™ Modules
 60 Amperes/100-1200 Volts**

Ordering Information

Example: Select the complete ten digit rating module part number you desire from the table — i.e. CD7212600Z is a 1200 Volt, 60 Ampere SCR with a 2400 Volt Series Diode Current Source Inverter POW-R-BLOK™ Module.

Type	SCR V _{RRM} Volts (x100)	Current Rating Amperes (60)	Diode V _{RRM} Volts (1.7 X SCR V _{RRM}) (2.0 X SCR V _{RRM})
CD72	01	60	OY
CD77	02		OZ
	04		
	06		
	08		
	10		
	12		

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	3.602	3.640	91.49	92.45
B	3.146	3.154	79.91	80.11
C	2.705	2.735	68.71	69.47
D	1.24	1.28	31.50	32.51
E	1.125	1.165	28.58	29.59
F	.795	.805	20.19	20.45
G	.788	.798	19.76	20.27
H	.608	.628	15.44	15.95
J	.585	.605	14.86	15.36
K	.480	.520	12.19	13.21
L	.43	.47	10.92	11.94
M	.36	.40	9.14	10.16
N	.265	.285	6.73	7.24
P	.245	.255	6.22	6.48
Q	—	—	M5 x 0.8	

Description

Powerex POW-R-BLOK™ Modules combine multiple power semiconductor devices in a single, electrically isolated module. This dense, cost-effective packaging is made possible by Powerex's proprietary *glass passivation* process, in which each semiconductor junction is sealed with a protective layer of glass. Exhaustive testing at high voltages and high temperatures has demonstrated the excellent parameter stability of these glass-protected products.

The POW-R-BLOK™ features a self-contained electrical isolation system. The use of BeO ceramic isolators with high thermal conductivity has achieved excellent circuit-to-baseplate isolation (≥2500 volts RMS), while maintaining efficient cooling of the semiconductors. Powerex Current Source Inverter Modules offer an SCR with up to 1200 volts blocking capability in series with a diode with up to 2400 volts blocking capability.

Features:

- Glass Passivated Chips
- Hybrid Construction
- Isolated Base Plate
- Low Thermal Impedance
- Metal Base Plate
- Quick Connect Gate Signal Terminals

Applications:

- ASCI Current Source Inverter AC Motor Drives

Benefits:

- No Additional Insulating Components Required
- Easy Installation
- Reduced Engineering Time
- Improved Heat Transfer
- Voltage Stability



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CD72 — 60 —, CD77 — 60 —

Current Source Inverter

POW-R-BLOK™ Modules

60 Amperes/100-1200 Volts

Absolute Maximum Ratings

Characteristics	Symbol	CD7201600Y/OZ CD7701600Y/OZ	CD7202600Y/OZ CD7702600Y/OZ	CD7204600Y/OZ CD7704600Y/OZ	CD7206600Y/OZ CD7706600Y/OZ	Units
SCR Peak Forward Blocking Voltage	V_{DRM}	100	200	400	600	Volts
SCR Peak Reverse Blocking Voltage	V_{RRM}	100	200	400	600	Volts
SCR Transient Peak Reverse Blocking Voltage (Non-Repetitive) $t < 5$ ms	V_{RSM}	200	300	500	700	Volts
Diode Peak Reverse Blocking Voltage	V_{RRM}	170/200	340/400	680/800	1020/1200	Volts

Characteristics	Symbol	CD7208600Y/OZ CD7708600Y/OZ	CD7210600Y/OZ CD7710600Y/OZ	CD7212600Y/OZ CD7712600Y/OZ	Units
SCR Peak Forward Blocking Voltage	V_{DRM}	800	1000	1200	Volts
SCR Peak Reverse Blocking Voltage	V_{RRM}	800	1000	1200	Volts
SCR Transient Peak Reverse Blocking Voltage (Non-Repetitive) $t < 5$ ms	V_{RSM}	950	1200	1450	Volts
Diode Peak Reverse Blocking Voltage	V_{RRM}	1360/1600	1700/2000	2040/2400	Volts

CD72 — 60 — CD77 — 60 —

RMS On-State Current	$I_{T(RMS)}$	125	Amperes
Average On-State Current	$I_{T(AV)}$	80	Amperes
Peak One-Cycle Surge (Non-Repetitive) On-State Current (60Hz)	I_{TSM}	1800	Amperes
Peak Three-Cycle Surge (Non-Repetitive) On-State Current (60Hz)	I_{TSM}, I_{FSM}	1300	Amperes
Peak Ten-Cycle Surge (Non-Repetitive) On-State Current (60Hz)	I_{TSM}, I_{FSM}	1170	Amperes
Peak One-Cycle Surge (Non-Repetitive) On-State Current (50Hz)	I_{TSM}	1640	Amperes
I^2t (for Fusing), 8.3 milliseconds	I^2t	13,500	A ² sec
Critical Rate-of-Rise of On-State Current ① (Non-Repetitive)	di/dt	800	Amperes/ μ s
Peak Gate Power Dissipation	P_{GM}	16	Watts
Average Gate Power Dissipation	$P_{G(AV)}$	3.0	Watts
Peak Forward Gate Voltage	V_{GFM}	10	Volts
Peak Reverse Gate Voltage	V_{GRM}	5.0	Volts
Peak Forward Gate Current	I_{GFM}	4.0	Amperes
Storage Temperature	T_{STG}	-40 to 150	°C
Operating Temperature	T_J	-40 to 125	°C
Maximum Mounting Torque M6 Mounting Screw	—	50	in.-lb.
Maximum Terminal Torque M5 Terminal Screw	—	35	in.-lb.
Module Weight (Typical)	—	142	Grams
V Isolation	V_{RMS}	2500	Volts

① Per JEDEC STD RS-397, 5.2.2.6.



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CD72 — 60 —, CD77 — 60 —

Current Source Inverter

POW-R-BLOK™ Modules

60 Amperes/100-1200 Volts

Electrical and Thermal Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified

Characteristics	Symbol	Test Conditions	CD72 — 60 — CD77 — 60 —	Units
Blocking State Maximums				
SCR Forward Leakage Current, Peak	I_{DRM}	$T_J = 125^\circ\text{C}$, $V_{DRM} = \text{rated}$	10	mA
SCR Reverse Leakage Current, Peak	I_{RRM}	$T_J = 125^\circ\text{C}$, $V_{RRM} = \text{rated}$	10	mA
Diode Reverse Leakage Current, Peak	I_{RRM}	$T_J = 125^\circ\text{C}$, $V_{RRM} = \text{rated}$	20	mA
Conducting State Maximums				
Peak On-State Voltage	V_{TM}	$I_{TM} = 250\text{A}$	1.75	Volts
Peak On-State Voltage	V_{FM}	$I_{FM} = 250\text{A}$	1.3	Volts
Switching Minimums				
Critical Rate of Rise of Off-State Voltage	dv/dt	$T_J = 125^\circ\text{C}$, Exponential to V_{DRM}	300	Volts/ μsec
Typical Turn-Off Time	t_q	$I_{TM} = 50\text{A}$, $T_J = 125^\circ\text{C}$, $di_F/dt = 5\text{A}/\mu\text{s}$ reapplied $dv/dt = 20\text{V}/\mu\text{s}$ linear to $0.8 V_{DRM}$	100	μsec
Typical Turn-On Time	t_{on}	$I_{TM} = 100\text{A}$, $V_D = 100\text{V}$	4	μsec
Thermal Maximums				
Thermal Resistance, Junction to Case	$R_{\theta JC}$	Per Device	0.28	$^\circ\text{C}/\text{Watt}$
Thermal Resistance, Case to Sink Lubricated	$R_{\theta CS}$	Per Device	0.2	$^\circ\text{C}/\text{Watt}$
Gate Parameters Maximums				
Gate Current to Trigger	I_{GT}	$V_D = 12\text{V}$	100	mA
Gate Voltage to Trigger	V_{GT}	$V_D = 12\text{V}$	3.0	Volts
Non-Triggering Gate Voltage	V_{GDM}	$T_J = 125^\circ\text{C}$, $V_D = V_{DRM}$	0.15	Volts

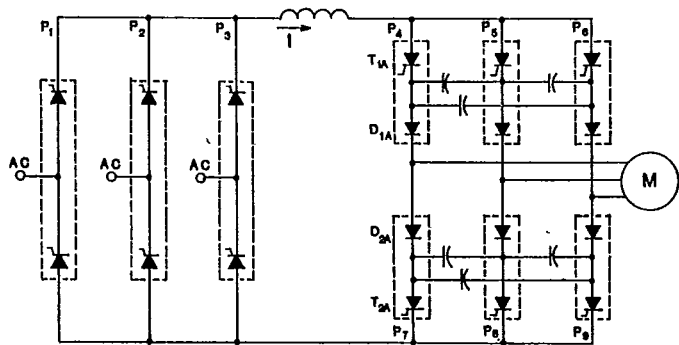
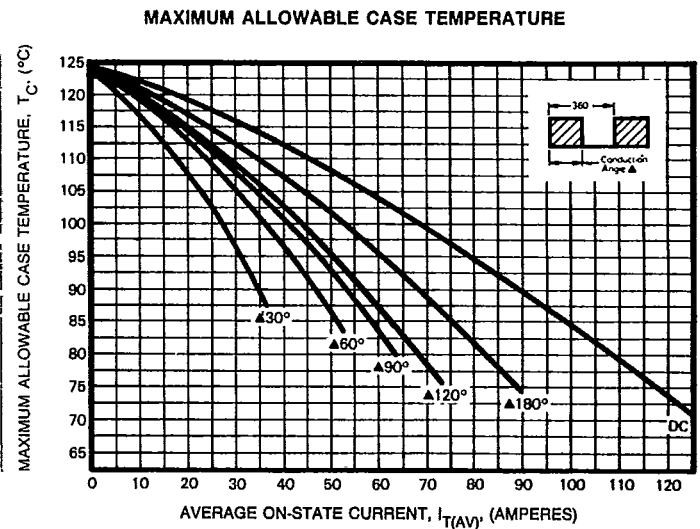
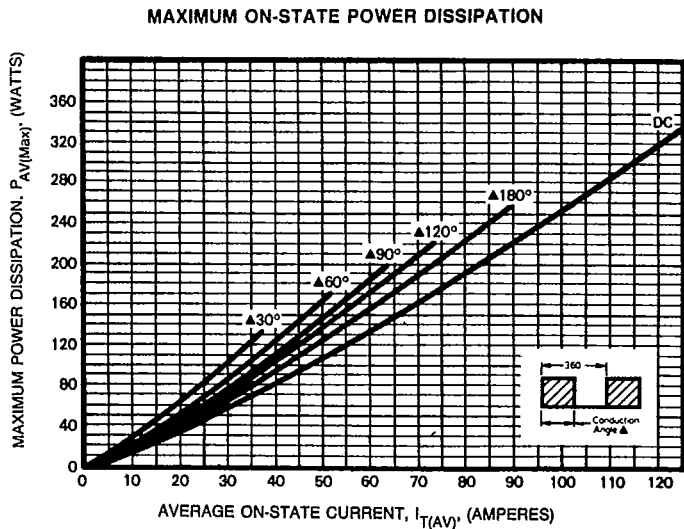
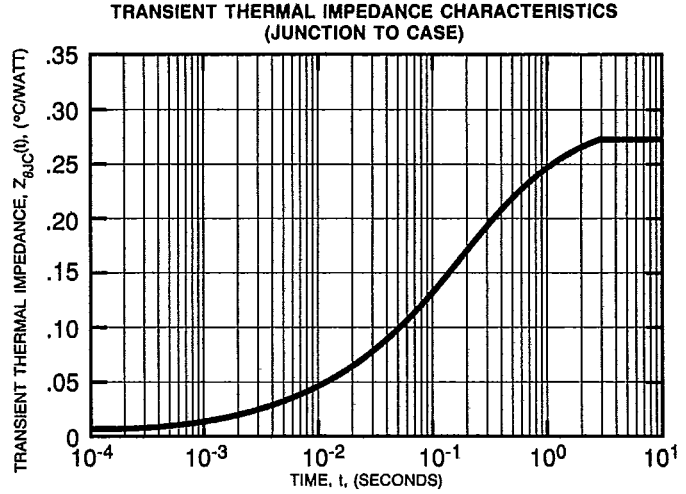
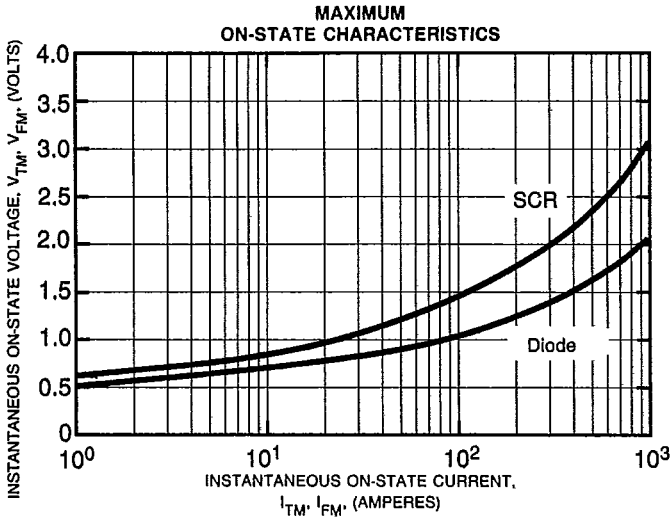
WARNING:

Internal insulation used is Beryllium Oxide. User should avoid grinding, crushing or abrading these portions. Care must be exercised in properly disposing of unwanted modules.



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CD72 — 60 —, CD77 — 60 —
 Current Source Inverter
 POW-R-BLOK™ Modules
 60 Amperes/100-1200 Volts



ASCI Current Source Inverter



T-91-01

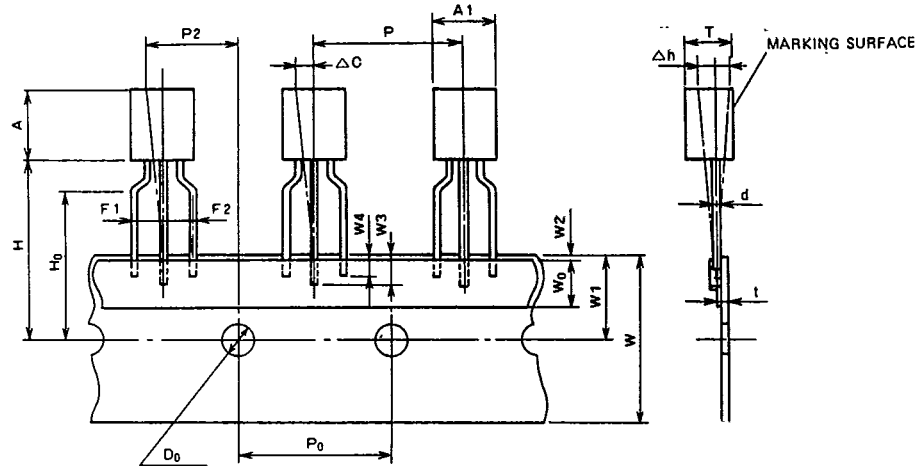
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Taping

STANDARD SPECIFICATIONS FOR TAPING OF MOLDED PACKAGE THYRISTORS AND TRIACS

TO-92 Package

Thyristor
CR02AM, CR03AM, CR04AM
Triac
BCR1AM



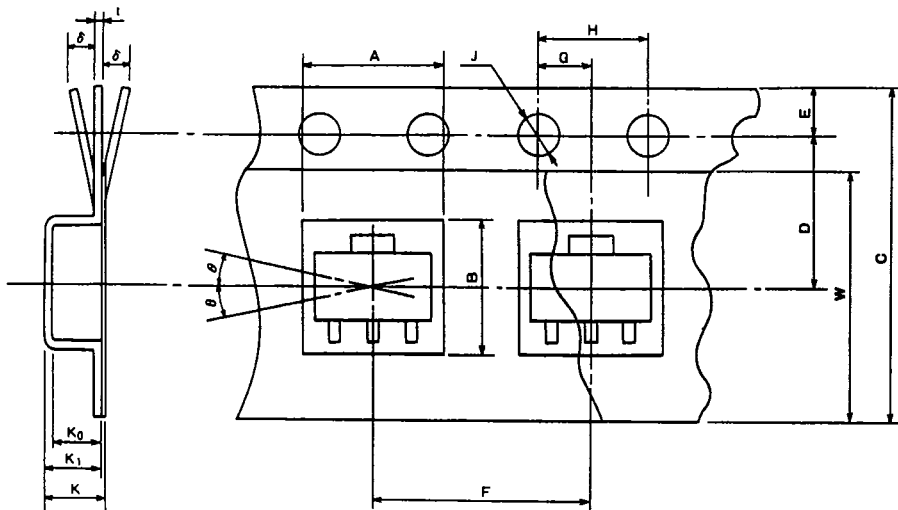
Taping dimensions

Description of symbol	Symbol	Dimensions (Unit:mm)	Remark
Product width	A1	5.0 MAX	
Product height	A	5.0 MAX	
Product thickness	T	3.7 MAX	
Lead wire diameter	d	0.6 MAX	
Sticker lead wire length (1)	W3	2.5 MIN	
Sticker lead wire length (2)	W4	2.0 MIN	
Pitch between products	P	12.7 ± 1.0	
Feed hole pitch	P ₀	12.7 ± 0.3	The cumulative pitch error is ± 1mm per 20 pitches.
Feed hole deviation (1)	P2	6.35 ± 1.3	
Distance between lead wires	F1, F2	2.5 ± 0.4	
Defective product (1)	Δh	0 ± 2.0	
Tape width	W	18.0 ± ^{1.0} / _{0.5}	
Sticker tape width	W ₀	6.0 ± 0.5	
Feed hole deviation (2)	W1	9.0 ± 0.5	
Sticker tape deviation	W2	0.5 MAX	
Position of product bottom surface	H	17.5 MIN	
Lynch height of lead wire	H ₀	16.0 ± 0.5	
Feed hole diameter	D ₀	4.0 ± 0.2	
Tape thickness	t	0.7 ± 0.2	
Defective product (2)	ΔC	0 ± 1.0	



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Powerex Semiconductor Data Book
 Taping



SOT-89 Package

Thyristor
 CR08AS

Taping dimensions

Description of symbol		Symbol	Dimensions/angles Unit:mm	Remark
Parts insertion	Height	A	5.0 ± 0.1	Cross-section of the surface 0.5mm above the inner bottom
	Width	B	4.6 ± 0.1	Cross-section of the surface 0.5mm above the inner bottom
Concave square hole	Depth	K ₀	1.8 ± 0.1	Inner space
	Pitch	F	8.0 ± 0.1	Cumulative error +0.1/-0.3 MAX/10 pitches
Round feed hole	Diameter	J	$\phi 1.5 \pm 0.05$	
	Pitch	H	4.0 ± 0.1	Cumulative error +0.1/-0.3 MAX/10 pitches
	Position	E	1.5 ± 0.1	Distance between the tape edge and the hole center
Distance between center lines	Vertical	G	2.0 ± 0.5	Center line of concave square hole and round feed hole
	Horizontal	D	5.65 ± 0.05	Center line of concave square hole and round feed hole
Cover tape	Width	W	$9.5 + 0.3/-0$	Thickness: 0.1 MAX
Carrier tape	Width	C	12 ± 0.2	Warp ± 0.3 MAX
	Thickness	t	0.3 ± 0.05	
	Package hole depth	K ₁	2.1 ± 0.1	
Device	Package dimensions	—	—	As shown in (e)
	Inclination	θ	30° MAX.	
Total Thickness		K	2.3 ± 0.1	Total thickness including cover and carrier tapes