



**Integrated  
Circuit  
Systems, Inc.**

**AV9107**

## CPU Frequency Generator

### Features

- Patented on-chip Phase Locked Loop with VCO for clock generation
- Provides reference clock and synthesized clock
- Generates frequencies from 2 to 120 MHz
- 2 to 32 MHz input reference frequency
- On chip loop filter
- Up to 16 frequencies stored internally
- Low power CMOS technology
- Single +3.3 or +5 volt power supply
- Runs up to 50 MHz at 3.3V
- 8 pin DIP or SOIC package or  
14 pin DIP or SOIC package

### General Description

The AV9107 offers a tiny footprint solution for generating two simultaneous clocks. One clock, the REFCLK, is a fixed output frequency which is the same as the input reference crystal (or clock). The other clock, CLK1, can vary between 2 and 120 MHz, with up to 16 selectable preprogrammed frequencies stored in internal ROM.

The device has advanced features which include on-chip loop filters, tri-state outputs, and power down capability. A minimum of external components - two decoupling capacitors and an optional ferrite bead - are all that are required for jitter free operation. Standard versions for computer motherboard applications are the AV9107-03, AV9107-04, AV9107-05 and AV9107-10. Custom masked versions, with customized frequencies and features, are available in 6-8 weeks for a small NRE.

### Applications

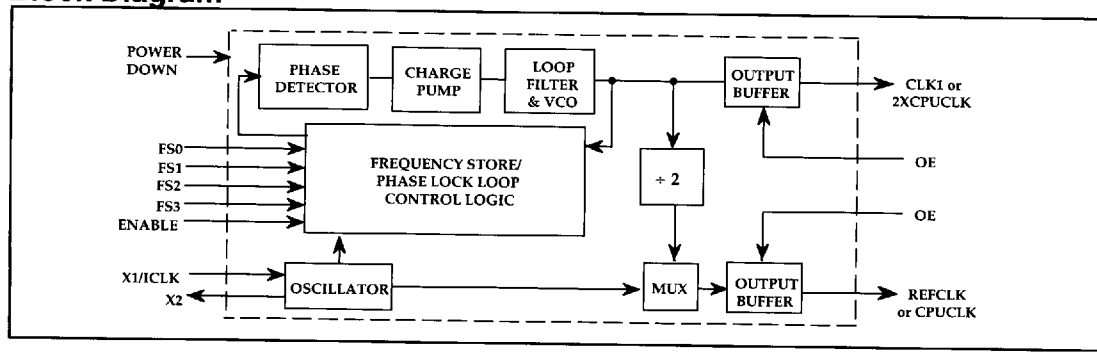
**Graphics:** The AV9107 is the easiest to use, lowest cost, and smallest footprint frequency generator for graphics applications. It can generate up to 16 different frequencies, including all frequencies necessary for VGA standards. It should be used in place of the AV9105/6 when the reference clock is also needed.

**Computer:** The AV9107 is the ideal solution for replacing high speed oscillators and for reducing clock speeds to save power in computers. The device provides smooth, glitch-free frequency transitions so that the CPU can continue to operate during slow down or speed up. The rate of frequency change makes the AV9107 compatible with all 386DX, 386SX, 486DX, 486DX2, and 486SX devices. Standard versions include the AV9107-03, -04, -05 and -10.

**Disk Drives:** Smaller than a single crystal or an oscillator, the tiny SOIC package can be used for any general purpose frequency generation in disk drives. The most popular application is for Constant Density Recording, where its low jitter output clock provides the necessary frequencies for reading and recording. Another popular application is for slowing the disk drive CPU to save power.

**High Speed Systems:** The AV9107 can be used as a proximity oscillator - using a low frequency (down to 2 MHz) input to generate a high frequency clock (up to 120 MHz) near the device requiring the high frequency. This avoids the need to route high speed traces over a long distance.

### Block Diagram





# AV9107

**Decoding Table for AV9107-05, 14.318 input**

FS1	FS0	CLK1
0	0	40 MHz
0	1	50 MHz
1	0	66.6 MHz
1	1	80 MHz

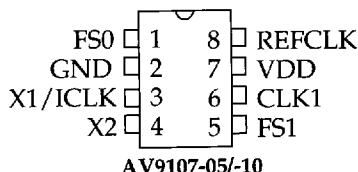
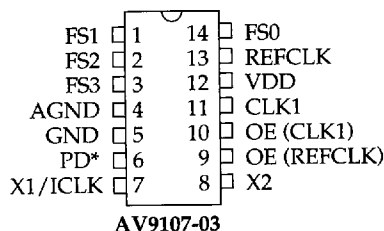
**Decoding Table for AV9107-10, 14.318 input**

FS1	FS0	CLK1
0	0	25 MHz
0	1	33.3 MHz
1	0	40 MHz
1	1	50 MHz

**Decoding Table for AV9107-03, 14.318 input**

FS3	FS2	FS1	FS0	CLK1
0	0	0	0	16 MHz
0	0	0	1	40 MHz
0	0	1	0	50 MHz
0	0	1	1	80 MHz
0	1	0	0	66.66 MHz
0	1	0	1	100 MHz
0	1	1	0	8 MHz
0	1	1	1	4 MHz
1	0	0	0	8 MHz
1	0	0	1	20 MHz
1	0	1	0	25 MHz
1	0	1	1	40 MHz
1	1	0	0	33.33 MHz
1	1	0	1	50 MHz
1	1	1	0	4 MHz
1	1	1	1	2 MHz

## Pin Configurations



## Pin Description for AV9107-03, AV9107-05 and AV9107-10

Pin Name	Pin #		Pin Type	Description
	-05/-10	-03		
FS0	1	14	Input	FREQUENCY SELECT 0 for CLK1 (-03 has pull-up)
FS1	5	1	Input	FREQUENCY SELECT 1 for CLK1 (-03 has pull-up)
FS2		2	Input	FREQUENCY SELECT 2 for CLK1 (-03 has pull-up)
FS3		3	Input	FREQUENCY SELECT 3 for CLK1 (-03 has pull-up)
AGND		4	-	Analog GROUND
GND	2	5	-	Digital GROUND
PD*		6	Input	POWER DOWN. Shuts off chip when low. Internal pull-up
X1/ICLK	3	7	Input	CRYSTAL INPUT or INPUT CLOCK frequency. Typically 14.318MHz system clock
X2	4	8	Output	CRYSTAL OUTPUT (No Connect when clock used)
OE(REFCLK)		9	Input	OUTPUT ENABLE. Tri-states REFCLK when low. Pull-up
OE(CLK1)		10	Input	OUTPUT ENABLE. Tri-states CLK1 when low. Pull-up
CLK1	6	11	Output	CLOCK1 Output (see decoding tables)
VDD	7	12	-	Digital power supply (+5V DC)
REFCLK	8	13	Output	REFERENCE CLOCK output. Produces a buffered version of the input clock or crystal frequency (typically 14.318 MHz)



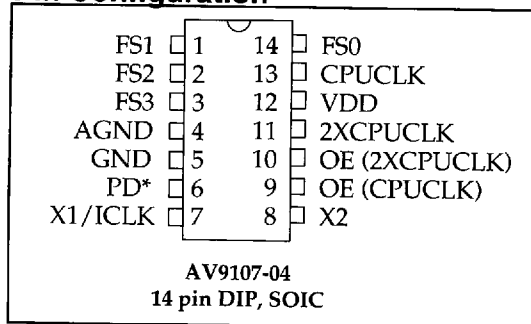
**AV9107**

**The AV9107-04**

The AV9107-04 provides a 2X output and a 1X output, which are skew controlled to within 1ns on the rising edges. For the frequencies listed in the decoding tables, the part assumes a 14.318 MHz input. The device is also useful for providing integer multiples or divides based on inputs in the range of 2 to 32 MHz.

**Decoding Table for AV9107-04  
(using a 14.318 MHz input)**

**Pin Configuration**



FS3	FS2	FS1	FS0	2XCPUCLK	CPUCLK
0	0	0	0	80 MHz	40 MHz
0	0	0	1	66.66 MHz	33.33 MHz
0	0	1	0	50 MHz	25 MHz
0	0	1	1	40 MHz	20 MHz
0	1	0	0	100 MHz	50 MHz
0	1	0	1	33.33 MHz	16.67 MHz
0	1	1	0	32 MHz	16 MHz
0	1	1	1	25 MHz	12.5 MHz
1	0	0	0	64 MHz	32 MHz
1	0	0	1	2X INPUT	INPUT
1	0	1	0	3X INPUT	1.5X INPUT
1	0	1	1	8X INPUT	4X INPUT
1	1	0	0	.5X INPUT	.25X INPUT
1	1	0	1	.25X INPUT	.125X INPUT
1	1	1	0	120 MHz	60 MHz
1	1	1	1	130 MHz	65 MHz

**D**

**Pin Description for AV9107-04**

Pin Name	Pin #	Pin Type	Description
FS1	1	Input	FREQUENCY SELECT 1 (see decoding table). Pull-up
FS2	2	Input	FREQUENCY SELECT 2 (see decoding table). Pull-up
FS3	3	Input	FREQUENCY SELECT 3 (see decoding table). Pull-up
AGND	4	-	Analog GROUND
GND	5	-	Digital GROUND
PD*	6	Input	POWER DOWN. Shuts off entire chip when low. Pull-up
X1/ICLK	7	Input	CRYSTAL INPUT or INPUT CLOCK frequency. Typically 14.318MHz system clock
X2	8	Output	CRYSTAL OUTPUT (No Connect when clock used)
OE(CPUCLK)	9	Input	OUTPUT ENABLE. Tri-states CPUCLK when low. Pull-up
OE(2XCPUCLK)	10	Input	OUTPUT ENABLE. Tri-states 2XCPUCLK when low. Pull-up
2XCPUCLK	11	Output	2X CPU CLOCK Output (see decoding table, note † below)
VDD	12	-	Digital power supply (+5V DC)
CPUCLK	13	Output	CPU CLOCK Output (see decoding table, note † below)
FS0	14	Input	FREQUENCY SELECT 0 (see decoding table). Pull-up

\*The CPUCLK and 2XCPUCLK outputs are skew controlled to within 1.0 ns max



## AV9107

---

### Frequency Accuracy and Calculation

The accuracy of the frequencies produced by the AV9107 depends on the input frequency and the desired actual output frequency. The formula for calculating the exact output frequency is as follows:

$$\text{Output Frequency} = \text{Input Frequency} \times \frac{A}{B}$$

where A = 2, 3, 4...128, and  
B = 2, 3, 4...32.

For example, to calculate the actual output frequency for a video monitor expecting a 44.900 MHz clock and using a 14.318 MHz input clock, the closest A/B ratio is 69/22, which gives an output of 44.906 MHz (within 0.02% of the target frequency). Generally, the AV9107 can produce frequencies within 0.1% of the desired output.

### Frequency Transitions

A key AV9107 feature is the ability to provide glitch-free frequency transitions across its output frequency range. The AV9107-03 provides smooth transitions between any of the two groups of eight frequencies (when FS3=0 or FS3=1), so that the device will switch glitch-free between 4 - 100 MHz and 2 - 50 MHz.

### Allowable Input and Output Frequencies

The input frequency should be between 2 and 32 MHz and the A/B ratio should not exceed 24. The output should fall in the range of 2-120 MHz.

### Output Enable

The Output Enable feature tri-states the specified output clock pins. This places the selected output pins in a high impedance state to allow for system level diagnostic testing.

### Power Down

If equipped, the power down pin shuts off the specified PLL or entire chip to save current. A few milliseconds are required to reach full functioning speed from a power down state.



AV9107

ABSOLUTE MAXIMUM RATINGS

AVDD, VDD referenced to GND..... 7V	Voltage on I/O pins referenced to GND..... GND -0.5V
Operating temperature under bias..... 0°C to +70°C	to VDD +0.5V
Storage temperature..... -65°C to +150°C	Power dissipation..... 0.5 Watts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect the reliability of the device.

ELECTRICAL CHARACTERISTICS AT 5V

(Operating  $V_{DD} = +4.5V$  to  $+5.5V$ ,  $T_A = 0°C$  to  $70°C$  unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
<b>DC CHARACTERISTICS</b>						
$V_{IL}$	Input Low Voltage	-	-	0.8	V	$V_{DD} = 5V$
$V_{IH}$	Input High Voltage	2.0	-	-	V	$V_{DD} = 5V$
$I_{IL}$	Input Low Current	-	-	-5	$\mu A$	$V_{IN} = 0V$
$I_{IH}$	Input High Current	-	-	5	$\mu A$	$V_{IN} = V_{DD}$
$V_{OL}$	Output Low Voltage	-	-	0.4	V	$I_{OL} = 8mA$
$V_{OH}$	Output High Voltage	2.4	-	-	V	$I_{OH} = -4mA$
$I_{DD}$	Supply Current	-	10	20	mA	Note 1
$f_d$	Output Frequency Change over Supply and Temperature	-	0.002	0.05	%	With respect to typical frequency
$C_i$	Input Capacitance	-	-	10	pF	Except X1, X2
$C_L$	Load Capacitance	-	20	-	pF	Pins X1, X2
$I_{DDSTDBY}$	Standby Supply Current	-	25	-	$\mu A$	Note 2
<b>AC CHARACTERISTICS</b>						
$t_w$	Enable pulse width	20	-	-	ns	
$t_{st}$	Setup time data to enable	20	-	-	ns	
$f_o$	Output Frequency	2	-	120	MHz	
$f_i$	Input Frequency	2	14.318	32	MHz	
$ICLK_i$	Input Clock Rise time	-	-	20	ns	
$ICLK_f$	Input Clock Fall time	-	-	20	ns	
$t_{hd}$	Hold time data to enable	10	-	-	ns	
$t_r$	Output Rise time, 0.8 to 2.0V	-	1	2	ns	25 pf load
$t_r$	Rise time, 20% to 80% $V_{DD}$	-	2	4	ns	25 pf load
$t_f$	Output Fall time, 2.0 to 0.8V	-	1	2	ns	25 pf load
$t_f$	Fall time, 80% to 20% $V_{DD}$	-	-	4	ns	25 pf load
$d_t$	Duty cycle	40	50/50	60	%	15 pf load
$T_{jis}$	Jitter, 1 sigma	-	$\pm 0.5$	$\pm 2$	%	All frequencies
$T_{jabs}$	Jitter, absolute	-	$\pm 3$	$\pm 5$	%	All frequencies
$t_{ft}$	Frequency Transition time	-	-	20	ms	From 50 to 4 MHz
$t_{pu}$	Power up time	-	15	30	ms	From off to 100MHz
$T_{sk}$	Clock skew between CPUCLK and 2XCPUCLK outputs	-	$\pm 0.5$	$\pm 1.0$	ns	AV9107-04

Note 1: AV9107-03 with no load, with 14.318 MHz crystal input, and CLK1 running at 40 MHz. Power supply current varies with frequency. Consult Avasem for actual current at different frequencies.

Note 2: AV9107-03 with the power down pin low (active).

Note 3: To guarantee operation at 100 MHz or above, please indicate the highest speed used when ordering. For example, if 120 MHz would be used on the AV9107-04CS14, order it as AV9107-04CS14-120.



# AV9107

## Electrical Characteristics at 3.3V

(Operating  $V_{DD} = +3.0V$  to  $+3.7V$ ,  $T_A = 0^{\circ}C$  to  $70^{\circ}C$  unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
<b>DC CHARACTERISTICS</b>						
$V_{IL}$	Input Low Voltage	-	-	$0.15V_{DD}$	V	
$V_{IH}$	Input High Voltage	$0.7V_{DD}$	-	-	V	
$I_{IL}$	Input Low Current	-	-	-5	$\mu A$	$V_{IN} = 0V$
$I_{IH}$	Input High Current	-	-	5	$\mu A$	$V_{IN} = V_{DD}$
$V_{OL}$	Output Low Voltage	-	-	0.1	V	$I_{OL} = 8mA$
$V_{OH}$	Output High Voltage	$V_{DD} - 1V$	-	-	V	$I_{OH} = -4mA$
$I_{DD}$	Supply Current	-	8	15	mA	Note 1
$F_d$	Output Frequency Change over Supply and Temperature	-	0.002	0.01	%	With respect to typical frequency
$C_i$	Input Capacitance	-	-	10	pF	Except X1, X2
$C_L$	Load Capacitance	-	20	-	pF	Pins X1, X2
$I_{DDSTDBY}$	Supply Current, Standby	-	15	-	$\mu A$	When powered down
<b>AC CHARACTERISTICS</b>						
$t_w$	Enable pulse width	20	-	-	ns	
$t_{setup}$	Setup time data to enable	20	-	-	ns	
$t_{r, ICLK}$	Input Clock Rise time	-	-	20	ns	
$t_{f, ICLK}$	Input Clock Fall time	-	-	20	ns	
$t_{hd}$	Hold time data to enable	10	-	-	ns	
$t_r$	Rise time	-	-	4	ns	15 pf load
$t_f$	Fall time	-	-	4	ns	15 pf load
$d$	Duty cycle	40	50/50	60	%	15 pf load
$T_{j1\sigma}$	Jitter, 1 sigma	-	$\pm 0.5$	$\pm 2$	%	All frequencies
$T_{jabs}$	Jitter, absolute	-	$\pm 3$	$\pm 5$	%	All frequencies
$t_{ft}$	Frequency Transition time	-	15	20	ms	From 2 to 25 MHz
$t_{pu}$	Power up time	-	-	-	ms	From off to 66.66 MHz
$f_o$	Output Frequency	2	-	80	MHz	
$f_i$	Input Frequency	2	14.318	32	MHz	

Note 1: AV9107-03 with no load, with 14.318 MHz crystal input, and CLK1 running at 40 MHz. Power supply current varies with frequency. Consult ICS for actual current at different frequencies.

Note 2: To guarantee 3V operation, please specify the AV9107-xxCxxx-3V when ordering.



**AV9107**

**Actual Frequencies**

**Decoding Table for AV9107-05, 14.318 input**

FS1	FS0	CLK1
0	0	40.01 MHz
0	1	50.11 MHz
1	0	66.61 MHz
1	1	80.01 MHz

**Decoding Table for AV9107-04, 14.318 input**

FS3	FS2	FS1	FS0	2XCPUCLK	CPUCLK
0	0	0	0	80.02 MHz	40.01 MHz
0	0	0	1	66.62 MHz	33.31 MHz
0	0	1	0	50.11 MHz	25.06 MHz
0	0	1	1	40.01 MHz	20.00 MHz
0	1	0	0	100.23 MHz	50.11 MHz
0	1	0	1	33.31 MHz	16.66 MHz
0	1	1	0	32.01 MHz	16.00 MHz
0	1	1	1	25.06 MHz	12.47 MHz
1	0	0	0	64.02 MHz	32.01 MHz
1	0	0	1	2X INPUT	1X INPUT
1	0	1	0	3X INPUT	1.5X INPUT
1	0	1	1	8X INPUT	4X INPUT
1	1	0	0	.5X INPUT	.25X INPUT
1	1	0	1	.25X INPUT	.125X INPUT
1	1	1	0	120.00 MHz	60.00 MHz
1	1	1	1	129.96 MHz	64.98 MHz

**Decoding Table for AV9107-03, 14.318 input**

FS3	FS2	FS1	FS0	CLK1
0	0	0	0	16.00 MHz
0	0	0	1	39.99 MHz
0	0	1	0	50.11 MHz
0	0	1	1	80.01 MHz
0	1	0	0	66.58 MHz
0	1	0	1	100.23 MHz
0	1	1	0	8.02 MHz
0	1	1	1	4.01 MHz
1	0	0	0	8.02 MHz
1	0	0	1	20.00 MHz
1	0	1	0	25.06 MHz
1	0	1	1	40.01 MHz
1	1	0	0	33.29 MHz
1	1	0	1	50.11 MHz
1	1	1	0	4.01 MHz
1	1	1	1	2.05 MHz

**Decoding Table for AV9107-10, 14.318 input**

FS1	FS0	CLK1
0	0	25.057 MHz
0	1	33.289 MHz
1	0	40.006 MHz
1	1	50.113 MHz

**D**



## AV9107

### Ordering Information

Part Number	Temperature Range	Package Type
AV9107-xxCN8	0°C to +70°C	8 lead Plastic DIP (300 mils)
AV9107-xxCS8	0°C to +70°C	8 lead SOIC (150 mils)
AV9107-xxCN14	0°C to +70°C	14 lead Plastic DIP (300 mils)
AV9107-xxCS14	0°C to +70°C	14 lead SOIC (150 mils)