| REVISIONS | | | |
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| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
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| REV | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | | | | | | | | | | | | | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | | | | | | | | | | |

| REV STATUS OF SHEETS | | REV | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Thomas M. Hess

CHECKED BY
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APPROVED BY
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DRAWING APPROVAL DATE
96-01-10

REVISION LEVEL

**DEFENSE ELECTRONICS SUPPLY CENTER**
**DAYTON, OHIO 45444**

MICROCIRCUIT, DIGITAL, RADIATION HARDENED, CMOS, HIGH PERFORMANCE PROGRAMMABLE DMA CONTROLLER, MONOLITHIC SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| A | 67268 | 5962-95821 |

SHEET 1 OF 24

DESC FORM 193
JUL 94

5962-E217-96

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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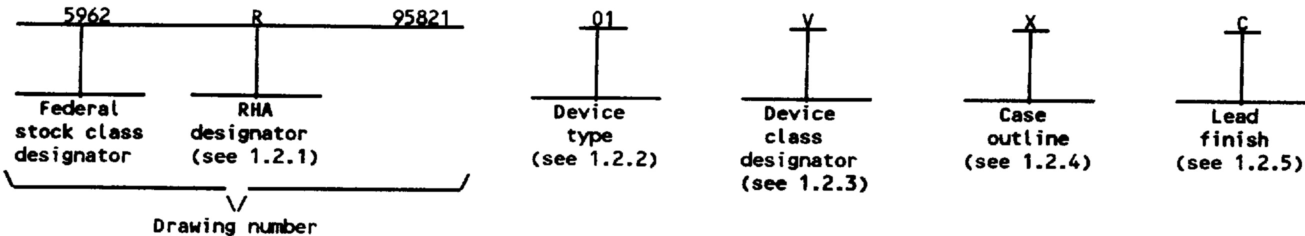
1. SCOPF

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:




1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 82C37ARH | Radiation hardened CMOS high performance programmable DMA controller |

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883 |
| Q or V | Certification and qualification to MIL-I-38535 |

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| Q | CDIP2-T40 | 40 | dual-in-line package |
| X | See figure 1 | 42 | flatpack |

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.



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1.3 Absolute maximum ratings. 1/

| | |
|---|---|
| Supply voltage ($V_{DD}$) | +6.5 V dc |
| Input or output voltage | $V_{SS}$ -0.3 V dc to $V_{DD}$ +0.3 V dc |
| Storage temperature range ($T_{STG}$) | -65°C to +150°C |
| Junction temperature ($T_J$) | +175°C |
| Lead temperature (soldering 10 seconds) ($T_S$) | +300°C |
| Thermal resistance junction-to-case ($\theta_{JC}$): | |
| Case outline Q | 5°C/W |
| Case outline X | 10°C/W |
| Thermal resistance junction-to-ambient ($\theta_{JA}$): | |
| Case outline Q | 38°C/W |
| Case outline X | 72°C/W |
| Maximum package power dissipation $T_A$ = +125°C ($P_D$): 2/ | |
| Case outline Q | 1.32 W |
| Case outline X | 0.69 W |

1.4 Recommended operating conditions.

| | |
|---|---|
| Operating supply voltage range ($V_{DD}$) | +4.5 V dc to +5.5 V dc |
| Operating temperature range ($T_A$) | -55°C to +125°C |
| Input low voltage range ($V_{IL}$) | 0 V dc to +0.8 V dc |
| Input high voltage range ($V_{IH}$) | $V_{DD}$ -1.5 V dc to $V_{DD}$ |
| Radiation features | |
| Total dose | > 100 k Rads(SI) |
| Transient upset | > $10^8$ RAD(SI)/sec 3/ |
| Single event phenomenon effective linear energy threshold, no upsets | 9 MEV/(mg/$cm^2$) 3/ |

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ If device power exceeds package dissipation capability. provide heat sinking or derate linearly (the derating is based on $\theta_{JA}$ at a rate of 26.3 mW/°C for case Q and 13.9 mW/°C for case X).
3/ Guaranteed by design or process but not tested.



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(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Switching waveforms test circuit The switching waveform shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).



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TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| TTL output high voltage | $V_{OH1}$ | $V_{DD}$ = 4.5 V, $I_O$ = -2.5 mA, $V_{IN}$ = 0 V or 4.0 V | 1,2,3 | All | 3.0 | | V |
| CMOS output high voltage | $V_{OH2}$ | $V_{DD}$ = 4.5 V, $I_O$ = -100 µA, $V_{IN}$ = 0 V or 4.0 V | 1,2,3 | All | $V_{DD}$-0.4 | | V |
| Output low voltage | $V_{OL1}$ | $V_{DD}$ = 4.5 V, $I_O$ = +2.5 mA, $V_{IN}$ = 0 V or 4.0 V | 1,2,3 | All | | 0.4 | V |
| Input leakage current | $I_{IL}$ or $I_{IH}$ | $V_{DD}$ = 5.5 V, $V_{IN}$ = 0 V or 5.5 V, DIL Pins: 6, 7, 11-13, 16-19 | 1,2,3 | All | -1.0 | 1.0 | µA |
| Output leakage current | $I_{OZL}$ or $I_{OZH}$ | $V_{DD}$ = 5.5 V, $V_{IN}$ = 0 V or 5.5 V, DIL Pins: 1-4, 21-23, 26, 30, 32-40 | 1,2,3 | All | -10 | 10 | µA |
| Standby power supply current | $I_{DDSB}$ | $V_{DD}$ = 5.5 V, $I_O$ = 0 mA, $V_{IN}$ = GND or $V_{DD}$ | 1,2,3 | All | | +50 | µA |
| Operating power supply current | $I_{DDOP}$ | $V_{DD}$ = 5.5 V, $I_O$ = 0 mA, $V_{IN}$ = GND or $V_{DD}$, f = 5 MHz | 1,2,3 | All | | 20 | mA |
| Input capacitance | $C_{IN}$ | See 4.4.1c $V_{DD}$ = Open, f = 1 MHz, All measurements referenced to device ground | 4 | All | | 15 | pF |
| Output capacitance | $C_{OUT}$ | See 4.4.1c $V_{DD}$ = Open, f = 1 MHz, All measurements referenced to device ground | 4 | All | | 15 | pF |
| I/O capacitance | $C_{I/O}$ | See 4.4.1c $V_{DD}$ = Open, f = 1 MHz, All measurements referenced to device ground | 4 | All | | 20 | pF |
| Functional test | | See 4.4.1b $V_{DD}$ = 4.5 V and 5.5 V, $V_{IN}$ = GND or $V_{DD}$, f = 1 MHz | 7,8 | All | | | |
| Noise immunity functional test | | See 4.4.1b $V_{DD}$ = 4.5 V and 5.5 V, $V_{IN}$ = GND or $V_{DD}$ - 1.5 V and $V_{DD}$ = 4.5 V, $V_{IN}$ = 0.8 V or $V_{DD}$ | 7,8 | All | | | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 1/ 2/ $-55°C \leq T_A +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| DMA (MASTER) MODE | | | | | | | |
| AEN HIGH from CLK LOW (S1) delay time | $t_{CLAEH}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | | 175 | ns |
| AEN LOW from CLK HIGH (S1) delay time | $t_{CHAEL}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | | 130 | ns |
| ADR from $\overline{READ}$ HIGH hold time | $t_{RHAX}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | $t_{CLCL}$-100 | | ns |
| DB from ADSTB LOW hold time | $t_{SLDZ}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | $t_{CLCH}$-18 | | ns |
| ADR from $\overline{WRITE}$ HIGH hold time | $t_{WHAX}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | $t_{CLCL}$-50 | | ns |
| DACK valid from CLK LOW delay time | $t_{CLDAV}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | | 170 | ns |
| $\overline{EOP}$ HIGH from CLK HIGH delay time | $t_{CHIPH}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | | 170 | ns |
| $\overline{EOP}$ LOW from CLK HIGH delay time | $t_{CHIPL}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | | 100 | ns |
| ADR stable from CLK HIGH | $t_{CHAV}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | | 110 | ns |
| DB to ADSTB LOW setup time | $t_{DVSL}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | $t_{CHCL}$+10 | | ns |
| Clock HIGH time (transitions 10 ns) | $t_{CHCL}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | 70 | | ns |
| Clock LOW time (transitions 10 ns) | $t_{CLCH}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | 50 | | ns |
| CLK cycle time | $t_{CLCL}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | 200 | | ns |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| DMA (MASTER) MODE - CONTINUED. | | | | | | | |
| CLK HIGH to READ or WRITE LOW delay | $t_{CHRWL}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | | 190 | ns |
| READ HIGH from CLK HIGH (S4) delay time | $t_{CHRH}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | | 190 | ns |
| WRITE HIGH from CLK HIGH (S4) delay time | $t_{CHWH}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | | 130 | ns |
| HRQ valid from CLK HIGH delay time | $t_{CHRQV}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | | 120 | ns |
| EOP LOW to CLK LOW setup time | $t_{EPLCL}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | 40 | | ns |
| EOP pulse width | $t_{EPLEPH}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | 220 | | ns |
| READ or WRITE active from CLK HIGH | $t_{CHRWV}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | | 150 | ns |
| DB float to active delay from CLK HIGH | $t_{CHDV}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | | 110 | ns |
| HLDA valid to CLK HIGH setup time | $t_{RAVCH}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | 75 | | ns |
| Input data from MEMR HIGH hold time | $t_{MRHDX}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | 0 | | ns |
| Input data from MEMR HIGH setup time | $t_{DVMRH}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | 155 | | ns |
| Output data from MEMW HIGH hold time | $t_{MWHDZ}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | 15 | | ns |
| Output data valid MEMW HIGH | $t_{DVMWH}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | $t_{CLCL}$-35 | | ns |
| DREQ to CLK LOW (S1,S4) setup time | $t_{DQVCL}$ | $V_{DD}$ = 4.5 V 2/ 3/ See figure 4 | 9,10,11 | All | 0 | | ns |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 1/ $-55°C \leq T_A \leq +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| DMA (MASTER) MODE - CONTINUED. | | | | | | | |
| CLK LOW to READY hold time | $t_{CLRYX}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | 20 | | ns |
| READY to CLK LOW setup time | $t_{RYVCL}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | 60 | | ns |
| ADSTB HIGH from CLK LOW delay time | $t_{CLSH}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | | 80 | ns |
| ADSTB LOW from CLK LOW delay time | $t_{CLSL}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | | 120 | ns |
| $\overline{READ}$ HIGH delay from $\overline{WRITE}$ HIGH | $t_{WHRH}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | 0 | | ns |
| $\overline{READ}$ pulse width, normal timing | $t_{RLRH1}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | $2t_{CLCL}$-50 | | ns |
| ADSTB pulse width | $t_{SHSL}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | $t_{CLCL}$-80 | | ns |
| Extended $\overline{WRITE}$ pulse width | $t_{WLWH1}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | $2t_{CLCL}$-100 | | ns |
| $\overline{WRITE}$ pulse width | $t_{WLWH2}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | $t_{CLCL}$-100 | | ns |
| $\overline{READ}$ pulse width, compressed | $t_{RLRH2}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | $t_{CLCL}$-50 | | ns |
| PERIPHERAL (SLAVE) MODE | | | | | | | |
| ADR valid or $\overline{CS}$ LOW to $\overline{IOR}$ LOW | $t_{AVIRL}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | 10 | | ns |
| Data valid to $\overline{IOW}$ HIGH setup time | $t_{DVIWH}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | 150 | | ns |
| ADR or $\overline{CS}$ hold from $\overline{IOR}$ HIGH | $t_{IRHAX}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | 0 | | ns |
| Data access from $\overline{IOR}$ | $t_{IRLDV}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | | 150 | ns |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 1/ -55°C ≤ $T_A$ ≤ +125°C unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| PERIPHERAL (SLAVE) MODE - CONTINUED. | | | | | | | |
| $\overline{RESET}$ to first $\overline{IOW}$ or $\overline{IOR}$ | $t_{RSLIRWL}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | $2t_{CLCL}$ | | ns |
| RESET pulse width | $t_{RSHRSL}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | 300 | | ns |
| $\overline{IOR}$ width | $t_{IRLIRH}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | 200 | | ns |
| ADR or $\overline{CS}$ HIGH from $\overline{IOW}$ HIGH hold time | $t_{IWHAX}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | 0 | | ns |
| Data from $\overline{IOW}$ HIGH hold time | $t_{IWHDX}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | 10 | | ns |
| $\overline{IOW}$ width | $t_{IWLIWH}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | 150 | | ns |
| ADR valid or $\overline{CS}$ low to IOW low setup time 0 | $t_{AVIWL}$ | See figure 4 $V_{DD}$ = 4.5 V 2/ 3/ | 9,10,11 | All | 0 | | ns |
| CHARACTERIZATION PARAMETERS | | | | | | | |
| ADR active to float delay from CLK HIGH | $t_{CHAZ}$ | See figure 4 $V_{DD}$ = 4.5 V and 5.5 V 4/ | 9,10,11 | All | | 90 | ns |
| READ or WRITE float delay from CLK HIGH | $t_{CHRWZ}$ | See figure 4 $V_{DD}$ = 4.5 V and 5.5 V 4/ | 9,10,11 | All | | 120 | ns |
| DB active to float delay from CLK HIGH | $t_{CHDZ}$ | See figure 4 $V_{DD}$ = 4.5 V and 5.5 V 4/ | 9,10,11 | All | | 170 | ns |
| DB float delay from IOR HIGH | $t_{IRHDZ}$ | See figure 4 $V_{DD}$ = 4.5 V and 5.5 V 4/ | 9,10,11 | All | 10 | 85 | ns |
| Power supply HIGH to RESET LOW setup time | $t_{PHRSL}$ | See figure 4 $V_{DD}$ = 4.5 V and 5.5 V 4/ | 9,10,11 | All | 500 | | ns |

1/ Devices supplied to this drawing will meet all levels M, D, L, and R of irradiation. However, this device is only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, $T_A$ = +25°C.

2/ $\overline{READ}$ refers to both $\overline{IOR}$, and $\overline{MEMR}$, and WRITE refers to both $\overline{IOW}$ and $\overline{MEMW}$, during memory to I/O and I/O to memory transfers.

3/ Unless otherwise specified, all testing to be performed using worst-case conditions.

4/ The parameters listed in the table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.



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Case X

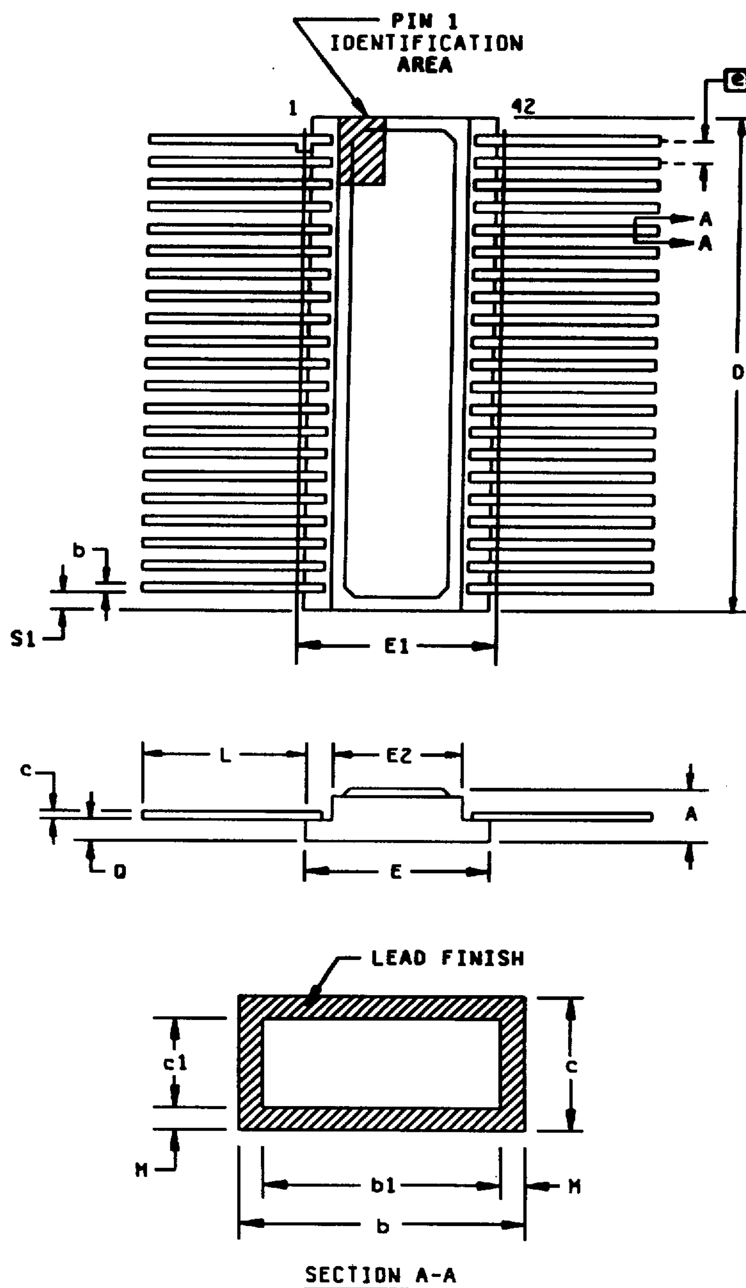


Figure 1. Case outline.



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Case X

| Symbol | Millimeters | | Inches | | Notes |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| A | - | 2.54 | - | 0.100 | |
| b | 0.43 | 0.64 | 0.017 | 0.025 | |
| b1 | 0.43 | 0.58 | 0.017 | -.023 | |
| c | 0.18 | 0.33 | 0.007 | 0.013 | |
| c1 | 0.18 | 0.25 | 0.007 | 0.010 | |
| D | 26.54 | 27.31 | 1.045 | 1.075 | 3 |
| E | 16.00 | 16.51 | 0.630 | 0.650 | |
| E1 | - | 17.27 | - | 0.680 | |
| E2 | 13.46 | 13.97 | 0.530 | 0.550 | |
| e | 1.27 BSC | | 0.050 BSC | | 11 |
| L | 8.13 | 8.89 | 0.320 | 0.350 | |
| Q | 1.14 | 1.65 | 0.045 | 0.065 | 8 |
| S1 | 0 | - | 0 | - | 6 |
| M | - | 0.04 | - | 0.0015 | |
| N | 42 | | 42 | | |

Figure 1. Case outline. - Continued



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| Device type | 01 | | |
|---|---|---|---|
| Case outlines | Q | | |
| Terminal number | Terminal symbol | Terminal number | Terminal symbol |
| 1 | $\overline{IOR}$ | 21 | DB7 |
| 2 | $\overline{IOW}$ | 22 | DB6 |
| 3 | $\overline{MEMR}$ | 23 | DB5 |
| 4 | $\overline{MEMW}$ | 24 | DACK1 |
| 5 | N.C. | 25 | DACK0 |
| 6 | READY | 26 | DB4 |
| 7 | HLDA | 27 | DB3 |
| 8 | ADSTB | 28 | DB2 |
| 9 | AEN | 29 | DB1 |
| 10 | HRQ | 30 | DB0 |
| 11 | $\overline{CS}$ | 31 | $V_{DD}$ |
| 12 | CLK | 32 | A0 |
| 13 | RESET | 33 | A1 |
| 14 | DACK2 | 34 | A2 |
| 15 | DACK3 | 35 | A3 |
| 16 | DREQ3 | 36 | $\overline{EOP}$ |
| 17 | DREQ2 | 37 | A4 |
| 18 | DREQ1 | 38 | A5 |
| 19 | DREQ0 | 39 | A6 |
| 20 | Vss | 40 | A7 |

FIGURE 2. Terminal connections.



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| Device type | 01 | | |
|---|---|---|---|
| Case outlines | X | | |
| Terminal number | Terminal symbol | Terminal number | Terminal symbol |
| 1 | $\overline{IOR}$ | 23 | DB6 |
| 2 | $\overline{IOW}$ | 24 | DB5 |
| 3 | $\overline{MEMR}$ | 25 | DACK1 |
| 4 | $\overline{MEMW}$ | 26 | DACK0 |
| 5 | N.C. | 27 | NC |
| 6 | READY | 28 | DB4 |
| 7 | HLDA | 29 | DB3 |
| 8 | ADSTB | 30 | DB2 |
| 9 | AEN | 31 | DB1 |
| 10 | HRQ | 32 | DB0 |
| 11 | $\overline{CS}$ | 33 | VDD |
| 12 | CLK | 34 | A0 |
| 13 | RESET | 35 | A1 |
| 14 | DACK2 | 36 | A2 |
| 15 | DACK3 | 37 | A3 |
| 16 | NC | 38 | $\overline{EOP}$ |
| 17 | DREQ3 | 39 | A4 |
| 18 | DREQ2 | 40 | A5 |
| 19 | DREQ1 | 41 | A6 |
| 20 | DREQ0 | 42 | A7 |
| 21 | GND | | |
| 22 | DB7 | | |

Figure 2. Terminal connections. - Continued




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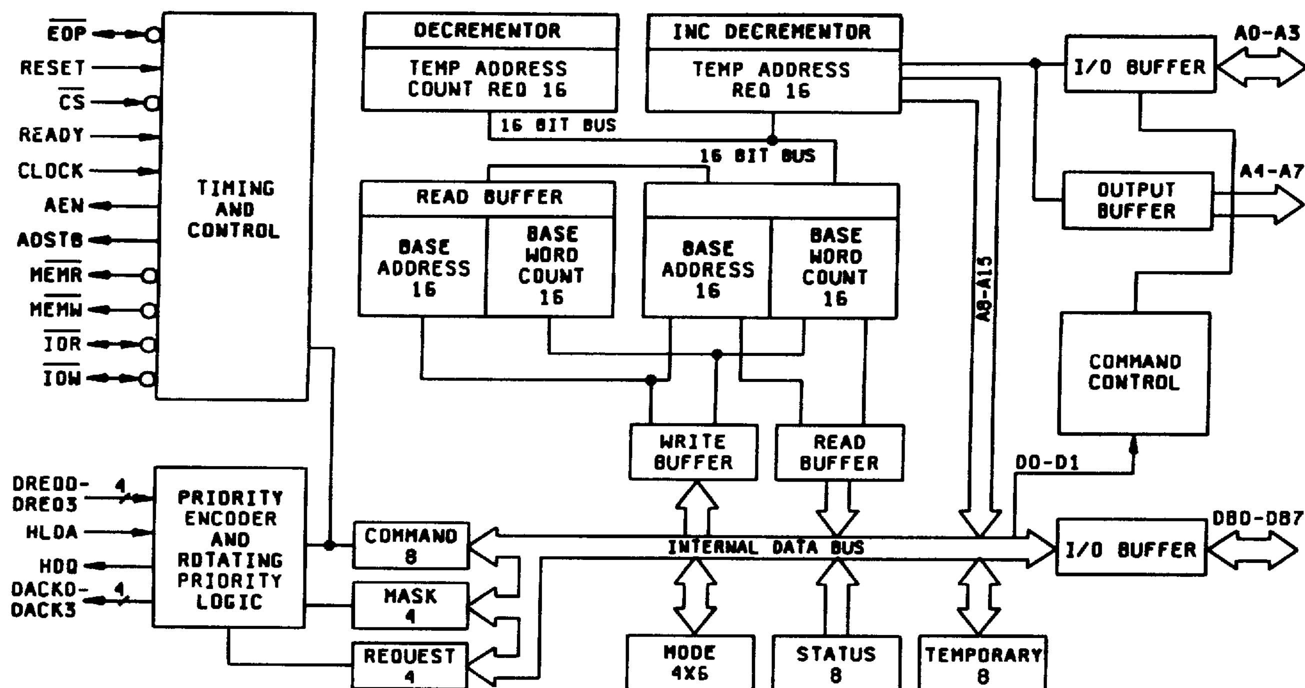


FIGURE 3. Block diagram.



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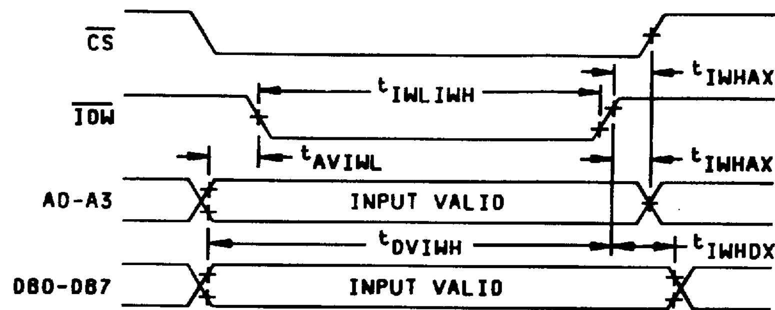
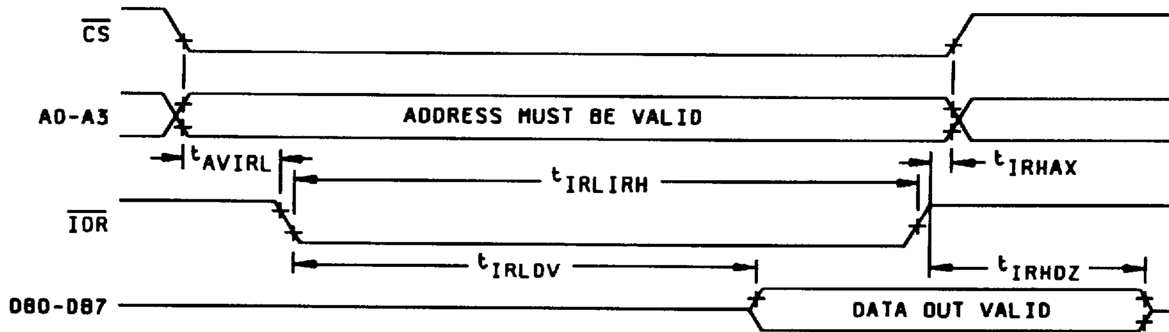


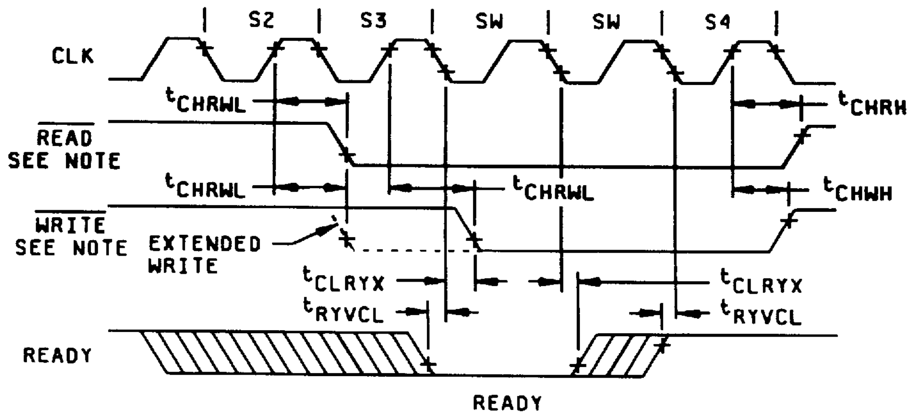

SLAVE MODE TIMING

NOTE: HOST SYSTEM MUST ALLOW AT LEAST TCLCL AS RECOVERY TIME BETWEEN SUCCESSIVE WRITE ACCESSES.




SLAVE MODE TIMING

NOTE: HOST SYSTEM MUST ALLOW AT LEAST TCLCL AS RECOVERY TIME BETWEEN SUCCESSIVE WRITE ACCESSES.




NOTE: READ REFERS TO BOTH IOR AND MEMR OUTPUTS.
WRITE REFERS TO BOTH IOW AND MEMW OUTPUTS.

Figure 4. Timing waveforms test circuit.



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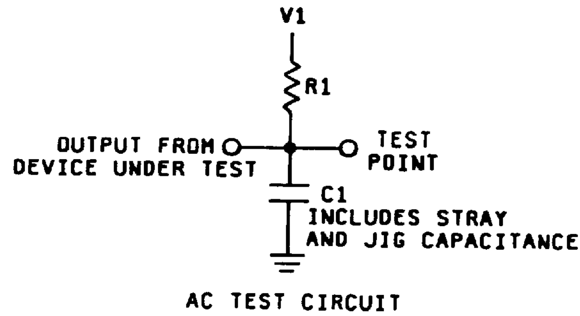
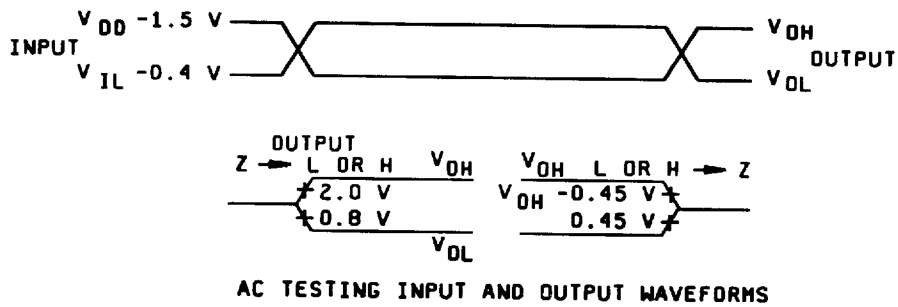



AC TEST CIRCUIT




AC TESTING INPUT AND OUTPUT WAVEFORMS

| Pins | $V_1$ | $R_1$ | $C_1$ |
|---|---|---|---|
| All output except $\overline{EOP}$ | 1.7 V | 510Ω | 100 pF |
| $\overline{EOP}$ | $V_{DD}$ | 1.6 kΩ | 50 pF |

Figure 4. Timing waveforms test circuit. - Continued



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DMA TRANSFER

Figure 4. Timing waveforms test circuit. - Continued



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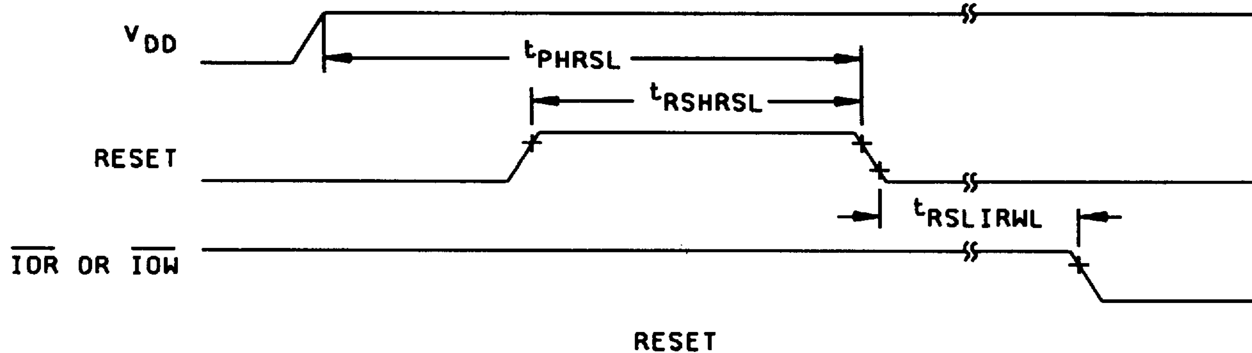
S0 | S11 | S12 | S13 | S14 | S21 | S22 | S23 | S24 | S1

CLK
ADSTB
A0-A7 — ADDRESS VALID — ADDRESS VALID
DB0-DB7 — A8-A15 — IN — A8-A15 — OUT
MEMR
MEMW
EXTENDED WRITE
INT EOP
EXT EOP

$t_{CLSH}$, $t_{CLSL}$, $t_{CHAV}$, $t_{SLDZ}$, $t_{CHAZ}$, $t_{CHDZ}$, $t_{CHDV}$, $t_{CHRH}$, $t_{CHRWL}$, $t_{MRHDX}$, $t_{DVMWH}$, $t_{MWHDZ}$, $t_{CHWH}$, $t_{CHRVW}$, $t_{DVMRH}$, $t_{CHRWZ}$, $t_{CHIPL}$, $t_{CHIPH}$, $t_{EPLCL}$, $t_{EPLEPH}$

MEMORY-TO-MEMORY TRANSFERS




RESET

Figure 4. Timing waveforms test circuit. - Continued



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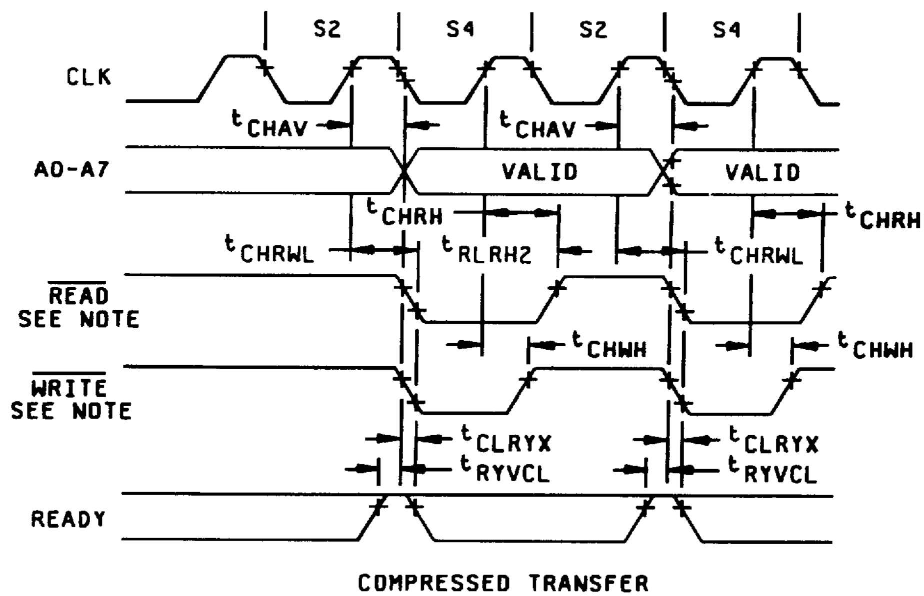


COMPRESSED TRANSFER

Note: READ refers to both IOR and MEMR outputs. WRITE refers to both IOW and MEMW outputs.

Figure 4. Timing waveforms test circuit. - Continued



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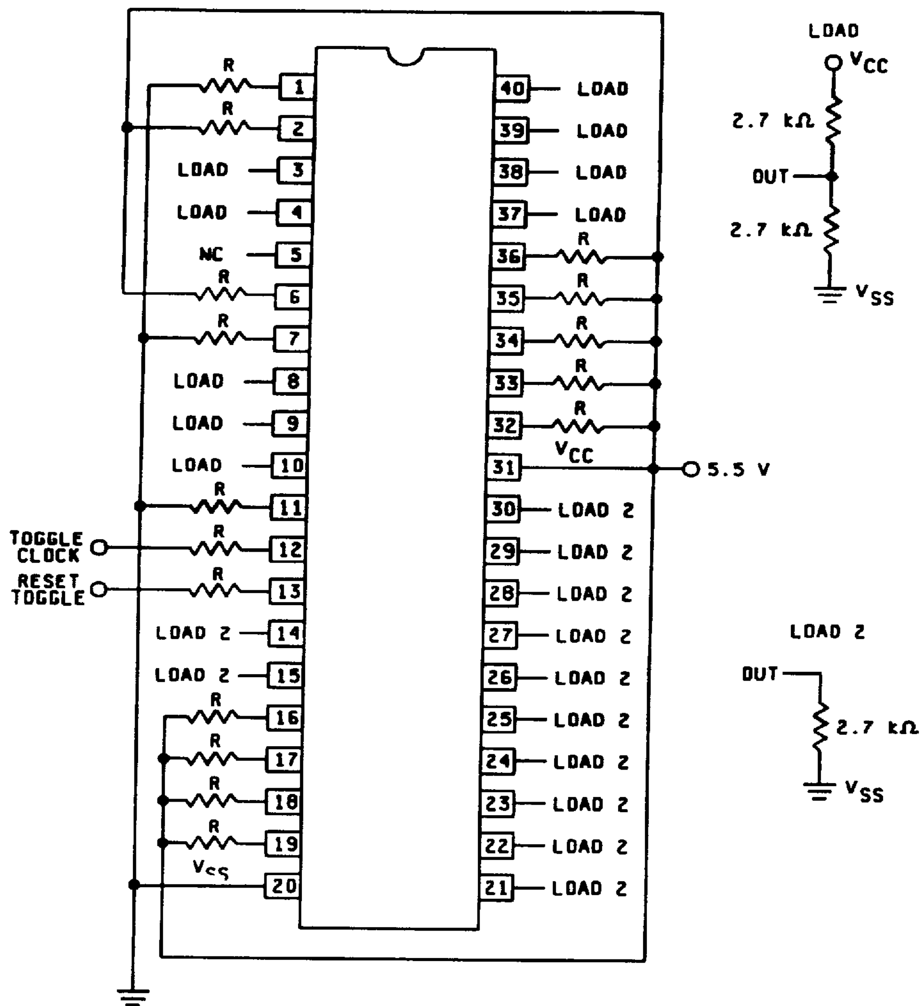


Notes:

1. R = 47kΩ
2. Pins with Load: 3, 4, 8,, 9, 10, 37-40
   Pins with Load2: 14, 15, 21-30
   Pins brought out: 12 (Clock), 13 (Reset)
3. $V_{DD}$ = 5.5 V ± 0.5 V

FIGURE 5. Radiation exposure circuit.



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## 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535, or as modified in the device manufacturers approved Quality Management (QM) plan.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 or as specified in the QM planincluding groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535, permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 ($C_{IN}$, $C_{OUT}$, and $C_{I/O}$ measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.



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TABLE IIA. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-STD-883, TM 5005, table I) | Subgroups (in accordance with MIL-I-38535, table III) | |
|---|---|---|---|
| | Device class M | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | 1,7,9 | 1,7,9 | 1,7,9 |
| Final electrical parameters (see 4.2) | 1,2,3,7,8,9, 1/ 10,11 | 1,2,3,7,8, 1/ 9,10,11 | 1,2,3,7, 2/ 8,9,10,11 3/ |
| Group A test requirements (see 4.4) | 1,2,3,4,7,8,9 10,11 | 1,2,3,4,7,8, 9,10,11 | 1,2,3,4,7,8, 9,10,11 |
| Group C end-point electrical parameters (see 4.4) | 1,2,3,7,8 9,10,11 | 1,2,3,7,8 9,10,11 | 1,2,3,7,8 9,10,11 3/ |
| Group D end-point electrical parameters (see 4.4) | 1,7,9 | 1,7,9 | 1,7,9 |
| Group E end-point electrical parameters (see 4.4) | 1,7,9 | 1,7,9 | 1,7,9 |

1/ PDA applies to subgroup 1 and 7.
2/ PDA applies to subgroups 1, 7 and delta's.
3/ Delta limits as specified in Table IIB herein shall be required where specified and the delta values shall be completed with reference to the zero hour.

TABLE IIB. Burn-in delta parameters (+25°).

| Parameter | Symbol | Delta limits |
|---|---|---|
| Standby power supply current | $I_{DDSB}$ | ±20 µA |
| Output leakage current | $I_{OZL}$, $I_{OZH}$ | ±2 µA |
| Input leakage current | $I_{IH}$, $I_{IL}$ | ±200 nA |
| Output low voltage | $V_{OL}$ | ±80 mV |
| TTL output high voltage | $V_{OH1}$ | ±600 mV |
| CMOS output high voltage | $V_{OH2}$ | ±150 mV |

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.



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4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-I-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (See 1.4). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (See 1.4).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-I-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices (See 1.4). SEP testing shall be performed on technology basis on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \le$ angle $\le 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $\ge$ 100 errors or $\ge 10^6$ ions/cm$^2$.

c. The flux shall be between $10^2$ and $10^5$ ions/cm$^2$/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\ge$ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit $V_{SS}$ terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.



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6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

| Military documentation format | Example PIN under new system | Manufacturing source listing | Document listing |
|---|---|---|---|
| New MIL-H-38534 Standard Microcircuit Drawings | 5962-XXXXXZZ(H or K)YY | QML-38534 | MIL-BUL-103 |
| New MIL-I-38535 Standard Microcircuit Drawings | 5962-XXXXXZZ(Q or V)YY | QML-38535 | MIL-BUL-103 |
| New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings | 5962-XXXXXZZ(M)YY | MIL-BUL-103 | MIL-BUL-103 |

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

6.8 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).



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