Oki Semiconductor

W110 Dual-Speed Ethernet Controller

100Mbps + 10Mbps Ethernet Media Access Controller Mega Macrofunction

DESCRIPTION

The W110 is a 100BASE-T Ethernet Media Access Controller (MAC) mega macrofunction for dual-speed operation (100Mbps/10Mbps) and an MII interface. Implemented in 0.5µm and 0.8µm technologies, the W110 supports a wide range of physical layer (PHY) devices, including both 100Mbps and 10Mbps devices for wired, optical, and wireless networks, operating in half- or full-duplex mode.

The W110 mega macrofunction is available in various configurations, depending upon customer partitioning requirements. The W110 contains two main submodules, called MAC110 and PCS110. The MAC110 submodule contains the key transmit/receive functions and performs the CSMA/CD function specified in ISO/IEC 8802-3: 1993 and the supplemental IEEE standard 802.3u-1995. The PCS110 submodule contains various PHY support modules and MII support.

Potential applications include network interface controllers (NICs), multiport switches, switching routers, hubs, and test equipment.

The MAC110 submodule contains ~10.1k gates. The final top-level gate count is determined by which particular PCS option is chosen by the user. The W110M option (transmit and receive function with MII interface only) contains ~7.1k gates. A gate-level model of the mega macrofunction is available in Verilog or VHDL.

FEATURES

- Support for 10 or 100 Mbps MII-based PHY devices, including:
  - 100BASE-TX
  - 100BASE-FX
  - 100BASE-T4
- Support for TP-PMD and fiber-PMD (FDDI) devices
- Complies with ISO/IEC 802-3:1993 and IEEE std. 802.3u-1995
- Generates transmit/receive statistics vectors
- Autonegotiation support
- Support for ENDEC devices
- Full-duplex Ethernet support
- PCS functions 4B/5B, and scrambling
- Optimized for switching and multi-port applications
- Generic interface supporting various buses, including ISA, PCI, MCA, VLB, SBus, NuBus, SCSI, and MULTIBUS
- Additional submodules available for packet filtering, statistics collection, and bus interface with FIFO

Supported ASIC Families

Family Name	Technology	Family Type
MSM38S0000	0.8µm	TLM Sea of Gates
MSM98S000		TLM Customer Structured Array
MSM12R/32R0000	0.5µm	DLM Sea of Gates
MSM13R/30R0000		TLM Sea of Gates
MSM98R/92R000		TLM Customer Structured Array

Recommended Operating Conditions (V_{SS} = 0V)

Parameter	Symbol	Rated Values			Unit
		Min.	Typ.	Max.	
Power supply voltage (5V operation)	V_{DD}	4.75	5.0	5.25	V
Power supply voltage (3V operation)	V_{DD}	2.7	3.3	3.6	V
Operating temperature	T_j	-40	+25	+85	°C

Mega Macrofunction Characteristics

Mega Macrofunction	Description	Logic Gate Count	Logic Pin Count
W110	Dual-Speed Ethernet MAC	~10,100	163

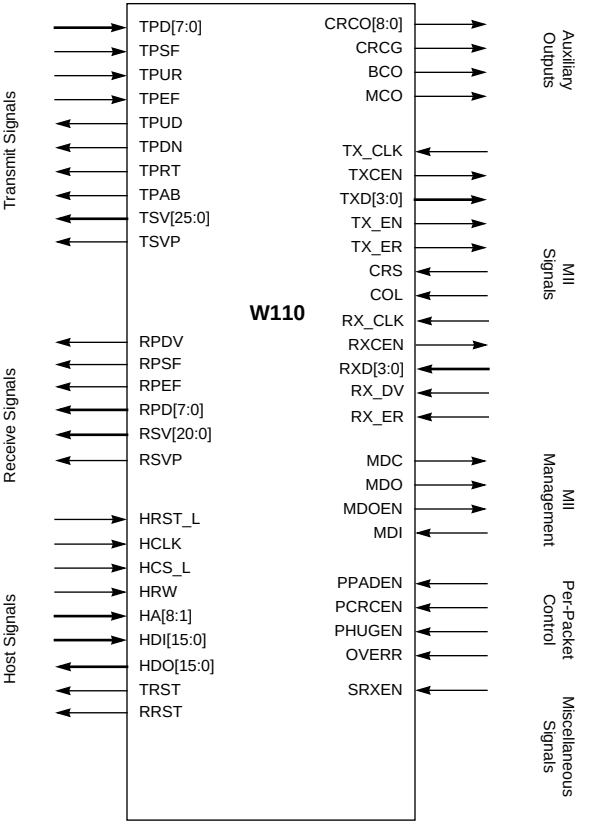

Figure 1. Logic Symbol

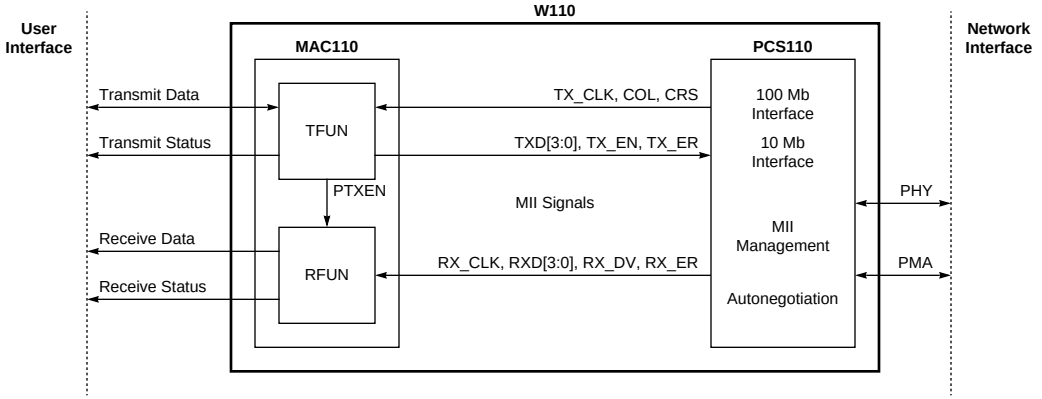

Figure 2. W110 Block Diagram

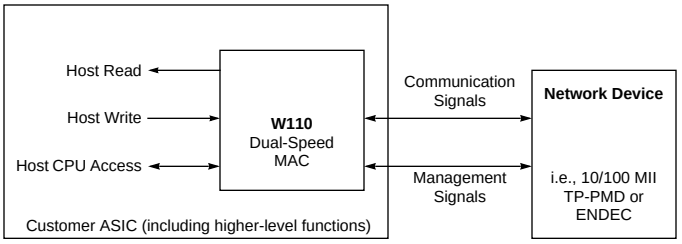

Figure 3. Example of W110 Application: PCI Ethernet Controller

SIGNAL DESCRIPTIONS

Transmit Byte Stream Signals

The following table lists the transmit byte stream signals between host system and the W110 mega macrofunction. All signals are synchronous with the rising edge of TX_CLK unless otherwise indicated. Signal direction is with respect to the W110 function block.

Signal	Type	Assertion	Description
TPD[7:0]	Input	HIGH	Transmit Packet Data. These eight signal lines transfer the transmit data byte from the ASIC's internal logic into the W110 mega macrofunction.
TPSF	Input	HIGH	Transmit Packet Start of Frame. When asserted HIGH, this signal marks the availability of the first byte of a transmit packet on TPD[7:0].
TPUR	Input	HIGH	Transmit Packet Data Under-Run. When asserted HIGH, this signal discontinues transmission.
TPEF	Input	HIGH	Transmit Packet End of Frame. When asserted HIGH, this signal indicates that the last byte of a transmit packet is available on TPD[7:0]
TPUD	Output	HIGH	Transmit Packet Use Data. When asserted HIGH, this signal indicates that data transmission has begun.
TPDN	Output	HIGH	Transmit Packet Done. When asserted HIGH, this signal indicates successful completion of the packet transmission process.
TPRT	Output	HIGH	Transmit Packet Retry. When asserted HIGH, this signal indicates that a collision was encountered during the transmit attempt.
TPAB	Output	HIGH	Transmit Packet Abort. When asserted HIGH, this signal indicates that the W110 has discontinued transmission.
TSV[25:0]	Output	—	Transmit Status Vector. These 26 signals indicate the status of the transmit data byte, as shown below.

Bit	Meaning	Bit	Meaning
25	Transmit OK.	12	Collision count bit 0.
24	TX abort - late collision.	11	Late collision.
23	TX abort - excessive deferral.	10	Transmit byte count bit 10.
22	TX abort - excessive collisions.	9	Transmit byte count bit 9.
21	TX abort due to under-run.	8	Transmit byte count bit 8.
20	TX abort - jumbo.	7	Transmit byte count bit 7.
19	Packet deferred.	6	Transmit byte count bit 6.
18	Broadcast packet transmitted.	5	Transmit byte count bit 5.
17	Multicast packet transmitted.	4	Transmit byte count bit 4.
16	CRC error.	3	Transmit byte count bit 3.
15	Collision count bit 3.	2	Transmit byte count bit 2.
14	Collision count bit 2.	1	Transmit byte count bit 1.
13	Collision count bit 1.	0	Transmit byte count bit 0.

TSVP	Output	HIGH	Transmit Status Vector Pulse. When asserted HIGH, this signal indicates that the transmit byte stream status vector, on TSV[25:0], is valid.

Receive Byte Stream Signals

The following table lists the receive byte stream signals between the host system and the W110 mega macrofunction. All signals are synchronous with the rising edge of the RX_CLK signal. Signal direction is with respect to the W110 function block.

Signal	Type	Assertion	Description
RPDV	Output	HIGH	Receive Packet Data Valid. The W110 mega macrofunction asserts this output HIGH to indicate that the data on RPD[7:0] is valid.
RPSF	Output	HIGH	Receive Packet Start of Frame. The W110 mega macrofunction asserts this output HIGH to indicate that the first data byte of a received packet is available on RPD[7:0]
RPEF	Output	HIGH	Receive Packet End of Frame. The W110 mega macrofunction asserts this output HIGH to indicate that the last byte of a received data packet is available on RPD[7:0]
RPD[7:0]	Output	HIGH	Receive Packet Data. These eight signals carry the received data byte to the ASIC internal logic.
RSV[20:0]	Output	HIGH	Receive Status Vector. These 21 bits indicate the status of the receive packet, as shown below.

Bit	Meaning	Bit	Meaning
20	Carrier event previously seen.	10	Packet length bit 10.
19	Rxdv event previously seen.	9	Packet length bit 9.
18	Receive OK.	8	Packet length bit 8.
17	Broadcast packet.	7	Packet length bit 7.
16	Multicast packet.	6	Packet length bit 6.
15	CRC error.	5	Packet length bit 5.
14	Dribble nibble.	4	Packet length bit 4.
13	Receive code violation.	3	Packet length bit 3.
12	Long packet.	2	Packet length bit 2.
11	Short packet.	1	Packet length bit 1.
		0	Packet length bit 0.

RSVP	Output	HIGH	Receive Status Vector Pulse. When asserted HIGH, this output indicates that the receive packet status is valid on RSV[20:0]

Host Interface Lines

The following table lists the host interface lines that access the W110 mega macrofunction for interfacing to ISA, PCI, MCA, VLB, S-Bus, NuBus, SCSI, and MULTIBUS systems. Signal direction is with respect to the W110 function block.

Signal	Type	Assertion	Description
HCLK	Input	—	Host Clock. The W110 mega macrofunction can use a 25MHz or 33MHz user-selectable clock frequency.
HCS_L	Input	LOW	Host Chip Select. When asserted LOW, this signal enable the host read or host write cycles.
HRW	Input	—	Host Read/Write Select. When asserted LOW, this signal selects a host write cycle. When asserted HIGH, this signal selects a host read cycle.
HA[8:1]	Input	—	Host Address. This address bus selects the address for the host register.
HDI[15:0]	Input	—	Host Write Data. Data on this bus is written into the selected register during a host write cycle.
HDO[15:0]	Output	—	Host Read Data. This bus carries the output data during the host read cycle.
HRST_L	Input	LOW	Host Reset. When external logic asserts this signal LOW, the host resets the MAC subsystem.
TRST	Output	HIGH	Transmit Synchronized Host Reset. The W110 mega macrofunction asserts this signal HIGH relative to TX_CLK to indicate that the W110 has performed a reset after the assertion of HRST_L.
RRST	Output	HIGH	Receive Synchronized Host Reset. The W110 mega macrofunction asserts this signal HIGH relative to RX_CLK to indicate that the W110 has performed a reset after the assertion of HRST_L.

Auxiliary Outputs

The following table lists the control lines used in receive packet filtering. All signals are synchronous with the RX_CLK rising edge. Signal direction is with respect to the W110 function block.

Signal	Type	Assertion	Description
CRCO[8:0]	Output	—	CRC Output. This signals contain CRC data for external hash table lookup. See the W110 data sheet for more information.
CRCG	Output	HIGH	CRC Qualifier. This signal validates the CRC output to the external hash table.
BCO	Output	HIGH	Broadcast Packet Indicator. When asserted HIGH, this signal indicates that the received data is a broadcast packet.
MCO	Output	HIGH	Multicast Packet Indicator. When asserted HIGH, this signal indicates that the received data is a multicast packet.

MII Signals

The MII interface signals are listed below. Signal direction is with respect to the W110 function block. See IEEE 802.3u standard documentation for further information.

Signal	Type	Assertion	Description
TX_CLK	Input	—	Transmit Symbol Clock. This transmit nibble or symbol clock input is derived from the PHY layer. The following table indicates the frequency and type of Transmit Symbol Clock for various PHY options.
TXCEN	Output	HIGH	Transmit Clock Enable. In 10-Mbps mode, TXCEN is the 10-MHz ENDEC clock divided by four. In 100-Mbps mode, the W110 asserts TXCEN HIGH.
TXD[3:0]	Output	—	Transmit Nibble Data. This bus outputs data from the transmit function, synchronous with TX_CLK
TX_EN	Output	HIGH	Transmit Enable. The transmit function outputs this enable signal, synchronous with TX_CLK.
TX_ER	Output	HIGH	Transmit Error. When asserted HIGH, this signal indicates a transmission error. This is a synchronous signal with the rising edge of TX_CLK.
CRS	Input	HIGH	Carrier Sense. This input receives information via the MII multiplex and is considered to be asynchronous.
COL	Input	HIGH	Collision. This input transmits information via the MII multiplex and is considered to be asynchronous. For half-duplex transceivers, the assertion of this signal indicates simultaneous transmission and reception. Full-duplex transceivers never activate this signal.
RX_CLK	Input	—	Receive Symbol Clock. The PHY layer produces this symbol clock or receive nibble input. The following table indicates the frequency and type of Receive Symbol Clock for various PHY options.
RXCEN	Output	HIGH	Receive Clock Enable. In 10-Mbps mode, RXCEN is the 10-MHz ENDEC clock divided by four. In 100-Mbps mode, the W110 assert SRXCEN HIGH.
RXD[3:0]	Input	—	Receive Nibble Data. This synchronous input indicates that nibble data has been received on the rising edge of RX_CLK.
RX_DV	Input	HIGH	Receive Data Valid. This synchronous input validates received data on the rising edge of RX_CLK.
RX_ER	Input	HIGH	Receive Error. The W110 reads this signal input on the rising edge of RX_CLK. The presence of receive errors usually indicates bad wiring.

TX_CLK:

Mode	TX_CLK	TXCEN
100-Mbps MII PHY	25 MHz	HIGH
10-Mbps MII PHY	2.5 MHz	HIGH
10-Mbps ENDEC	10 MHz	2.5 MHz ($^1/_4$ duty cycle)

RX_CLK:

Mode	MRXC	RXCEN
100-Mbps MII PHY	25 MHz	HIGH
10-Mbps MII PHY	2.5 MHz	HIGH
10-Mbps ENDEC	10 MHz	2.5 MHz ($^1/_4$ duty cycle)

MII Management Signals

The table below lists MII management signals. Signal direction is with respect to the W110 function block. See the IEEE 802.3u standard documentation for further information.

Signal	Type	Assertion	Description
MDC	Output	HIGH	Management Data Clock. The W110 mega macrocell derives this signal from the HCLK input.
MDO	Output	HIGH	Management Data Output. To form the external bidirectional MII signal MDIO, combine this signal with MDI in a chip I/O buffer. Use the MDOEN signal to 3-state the I/O buffer output.
MDI	Input	HIGH	Management Data Input. To form the external bidirectional signal MDIO, combine this signal with MDO in a chip I/O buffer. Use the MDOEN signal to 3-state the I/O buffer output.
MDOEN	Output	HIGH	Management Data Output Enable. Use this output to 3-state the MDIO I/O buffer output, formed from combining the MDI input and MDO output.

Per-Packet Control

The following signals override the programmed configuration on a per-packet basis. Signal direction is with respect to the W110.

Signal	Type	Assertion	Description
PPADEN	Input	—	Per-Packet Pad Enable. If OVERR is “1” then the value of PPADEN is input to TFUN.
PCRCEN	Input	—	Per-Packet CRC Enable. If OVERR is “1” then the value of PCRCEN is input to TFUN.
PHUGEN	Input	—	Per-Packet Huge Enable. If OVERR is “1” then the value of PHUGEN is input to TFUN.
OVERR	Input	—	Per-Packet OverRide. When logic external to the W110 mega macrofunction sets this bit to “1”, then the per-packet controls are input to TFUN. When set to “0”, then the values from an internal configuration register are gated to TFUN instead.

Miscellaneous Signals

The following signals provide additional functionality for the W110 mega macrofunction. Signal direction is with respect to the W110.

Signal	Type	Assertion	Description
SRXEN	Input	—	Synchronized Receive Enable. When logic external to the W110 mega macrofunction sets this bit to “1”, then RFUN outputs received frame data. When set to “0”, then RFUN does not output received frame data.

FUNCTIONAL DESCRIPTION

The W110 consists of five function blocks which are partitioned into the two main submodules, MAC110 and PCS110.

- The MAC110 module contains the Ethernet MAC functions in two submodules, called TFUN and RFUN.
  - The MAC110 TFUN submodule contains the MAC transmit functions.
  - The MAC110 RFUN submodule contains the MAC receive functions.

  All ASIC implementations using the W110 must include both the TFUN and RFUN modules.
- The PCS110 module contains the I/O functions. The PCS110 module contains a collection of submodules that support connectivity to the network media through a variety of PHY devices. A given implementation may require one or all of these submodules, depending on the flexibility required, to support a 100-Mbps interface, 10-Mbps interface, and/or MII.

Included in the MAC110 and PCS110 modules is supporting logic for the Host Interface. If the W110 is used to create a multiport device like a switch, this interface will typically be to the embedded processor. In the case of an end-station implementation, this might be the end-station bus. Again, the Host Interface needs to be created for the individual application.

Management Statistics

The W110 transmit and receive functions do not implement large numbers of counters for statistics collection. The W110 mega macrocell uses the vector-generation method instead. The vector technique has the effect of simplifying the timing of lots of asynchronous events.

The vector method is also more efficient in multiple-MAC systems, because a single logic block can perform statistics accumulation for all of the MACs in the system, reducing gate count and improving processing efficiency. However, the designer must then create a statistics gathering mechanism outside the MAC on a case-by-case basis.

Oki supports an optional module to perform statistics collection. Please contact Oki ASIC Application Engineering for more information.

Applications

Switch Building Blocks

Oki has optimized the W110 for use in multiple-MAC applications. These applications include switches, multi-port interface cards and routers. *Figure 4* shows a typical application where the W110 is used as a building block for an eight-port switch.

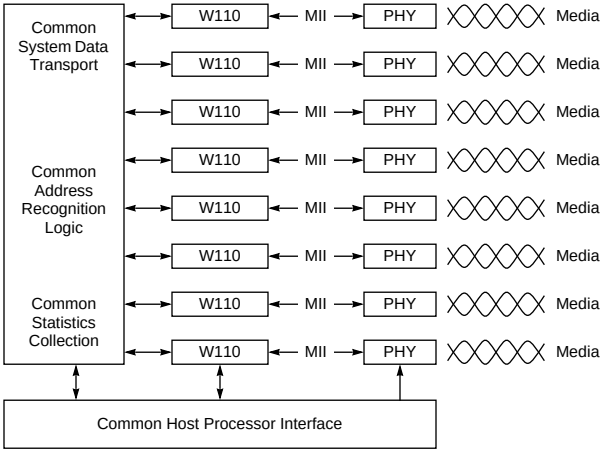

Figure 4. Using the W110 in an Eight-Port Ethernet Switch

The exact nature of the common sections for system data transport, address recognition and statistics will be application dependent. The W110 has enough built-in flexibility to cover almost any system concept.

The PHY devices are currently supported externally to the design. A logical MII supports the external interface for the network.

Network Interface Controllers

The example in *Figure 5* below shows the W110 implemented in a network controller IC. The IC is used to create a PCI-based network controller for PCs.

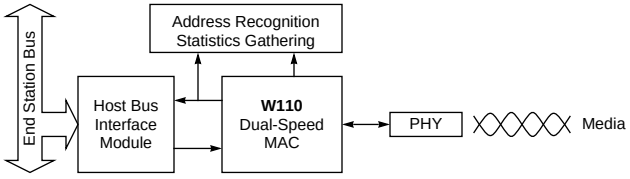

Figure 5. Single MAC Implementation

This application shows that address resolution for the W110 occurs after the data has left the MAC as a byte stream. This approach makes little difference in a single-MAC application. The approach does improve the design of multiple-MAC applications.

Management statistics are generated as vectors by the W110. A mechanism is required externally to collect these vectors and parse the information appropriately. Oki can provide an additional module to perform statistics collection.

The generalized byte streams of data may be interfaced to any bus type. Depending on the sophistication and the bus, the bus interface module might range from a trivial to a very complex implementation. The W110 can be implemented with ISA, PCI, MCA, VLB, SBus, NuBus, SCSI, Multibus and many more.

Physical Layer Options

A logical MII forms the output from the MAC, sending data to the network, and the input to the MAC, receiving data from the network. The logical MII provides a uniform interface for all possible implementations of the MAC. A combination of the supporting I/O modules and the I/O multiplexer converts the logical MII signals to the appropriate driver levels. There are several different possible final interfaces, including true MII devices at 100 Mbps or 10 Mbps, TP-PMD devices such as the PDT/PDR combination, and 10 Mbps ENDEC devices.

A given implementation of the W110 may use any combination of these outputs. The more output types used in the design, the more complex the multiplexing circuits must be. *Figure 6* shows the data flows for each type of device implementation.

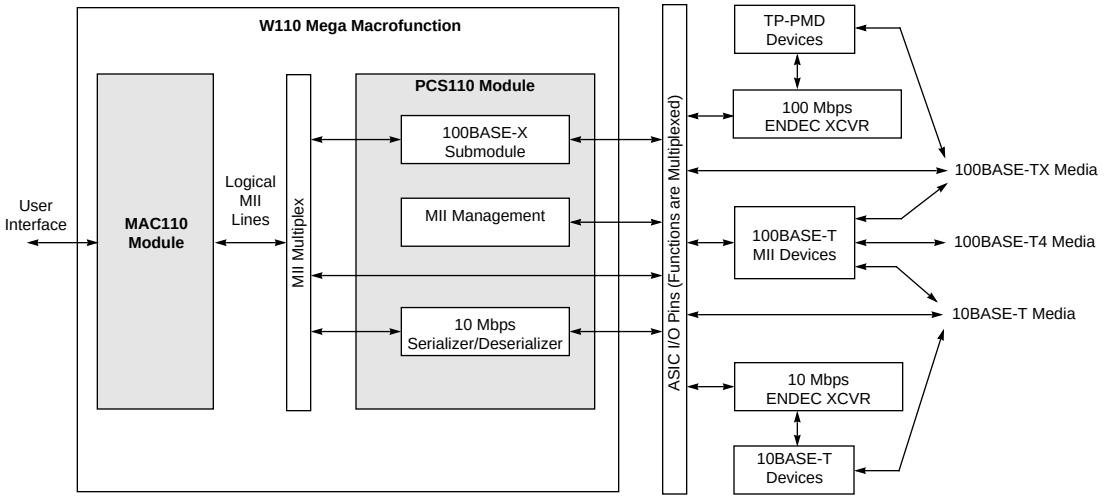

Figure 6. MII and I/O Multiplex

Data Paths

The diagrams below show the transmit packet data flow path and the receive packet data flow path. The host system supplies data for transmission to the network as a stream of bytes. The transmit function block performs the Ethernet MAC operations. The output of the transmit function flows across the logical MII lines to the MII multiplexer. If the external PHY device is a MII-based PHY, the MII multiplex and I/O multiplex blocks connect the internal MII lines directly to the output pins. When using an external TP-PMD PHY device, the MII multiplexer routes the internal MII lines to the 100BASE-X submodule. The output of the 100BASE-X submodule is connected to the output pins via the I/O multiplexer.

If an external 10BASE-T ENDEC is being used, the MII multiplexer routes the internal MII lines to the 10Base-T Module. The I/O multiplexer connects the output of the module to the output pins.

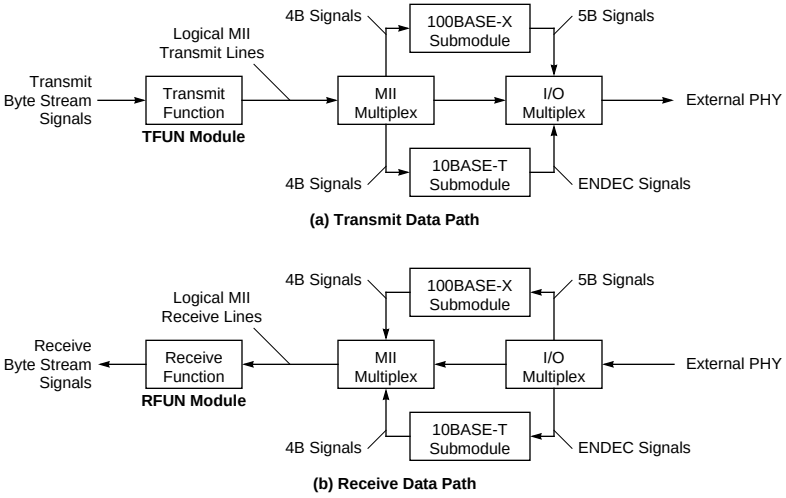

Figure 7. Transmit and Receive Data Paths

Similarly, the receive data path flows through the appropriate modules, routed by the I/O multiplexer. The MII multiplexer then connects the appropriate module outputs to the receive function. The receive function performs the Ethernet MAC operations.

The MII Interface

The W110 communicates with external PHY devices through the logical MII interface. The logical MII is divided into two signal sets. One set handles data transmission and reception while the second set handles MII management functions.

Figure 8. MII Data and Management Signal Sets

Within the W110, the data function are handled by the TFUN and RFUN modules. The MII management set is handled by the MII module. Host access to the management interface is on a word basis through the normal host interface. The interface between the MII and the external PHY is a clocked serial interface as defined in the IEEE 802.3u standard.

Statistics Gathering and Vectors

Most activity in a MAC is centered around major events such as completion of packet reception or completion of packet transmission attempts. When these major events occur, the W110 generates a statistics vector, summarizing the detailed results associated with the event. The vector can be latched into a separate statistics collection block. A vector is latched once for each major event.

This vector approach reduces the requirement for individual synchronization of many individual events. The approach also reduces the gate count by eliminating the need for flip-flops scattered around the MAC design.

When multiple-MAC designs are involved, the statistics collecting block may be common for all MACs. Again, the vector approach reduces the complexity of the design and the gate count. Central statistics gathering is also easier than distributed gathering when it comes to parsing cumulative and derivative statistics.

There are generally two different vectors, one for receive and one for transmit. Vectors may be designed to include or exclude as many different parameters as a customer requires. Examples of vectors and parameters are shown in the following table.

Statistics Vector Parameters

Transmit Status Bit				Receive Status Bit		Transmit Status Bit	
Bit	Meaning	Bit	Meaning	Bit	Meaning	Bit	Meaning
25	Transmit OK.	12	Collision count bit 0.	20	Carrier event previously seen.	10	Packet length bit 10.
24	TX abort - late collision.	11	Late collision.	19	Rxdv event previously seen.	9	Packet length bit 9.
23	TX abort - excessive deferral.	10	Transmit byte count bit 10.	18	Receive OK.	8	Packet length bit 8.
22	TX abort - excessive collisions.	9	Transmit byte count bit 9.	17	Broadcast packet.	7	Packet length bit 7.
21	TX abort due to underrun.	8	Transmit byte count bit 8.	16	Multicast packet.	6	Packet length bit 6.
20	TX abort - jumbo.	7	Transmit byte count bit 7.	15	CRC error.	5	Packet length bit 5.
19	Packet deferred.	6	Transmit byte count bit 6.	14	Dribble nibble.	4	Packet length bit 4.
18	Broadcast packet transmitted.	5	Transmit byte count bit 5.	13	Receive code violation.	3	Packet length bit 3.
17	Multicast packet transmitted.	4	Transmit byte count bit 4.	12	Long packet.	2	Packet length bit 2.
16	CRC error.	3	Transmit byte count bit 3.	11	Short packet.	1	Packet length bit 1.
15	Collision count bit 3.	2	Transmit byte count bit 2.	—	—	0	Packet length bit 0.
14	Collision count bit 2.	1	Transmit byte count bit 1.	—	—	—	—
13	Collision count bit 1.	0	Transmit byte count bit 0.	—	—	—	—

In the above implementation example, the transmit vector is 26 bits long and the receive vector is 21 bits long. Vector implementations are not limited to these parameters or lengths.

Address Recognition

The W110 does not perform address recognition in the body of the MAC. Address recognition is performed downstream on the receive byte stream. This arrangement improves the design of multiple-MAC implementations. In multiple-MAC implementations, the receive byte streams from several MACs can be directed to a central address recognition logic block. This common arrangement reduces gate count, speeds processing and improves management access and control. OKI does support a separate block to perform address recognition. Please contact OKI ASIC Application Engineering for more information.

Host Interface Options

The W110 connects to a host system of a customer-specified type. Many different types of host interface may be used. Examples include sophisticated bus-mastering types such as PCI, shared memory, ring-buffer, DMA and FIFO-based designs. In a switch system, the host generally is an embedded CPU or a backplane switching fabric. In a general network interface, the host might be a general purpose computer communicating over the computer bus. The W110 communicates to the host system using generalized receive and transmit byte streams. Oki can provide an additional module for interfacing to 16-, 32-, or 64-bit host interfaces with DMA and FIFO.

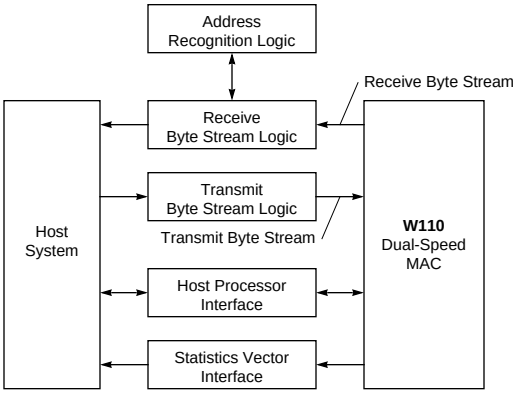

Figure 9. Example of W110 Interface to Host System

Testing

OKI Semiconductor provides appropriate test vectors to verify the timing and functionality of each design implementation. OKI also creates appropriate test bench modules during development. Contact the Oki ASIC Application Engineering Department for more information.

Glossary

Term	Definition
10BASE-T	10Mbps UTP transceiver type. ISO/IEC 8802-3 physical layer and media type specification for 10Mbps baseband data rate using two pairs of UTP wire.
100BASE-T	100Mbps transceiver type. IEEE 802.3u physical layer and media type specification for 100Mbps baseband data rate using two or four pairs of Category 5 or Category 3 (respectively) UTP wire.
4B	4 Bit.
5B	5 Bit.
ANSI	American National Standards Institute.
ASIC	Application Specific Integrated Circuit.
AUTONEG	Autonegotiation. The ability to differentiate between 10Mbps and 100Mbps connections, and automatically establish communications with the remote unit.
CPU	Central Processing Unit.
CRC	Cyclic Redundancy Check. A logical coding system for error detection and correction on an established connection.
DMA	Direct Memory Access. A method of accessing memory where a peripheral will “steal” bus cycles from the CPU. During these cycles, the peripheral will directly access memory.
ECU	Embedded Control Unit.
ENDEC	ENcoder-DECoder. A device used to convert an Ethernet bit stream into the Manchester-encoded data required for transmission on a LAN, and vice-versa.
FDDI	Fiber Distributed Data Interface. A LAN technology specifying a data rate of 100 Mbps which has sophisticated redundancy features. The PHY of FDDI was used as the basis for the development of the X components of 100BASE-T (100BASE-TX and 100BASE-FX).
FIFO	First-In First-Out Queue. A buffer mechanism that ensures the order of data is maintained. FIFOs are asynchronous.
HDL	Hardware Description Language. Term for logical descriptive languages used in chip design.
IEEE	Institute of Electrical and Electronics Engineers. Professional engineering society that promotes formal standards through the IEEE Standards Board. The actual work of creating standards is conducted through a framework of committees, sub-committees and task forces. The most relevant committee for this document is the LAMS (LAN-MAN Standards Committee) which is responsible for the Ethernet standard IEEE 802.3.
I/O	Input/Output.
ISO	International Organization for Standardization.
IETF	Internet Engineering Task Force. The body charged with setting the operating standards for the Internet.
LAN	Local Area Network.
LAMS	LAN-MAN Standards committee.
MAC	Media Access Control. Protocol used to control access to the physical layer by upper communications layers.
MAN	Metropolitan Area Network.
MIB	Management Information Base. A collection of management variables linked by some common factor.
MII	Medium Independent Interface. The interface between the Ethernet MAC and PHY layers as defined in IEEE 802.3u. The MII separates the MAC function (common to all implementations) from the PHY components which vary with the type of medium being used.
Packet	A collection of data and control information. A packet makes up a recognizable single unit that can be dealt with by LAN and communications systems. Packets generally have variable length as opposed to cells which are fixed length. Rules for packet construction vary from system to system and protocol to protocol.

Glossary (Continued)

Term	Definition
PDT/PDR	**Physical Data Transmitter/Physical Data Receiver. A pair of devices that provide parallel-to-serial and serial-to-parallel conversions. PDT accepts parallel input of 5B symbols and converts them into a serial NRZI data stream at 125M baud. The PDR provides the reverse function.**
PHY	**PHYsical layer device. A PHY usually consists of the analog and supporting components of a transmission scheme associated with a particular medium.**
PLD	**Programmable Logic Device.**
PMA	**Physical Medium Attachment. A sublayer of the PHY responsible for analog functions, such as transmit wave shaping (the T4 standard).**
PMD	**Physical Medium Dependent (interface). A sublayer of the PHY layer responsible for analog functions, such as receive data discrimination (TX/FX standards).**
PQFP	**Plastic Quad Flat Pack.**
RFC	**Request For Comments. The name given to standards and discussion documents in the IETF.**
RMON	**Remote MONitoring MIB. A MIB covering nine groups of management variables associated with network probe devices. RMON is defined by RFC 1757.**
SRAM	**Static Random Access Memory.**
TP	**Twisted Pair. Used to describe copper cables where pairs of wires are twisted around each other to provide balanced electrical characteristics.**
TP-PMD	**Twisted-Pair PMD. The name given to the PMD layer of the copper version of the FDDI specification.**
UTP	**Unshielded Twisted Pair. The standard wire interconnection medium used for thin Ethernet 10Mbps connectivity.**
VHDL	**Very high-speed integrated circuit Hardware Description Language. One of several HDLs in use. VHDL has been standardized by the IEEE.**
XCVR	**Transceiver.**

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