Data Quantizer

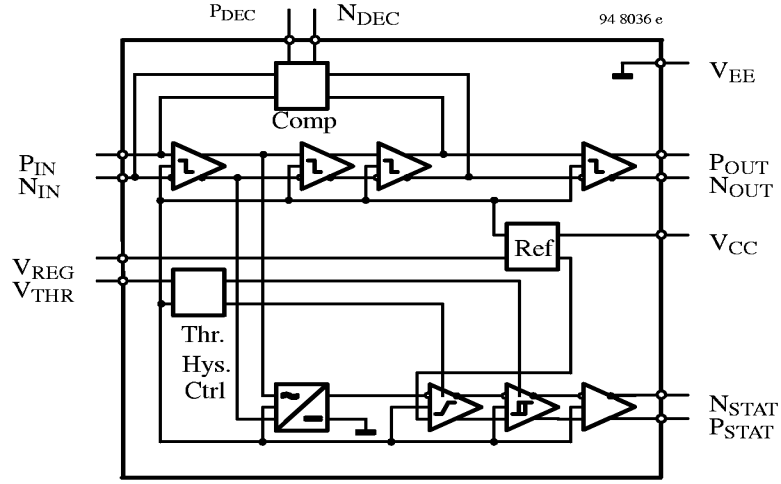
Description

U6792B-E data quantizer is a low-noise, wideband IC for signal recovering in fiber optic receiver systems. It contains a three stage wideband limiting amplifier which accepts input signal as low as 1.5 mV_{pp} with a 60 dB dynamic range. This sensitivity is achieved by using a dc restoration feedback loop which nulls any offset voltage produced in the limiting amplifier. The ECL output buffer can drive 50 Ω loads to –2 V. The minimum signal discriminator circuit provides a link monitor function with a user selectable threshold voltage.

Features

- 200-MHz minimum bandwidth allows for data rates of up to 200 Mb/s
- Low-noise design: 25 µV RMS over 200-MHz range
- Adjustable link monitor function
- Wide 60-dB input dynamic range
- 2.5 ns minimum input pulse
- Low-power design: 30 mA maximum without load
- Regulated voltage output for supply voltage independent threshold adjust
- Available in SO-16 package or chip form

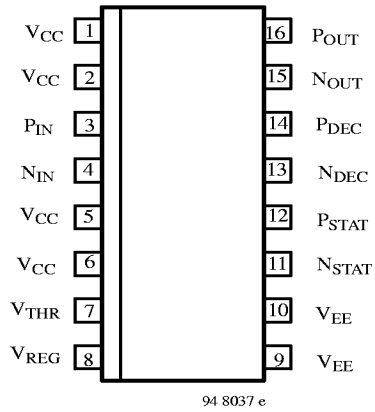
Block Diagram



U6792B-E

Pin Description

Pin	Symbol	Function
1, 2	V_{CC}	Positive supply voltage
3,4	P_{IN}, N_{IN}	Capacitively coupled to the input source or to ground (the input resistance is approximately 5 kΩ)
5, 6	V_{CC}	Positive supply voltage
7	V_{THR}	Threshold adjusting for the link monitor circuit
8	V_{REG}	3.1 V reference voltage with respect to V_{EE} (should be decoupled with min. 10 nF to V_{EE}.)
9, 10	V_{EE}	Negative supply voltage
11	N_{STAT}	Negative ECL compatible link monitor output
12	P_{STAT}	Positive ECL compatible link monitor output
13,14	P_{DEC}, N_{DEC}	A decoupling capacitor must be connected between these pins
15	N_{OUT}	Negative ECL compatible output
16	P_{OUT}	Positive ECL compatible output



Absolute Maximum Ratings

Parameters		Symbol	Value	Unit
Supply voltage	Pins 9 and 10	V_{EE}	6.0	V
Input voltage	Pins 3, 4, 8, 13 and 14	V_i	V_{EE} to GND	V
Junction temperature		T_j	125	°C
Storage temperature range		T_{stg}	–40 to +125	°C

Operating Range

Parameters		Symbol	Value	Unit
Supply voltage range	Pins 9 and 10	V_{EE}	4.5 to 5.7	V
Ambient temperature range		T_{amb}	–40 to +85	K/W

Thermal Resistance

Parameters		Symbol	Value	Unit
Junction ambient	SO–16	R_{thJA}	typ. 120	°C

DC Electrical Characteristics

Operating conditions: T_{amb} = 0°C to 70°C, V_{EE} = –5.2V ± 10%

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
V_{EE} supply current	Unloaded outputs	I_{EE}	–30	–23		mA
Reference voltage *		V_{REG}	3.10	3.15	3.20	V
V_{REG} output current		I_{EE}			100	µA
Voltage at V_{THR} *	Left open	V_{THRO}		0.45		V
Voltage Range of V_{THR}		V_{THRR}	0		V_{REG}	V
Input offset voltage		V_{OS}			1	mV
Input resistance	$V_{IN,NIM}$	$R_{IN,NIN}$		5		kΩ
Output high level at P_{OUT}, N_{OUT}, P_{STAT}, N_{STAT}	With 50 Ω load to –2 V	V_{OH}	–0.98		–0.7	V
Output low level at P_{OUT}, N_{OUT}, P_{STAT}, N_{STA}	With 50 Ω load to –2 V	V_{OL}	–1.89		–1.62	V
Hysteresis of monitor comparator	Over entire range of V_{THR}	V_{HYS}	3	4		dB

* With reference to V_{EE}

AC Electrical Characteristics

Operating conditions: T_{amb} = 0°C to 70°C, V_{EE} = –5.2V ± 10%

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Input voltage range		V_{IN}	1.5		1500	mV_{pp}
Input reference noise		N_T		25		µV
Rise time at P_{OUT}, N_{OUT}, P_{STAT}, N_{STAT}	With 50 Ω load to –2 V	t_r	1.1		1.9	ns
Fall time at P_{OUT}, N_{OUT}, P_{STAT}, N_{STA}	With 50 Ω load to –2 V	t_f	1.1		1.9	ns
Propagation time		t_{pd}	2		4	ns
Bandwidth		BW	200			MHz

Functional Description

Amplifier Stage

This data quantizer has a three stage limiting amplifier with an input common mode range of V_{EE} +1.8 V to V_{CC} –1.0 V. Maximum sensitivity is achieved through the use of a dc restoration feedback loop and ac coupling the input. When ac coupled, the input dc bias voltage is set by the limiting amplifier itself at about –2.1 V. The differential input requires two capacitors of equal value. For single ended operation, one of the coupling capacitors has to be connected to ground.

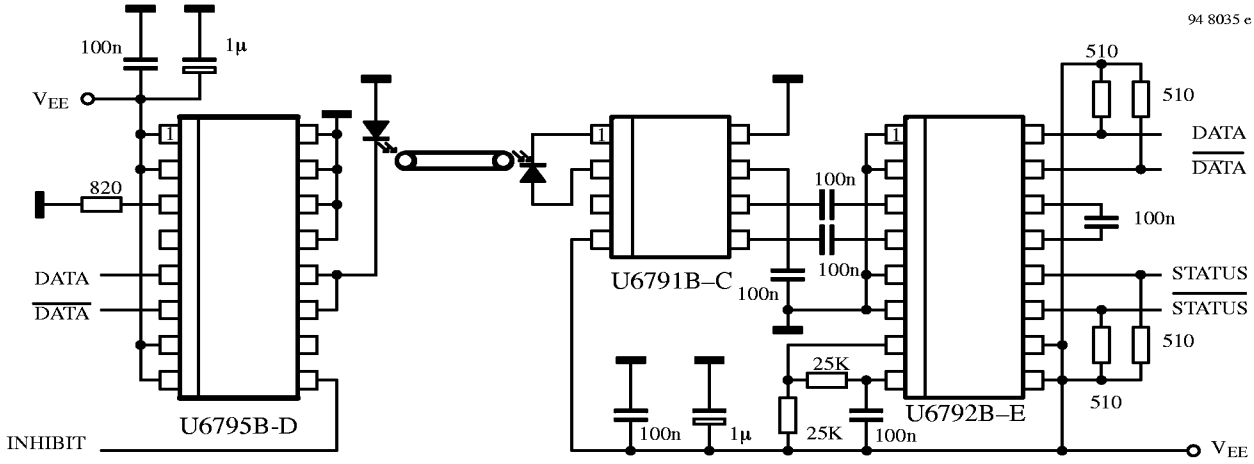
An external capacitor between P_{DEC} and N_{DEC} is used to store the internal offset voltage. The value of this capacitor is not critical. In order to avoid stability problems, the value of this capacitor should be at least the same as the coupling capacitors.

Link Monitor

The link monitor function is implemented by the minimum signal discriminator and the threshold generator circuits. The purpose of this function is to monitor the input signal and to provide a status signal indicating when the input signal falls below or rises above a preset voltage level. This is done by peak detecting the output of the first stage of the limiting amplifier and comparing this level with the internal threshold voltage set by V_{THR}.

If V_{THR} is left open, the typical threshold level is 2.85 mV. The on–chip reference voltage, V_{REG}, can be used to adjust the voltage at V_{THR} by dividing V_{REG} with a resistor string.

Typical Application



Typical Characteristics (T_{amb} = 25°C)

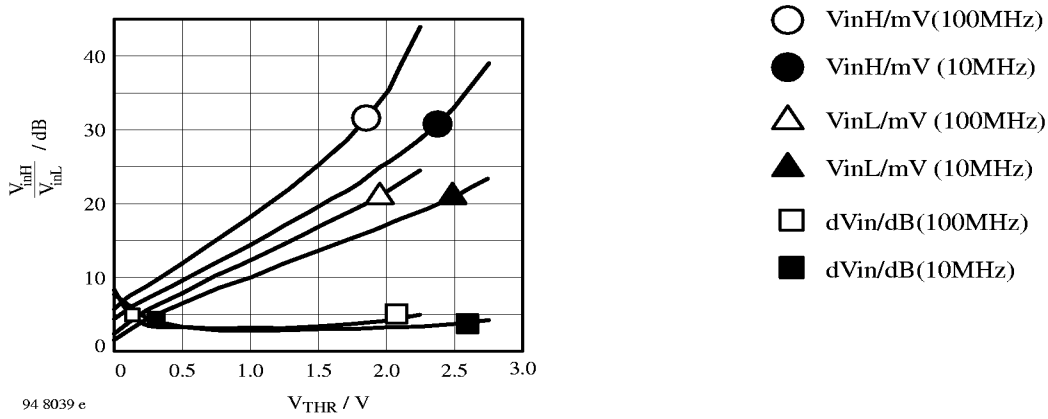


Figure 1. Threshold levels and hysteresis vs. threshold voltage

Dimensions in mm

Package: SO 16