SSI 32R115
2, 4, 5-Channel Read/Write Device

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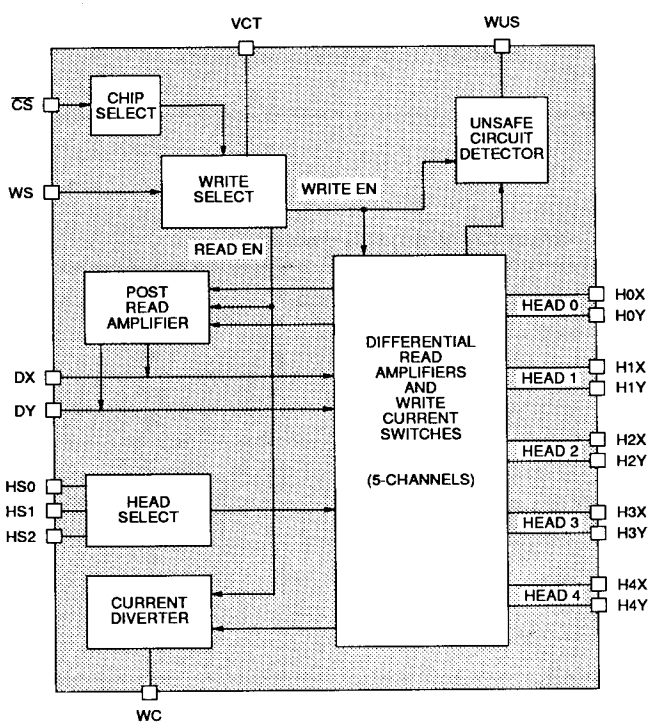
DESCRIPTION

The SSI 32R115 is a monolithic bipolar integrated circuit designed for use with 8-inch and 5-1/4-inch Winchester disk drive magnetic recording heads. The circuit interfaces with up to five magnetic recording heads providing the required read/write electronic functions as well as various control and data protect functions. The circuit operates on +5 volt and -5 volt (or -5.2 volt) power and is available in a variety of packages.

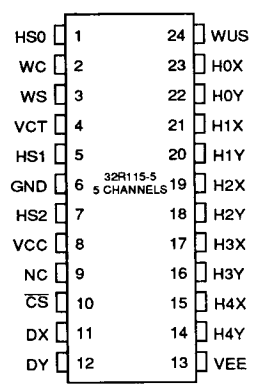
FEATURES

- Electrically compatible with 8-inch and 5-1/4-inch Winchester disk drive magnetic recording heads
- Supports up to five recording heads per circuit
- Detects and indicates unsafe write conditions
- On-chip current diverter eliminates the need for external write current switching
- Control signals are TTL compatible
- Operates on standard +5 volt and -5 volt (or -5.2 volt) power sources

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

WRITE MODE

With both the chip select and write select signals activated, SSI 32R115 is switched to the write mode and the circuit operates as a differential current switch. The center tap head voltage (VCT) is turned on, the unsafe circuit detector is activated, and the current diverter is disabled. The head select signals (HS0, HS1, HS2) select one of five differential current switches. The selected current switch senses the polarity of the data input signal (DX–DY) and gates write current to the corresponding side of the head (HX or HNY). Head overshoot voltages that occur during normal write operation are sensed to determine safe or unsafe head circuit conditions. The detector senses the following unsafe conditions: no data transitions, head open, or no write current.

READ MODE

With chip select active and write select disabled, the SSI 32R115 is switched to the read mode and the circuit operates as a differential amplifier. The center tap head voltage is turned off, the unsafe circuit detector is deactivated, and the write current diverter is enabled. The differential head input signal (HX–HY), selected by the head select signals, is amplified by a differential read amplifier and appears as a differential output signal on the data lines (DX, DY).

During the read and idle modes, the on-chip current diverter circuit prevents write current from flowing in the head circuits. Therefore, external gating of the write current source is not required.

TABLE 1: Head Select

HEAD	HS2	HS1	HS0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0

Note: Invalid Head Select input codes (5, 6 and 7) have the effect of not selecting any heads.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
Positive Supply Voltage, VCC	6	V
Negative Supply Voltage, VEE	-6	V
Write Current (IWC)	70	mA
Operating Junction Temperature	25 to 135	°C
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering, 10 SEC)	260	°C
INPUT VOLTAGES		
Head Select (HS)	-0.4 to VCC +0.3	V
Unsafe (US) (IHUS ≤ 15 mA)	-0.3 to VCC +0.3	V
Write Current (WC) Voltage in read idle modes. (Write mode must be current limited to -70 mA)	VEE -0.3 to 0.3	V

ABSOLUTE MAXIMUM RATINGS (Continued)

PARAMETER	RATING	UNIT
INPUT VOLTAGES (Continued)		
Data (DX, DY)	VEE to 0.3	V
Chip Select ($\overline{CS}$)	-0.4 to VCC +0.3	V
Write Select ($\overline{WS}$)	-0.4 to VCC +0.3	V

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
DC Supply Voltage	VCC	4.75	5	5.25	V
DC Supply Voltage	VEE	-5.5	-5	-4.75	V
Write Current (0-pk)	IWC	-30	-45	-50	mA
Head Inductance	LH		10		µH
Junction Temperature Range	Tj	25		135	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Total Power Dissipation (PD)	Write Mode, IWC ≤ 45 mA, Tj ≥ 125 °C			700	mW
Positive Supply Current (ICC)	Read/Write Mode			35 + IWC	mA
Positive Supply Current (ICC)	Idle Mode			10	mA
Negative Supply Current (IEE)	Read/Write Mode	-65			mA
Negative Supply Current (IEE)	Idle Mode	-10			mA

LOGIC SIGNALS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Chip Select Low voltage (VLCS)	Read or Write Mode	-0.3		0.8	V
Chip Select Low Current (ILCS)	VLCS = 0V	-2.4			mA
Chip Select High Current (IHCS)	Idle Mode	-250			µA
Write Select Low Voltage (VLWS)	Write or Idle Mode	-0.3		0.8	V
Write Select Low Current (ILWS)	VLWS = 0V	-3.2			mA
Write Select High Current (IHWS)	Read or Idle Mode	-250			µA

LOGIC SIGNALS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Head Select High Level Voltage (VHHS)		2.0		VCC	V
Head Select High Level Current (IHHS)	VHHS = VCC			100	µA
Head Select Low Level Voltage (VLHS)		-0.3		0.8	V
Head Select Low Level Current (ILHS)	VLHS = 0V	-0.6			mA
Unsafe Low Level Voltage (VLUS)*	ILUS = 8 mA (Denotes Unsafe Condition)			0.5	V
Unsafe High Level Current (IHUS)*	VHUS = 5.0V (Denotes Safe Condition)			100	µA
*Note: Unsafe is an open collector output.					

READ MODE (Tests performed with 50 load resistors from DX and DY to ground.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Common Mode Range		-0.6		0.1	V
Total Input Bias Current	-0.6V ≤ Vin ≤ 0.1V			60	µA
Differential Voltage Gain	Vin = 1 mVpp, f = 300 KHz	26		52	V/V
Voltage Bandwidth (-3dB)	Zs ≤ 10Ω, Vin = 1 mVpp, f midband = 300 KHz	30			MHz
Input Noise Voltage	Zs = 0, Vin = 0V, Power Bandwidth = 15 MHz			7	µVrms
Differential Input Capacitance	Vin = 0, f = 5 MHz			20	pF
Differential Input Resistance (Internal Damping Resistor)	Vin =0, f = 300 KHz	560		1070	Ω
Output Offset Voltage				120	mV
Differential Head Current	IWC = 45 mA, LH = 10 µH, f = 2 MHz			2	mAp
Output Common Mode Voltage		-0.4		-.125	V
Single Ended Output Resistance	f = 300 KHz	10			KΩ
Single Ended Output Capacitance				10	pF
Dynamic Range	DC input voltage where the AC gain falls to 90% of its 0VDC input value (Measured with 0.5 mVpp AC input voltage)	2			mVp
Common Mode Rejection Ratio	Vin = 100 mVpp, 0VDC, f = 5 MHz	50			dB

READ MODE (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Power Supply Rejection Ratio	ΔVCC or ΔVEE, 100 mVpp, f = 5 MHz	45			dB
Channel Seperation	The four unselected channels are driven with Vin = 100mVpp, f = 5MHz	45			dB
Write Current Voltage	IWC = 45 mA	-2.7		-0.5	V
Total Head Input Current	IWC = 0			200	μA

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Current Gain (IH/IWC)	IWC = 45 mA, IH≙ Head Current	0.95		1.0	
Write Current Pin Voltage	IWC - 45 mA	-3.7		-1.5	V
Center Tap Head Voltage (VCT)	IWC = 45 mA	3.0		VCC -0.5	V
Differential Head Voltage Swing	3.0 ≤ VCT ≤ VCC -0.5V IWC = 45 mA, LH = 10 μH	5.7		7.7	V
Differential Data Voltage (DX – DY)		.175			V
Single Ended Data Input Voltage (DX, DY)		-0.9		0.1	V
Data Input Current	-0.9 ≤ VDX, VDY ≤ 0.1	-10		100	μA
Data Input Differential Resistance	f = 300 KHz	5			KΩ
Data Input Capacitance				10	pF
Unselected Diff. Head Current	IWC = 45 mA, LH = 10 μH, f = 2 MHz			2	mAp
Write Current Range		30		50	mA
Total Head Input Current	IWC = 0			500	μA

IDLE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Write Current Pin Voltage	IWC = 45 mA	VEE			V
Differential Head Current	IWC = 45 mA, LH = 10 μH, f = 2 MHz			2	mAp
Total Head Input Current	IWC = 0			500	μA

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Idle to Read/Write Transition Time				0.6	µs
Read/Write to Idle Transition Time				0.6	µs
Read to Write Transition Time	0 ≤ VLCS ≤ 0.8V (Circuit Enabled)			0.6	µA
Write to Read Transition Time	0 ≤ VLCS ≤ 0.8V (Circuit Enabled)			0.6	µs
Head Select Switching Delay Time				0.25	µs
Head Current Transition Time	(10% to 90% points) IWC = 45 mA, LH = 0H, RH = 0Ω			15	ns
Head Current Switching Delay Time ($TD_1 - TD_2$)	IWC = 45 mA, LH = 0H, RH = 0Ω, f = 5 MHz (See Figure 1)			19	ns
Head Current Switching Hysteresis TH = ($TD_1 - TD_2$)	IWC = 45 mA, LH = 0H, RH = 0Ω, f = 5 MHz, (VDx – VDy) Rise Time = 2ns (See Figure 1)			3	ns
Unsafe to Safe Delay After Write Data Begins (TD_3)	IWC = 30 mA, LH = 10 µH, f = 2 MHz (See Figure 2A)			1.0	µs
Safe to Unsafe Delay (TD_4)	LH = 10 µH, f = 2 MHz, IWC = 45 mA (See Figure 2B)	1.6		8.0	µs

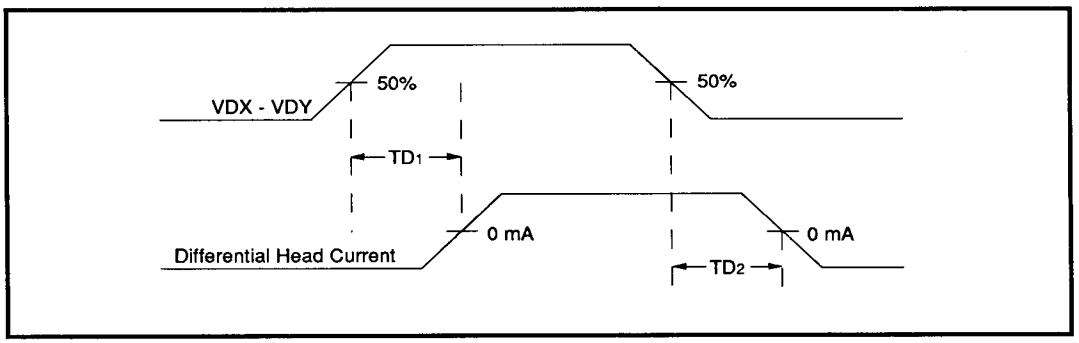


FIGURE 1: Head Current Timing

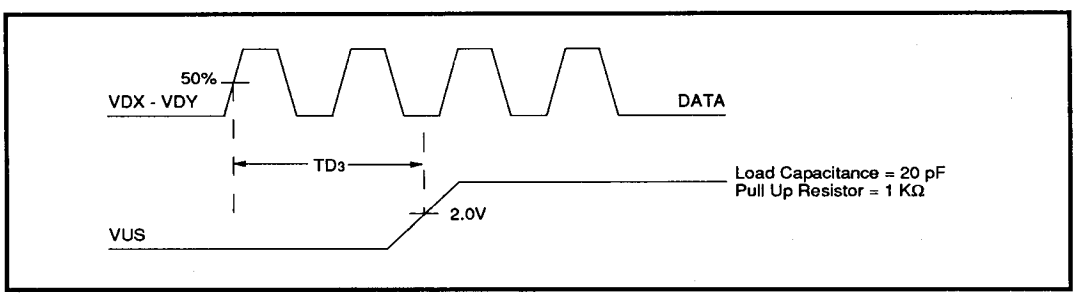


FIGURE 2A: Unsafe to Safe Timing

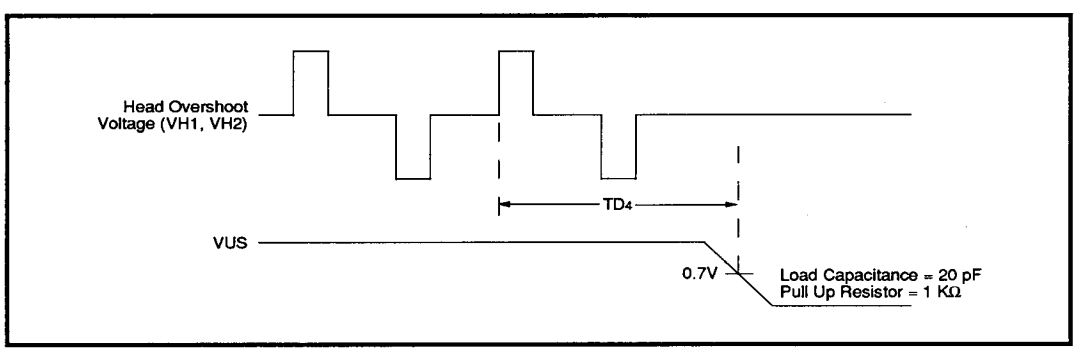


FIGURE 2B: Safe to Unsafe Timing

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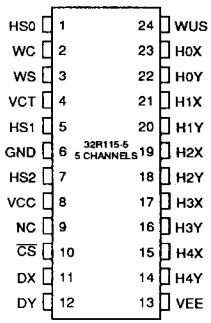
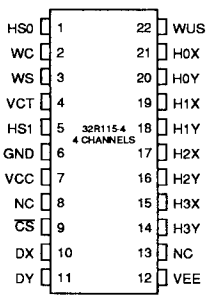
Read/Write Device

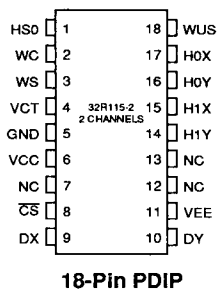
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



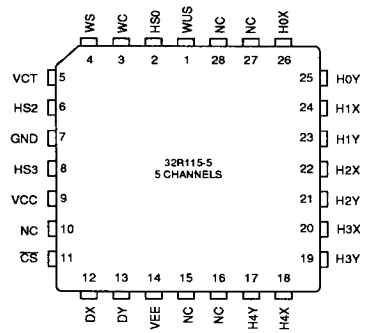
24-Pin PDIP, Flatpack, SOL



22-Pin PDIP



18-Pin PDIP



28-Pin PLCC

THERMAL CHARACTERISTICS: Øja

18-lead	PDIP	140°C/W	24-lead	PDIP	115°C/W
22-lead	PDIP	65°C/W	24-lead	Flatpack	70°C/W
28-lead	PLCC	65°C/W	24-lead	SOL	80°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32R115		
2-Channel PDIP	SSI 32R115-2P	SSI 32R115-2P
4-Channel PDIP	SSI 32R115-4CP	SSI 32R115-4CP
5-Channel PDIP	SSI 32R115-5P	SSI 32R115-5P
5-Channel SOL	SSI 32R115-5CL	SSI 32R115-5CL
5-Channel Flatpack	SSI 32R115-5F	SSI 32R115-5F
5-Channel PLCC	SSI 32R115-5CH	SSI 32R115-5CH