液晶之友 电话: 020-33819057 Http://www.lcdfriends.com No. Preliminary

DATE: 08 May 2002

REFERENCE SPECIFICATION

Description: 5.8" Wide Q-VGA TFT Color LCD Module

Customer's Parts Number

Model Number EDTCA39QRF

Notice: This Specification is "Preliminary". The contents described in this specification may be changed without notice. Please ask us to send final version and reconfirm before you start to design.						
AV-USE	LCD DIV	ISSUE				
AV-USE Marketing	g&Engineering Dept.					
Approval	Check					
Check						

Toshiba Matsushita Display Technology Co.,Ltd.

26-2 Yamada-Senden, Kawakita, Nomi-Gun, Ishikawa, 923-1296, Japan TEL:81-076-277-2113 FAX:076-277-2906

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ME OF SPECIFICATION: REFERENCE SPECIFICATION							SPEC.No.
DEL No.	EL No.: EDTCA39QRF						
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Record	of revision						
R/V No	Change of date	Contents	of R/V	Note	Approval	Check	Design
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NAM	E OF SPECIFICATION: RE	FERENCE SPECIFI	ICATIO	N	SPEC.No.
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MODEL No.: EDTCA3	39QRF Preliminary 3/21						
1. Application This specification is applied to the 5.8 inch wide , full colors and 400×RGB×234 dots color TFT Liquid Crystal Display Module. Controller circuit, inverter for lamp are not included in this module. Production Code(Part No) :EDTCA39QRF 2. General Specification							
CHARACTERISTIC ITEM	SPECIFICATION						
1.Display technology	a-Si TFT active-matrix						
2.Display mode	NW(normally white)						
3.Module outer dimension (note2-1) 144.5(W) \times 88.6(H) \times 7.2(D)							
4.Effective display area	$127.20 \times 71.838 \text{ mm}$						
5.Number of dots	400(W) × 3(RGB) × 234(H)						
6.Color-filter-array	RGB vertical stripes						
7.Weight	136 g ± 10 g						
8.Backlight	CCFL with 3 wave-length spectrum U Type						
9.Front surface treatment	AG coat (with WV film)						
10.Polarizer protective sheet	None						
11.Appearance	There are not remarkable defects.						
12.Metal frame condition	Not be connected to inner circuit						
note 2-1: Detailed dimensions are show	vn as per attached drawing.						
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3. Absolute Maximum Ratings

CHARACTERISTICS	SYMBOL	CONDITION	MIN.	MAX.	UNIT	REMARKS
Logic voltage	VDD	Ta=25	-0.3	6.5	v	
Source driver voltage	VEE	Ta=25	-0.3	6.5	v	
Logic signal voltage	VIN	Ta=25	-0.3	VDD+0.3	v	
Analog input voltage	VANA	Ta=25	-0.3	VEE+0.3	v	note 3-1
Gate driver positive voltage	VGON	Ta=25	-0.3	45	v	
Gate driver negative voltage	VSS	Ta=25	VGON-45	VGON+0.3		
Back light input voltage	VBL	Ta=25	-	3000	ACV	
Panel surface temp			-30	80		

note 3-1...Analog input voltages mean seven kinds of voltage such as VB, RED1, RED2, GREEN1, GREEN2, BLUE1, BLUE2.

Absolute maximum ratings are the limited value which must not be applied to the product even a second, and the product may have a permanent damage when it is exceeded. Accordingly, please pay attention to the surge of input voltage, fluctuation and/or ripple of supply voltage, ambient temperature and so on.

4.Environmental Conditions

ITEM	SPECIFICATION		REMARKS
Operating Temperature (Panel surface temp.)	-20 ~	70	note4-1,note4-2
Storage Temperature (Panel surface temp.)	-30 ~	80	note4-2

note 4-1...This value guarantees only operation, but doesn't guarantee all the contents of Electro-optical specification.

Electro-optical specification can be guaranteed at the condition that ambient temperature is $\mathbf{25}_{-}$.

note 4-2...Please refer to section 7. "Attention".



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5.Electro-optical Specification

CHARACTERISTICS	SYM	CO	CONDITION STANDARD VA				ALUE		measure	
CHARACTERISTICS	BOL			C.	MIN.	TYP.	MAX.	UNIT	method	
1.Brightness *note	В	0°	0°	\nearrow	240	300	-	cd/m ²	5-1	
2.Contrast Ratio	Cmax	best a	ngle		60	150	-	-	5-2	
3.White color	X	0°	0°		0.26	0.31	0.36	-	F 1	
chromaticity	Y	0°	0°	\nearrow	0.27	0.32	0.37	-	9-1	
4.Brightness uniformity	-	0°	0°	\nearrow	0.7	-	-	-	5-1	
5.Vertical viewing	u	-	0°	5	20	30	-	deg.		
Angle	D	-	0°	5	40	60	-	deg.	5.0	
6.Horizontal	L	0°	-	5	45	60	-	deg.	5-3	
Viewing Angle	R	0°	-	5	45	60	-	deg.		
7 Desmanae Time	r	0°	0°	\nearrow	-	11	22	ms	5.4	
	d	0°	0°	\nearrow	-	22	44	ms	5-4	

* note : Fluorescent lamp current is 2.0mA.(Measuring temperture : 25 ± 2)

Measuring condition:

Measuring surroundings	:	Dark room or its coordinate
Measuring temperature	:	25±5
Measuring humidity	:	40 ~ 70%RH
Adjust operating voltage to g	get op	ptimum contrast at the center of the display.
Use inverter	:	HIU-742A(16.5pF)

Main viewing angle direction (Contrast ratio becomes max.)





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5-2. Measuri	ng method for co	ontrast			
(1)Measu	ring instrument	• • 11 10)			
IUPCO	N BM-5A (meas	suring field = 1^{-1}			
(2)Measu	ring point				
Center o	of the display are	ea			
(3)Measu	ring method	- 0 - 0			
· Set the : view	ving angle in ver	= 0, – 0 tical axis			
: view	ving angle in hor	izontal axis			
0, 0) are the best an	gle to get the ma	ximum contrast	•	
• Measur	e maximum brig	htness "Y1"(Vlc=	=0v)and minimu	m brightness "	Y2"(Vlc=5v).
• The con Where, V	trast ratio U is a Ac means the eff	(1/YZ. fective voltage ar	unlied to liquid c	rystal in LCD pa	anel
		terre torrage ar	phone to inquire of	rystar in 202 r	inci.
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<u>6. Electrical Specification</u> (1)Contents			
Item	Contents		Remark
Screen size	15 cm (5.8 inch)wide		
Display mode	TN type full color(Transmitting type)	Norma	lly white
Driving method	a-Si TFT active-matrix line-at-a-time scan		
Pixel arrangement	RGB stripe arrangement		
Input video signal	RGB line-inverted	(Fig 6-2	l) P.15/21
Control voltage	CMOS level	(Fig 6-2	2) P.16/21
Backlight	Light-guiding plate with U type lamp	F	2.18,19/21

(2)Pixel arrangement and I/O interface pin assignment

	1	2	3	4		5	6 1198 1199 1200
1	R	G	В	R	G	В	R G B
2	R	G	В	R	G	В	R G B
3	R	G	В	R	G	В	R G B
					-		
233	R	G	В	R	G	В	R G B
234	R	G	В	R	G	В	R G B



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(3)Interface

Pin NO	SYMBOL	Function
1	CLK1	Source driver clock input 1
2	CLK2	Source driver clock input 2 (Set "H" at Simultaneous Mode)
3	CLK3	Source driver clock input 3 (Set "H" at Simultaneous Mode)
4	GND	Ground
5	STH1	Source scanning start signal 1
6	GND	Ground
7	MOD	Sampling mode change (H: Simultaneous, L: Sequential)
8	STH2	Source scanning start Signal 2
9	RL	Right / Left scanning change
10	RED2	Red video signal 2
11	GREEN2	Green video signal 2
12	BLUE2	Blue video signal 2
13	VB	Source output current adjustment
14	BLUE1	Blue video signal 1 、 connect to 12 pin
15	GREEN1	Green video signal 1, connect to 11 pin
16	RED1	Red video signal 1 、 connect to 10 pin
17	OEH	Source driver output enable
18	VDD	Power line for logic
19	Vcom	Voltage applied to color filter substrate
20	VEE	Power line for source driver IC
21	STV1	Gate scanning start signal 1
22	STV2	Gate scanning start signal 2
23	VGON	Gate driver positive voltage
24	OEV1	Gate driver output enable 1
25	OEV2	Gate driver output enable 2
26	OEV3	Gate driver output enable 3
27	U/D	Up/Down scanning change
28	CPV	Gate driver scanning clock pulse
29	VSS	Gate driver negative voltage
30	VSS	Gate driver negative voltage
	Connector : IL - 1	FPR Series (0.5mm pitch 30p) (JAE) gilded type
<i>v</i> .1	2	3 4 5 6

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NAME OF SPECIFICATION: REP		SPEC.No.							
MODEL No.:	EI		F			Preliminary			
	EDICA39QRF								
4)Electrical Specification Under TFT LCD Module op	perating con	dition							
ITEM	UNIT	REMAEKS							
IC logic voltage	VDD	2.70	3.0 ~ 3.3	3.60	V				
Source driver IC voltage	VEE	4.50	5.00	5.50	V				
Logic signal input voltage	VIL	0		0.20*VDD	V				
	VIH	0.80*VDD		VDD	V				
Black input voltage(+)	VSB+	(0.20)	0.75	(VSW+)	V	R,G,B, VEE=5V			
White input voltage(+)	VSW+	(VSB+)	4.25	(4.8)	V	R,G,B, VEE=5V			
Black input voltage(-)	VSB-	(VSW-)	4.25	(4.8)	V	R,G,B, VEE=5V			
White input voltage(-)	VSW-	(0.20)	0.75	(VSB-)	V	R,G,B, VEE=5V			
Source signal width	VSPP	-	3.50	VEE-0.4	V	R,G,B, note 6-4			
Source driver center voltage	VSC	2.30	2.50	2.70	V	R,G,B, VEE=5V			
Source output current adjustment	VB	2.30	2.50	2.60	V	VEE=5.0V VSPP=3.5V VCOM=7.0V			
Gate driver positive voltage	VGON	16.00	17.00	18.00	V				
Gate driver negative voltage	VSS	-14.00	-13.00	-12.00	V				
V center applied to color filter sub.	VCOM	0.70	1.70	2.70	V	note 6-2			
V amplitude applied to color filter sub.	VCPP	2.70	6.70	8.70	Vpp	note 6-1 & 6-4			
Logic supply current	IDD		1.60	3.20	mA	note 6-3			
Source driver IC supply current	IEE		21.20	42.40	mA	note 6-3 VB=2.5V			
Gate driver IC positive supply curren	IGH		0.08	1.00	mA	note 6-3			
Gate driver IC negative supply current	ISS		-0.01	-1.00	mA	note 6-3			

note 6-1...Brightness level is adjusted by varying this amplitude.

- note 6-2...Please adjust VCOM voltage between -1.5V and +2.5V to make the flicker level be minimum.
- note 6-3...Current value is an average level , not a peak level.

note 6-4...VSPP/2+VCPP/2<5.5(V) Please keep this condition for picture quality.

Attention) Electrical specification guarantees the normal operation of the product. In case of using the product over electrical specification, the normal operation is not guaranteed even within absolute maximum ratings.

The function of STV1 and STV2 is changed as follows by the U/D terminal (up/down scanning)

U/V	STV1	STV2
H(VDD)	Signal Input	Signal Output
L(0V)	Signal Output	Signal Input

The function of STH1 and STH2 is changed as follows by the RL terminal (Right/Left scanning)

RL	STH1	STH2
H(VD	Signal Input	Signal Output
L(0V)	Signal Output	Signal Input

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(6) Timing characteristics of input signals

CUADACTEDICTICS	CVMDOI	MINI	TVD	MAN	TINITT	DEMADIZO
CHARACTERISTICS	SIMBOL	IVIIIN	IYP	MAX	UNII	REMARKS
1 Field scanning period	tlV	-	262.5	-	H	
1 Line scanning period	tlH	-	63.5	-	μs	
Source driver operating frequency	fhc	1.0	8.25	9.0	MHz	full scan mode
Source arriver operating frequency	fhc			(13.0)	MHz	side panel area
Signal sampling pulse width	tchw	110	121.2	1000	ns	
Signal sampling pulse delay	tchd	36.4	40.4	44.4	ns	
Signal sampling pulse width(H)	tchwh	54.4	60.6	66.6	ns	tchd 12,23
Signal sampling pulse width(L)	tchwl	54.4	60.6	66.6	ns	
Source start signal pulse width	tshw	40	121.2	240*	ns	*shset=tshhld
Source start signal setup time	tshset	15	60.6	-	ns	
Source start signal hold time	tshhld	25	60.6	-	ns	
Source output enable pulse width	tohw	7.5	8.0	8.5	μs	
Source start signal rising time	tss	1.45	9.85	10.96	μs	
Video input signal start point	tvs	1.59	10.0	11.11	μs	
Phase difference between OEH & CPV	toc	1.5	2.3	-	μs	
Gate clock period	tvcvw	10	63.5	-	μs	
Gate clock pulse width (H)	tcvwh	5	10.3	58.5	μs	
Gate clock pulse width (L)	tsvwl	5	53.2	58.5	μs	
Gate start signal pulse width	tsvw	5	63.5	126**	μs	**tsvset=tsvhld
Gate start signal setup time	tsvset	2	31.75	-	μs	
Gate start signal hold time	tsvhld	2	31.75	-	μs	
Phase difference between OEH & STH	tosp	0	0.5	-	μs	
Phase difference between SYNC & OEH	tohs	-	1	1.9	μs	

note) •Rise time (tr) and fall time (tf) of source driver logic signal are both 6ns. •Rise time (tr) and fall time (tf) of gate driver logic signal are both 50ns.

N	Nise time (ii) and fan time (ii) of gate driver logic signal are both jons.							
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(8) Backlight						
CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT	REMARKS
Lamp current	IL	-	2.0	5.0	mArms	
Lamp voltage	VL	-	800	-	Vrms	
Lamp power consumption	PL	-	1.6	-	Wrms	
Possible lighting frequency	FL	-	30 ~ 80	-	kHz	
Starting Voltage	VS	-	-	2100	Vrms	Ta=-20
Life time	-	10000	-	-	Hour	

Attention)

- *1 Panel surface temperature should be kept less than contents of "3. Absolute Maximum Ratings".
- *2 Inverter should be designed to be subject to the conditions below:
 - Both the area and the peak under the positive and negative cycles of the waveform of the lamp current and lamp voltage should be symmetric. (The symmetric ratio should be larger than 90%)
 - (2) There should not be any spikes in the waveform.
 - (3) The waveform should be close to a sine wave whenever possible.
 - (4) Lamp current should not exceed the "MAX" value under the "Operating Temperature" (It is prohibited to exceed the "MAX" value even if it is operated in the non-guaranteed temperature). When lamp current exceed the maximum value for a long time, it may cause a smoking and ignition. Therefore, it is recommended that the inverter have the current limited circuit that is used as a protection circuit and/or the lamp current-controlled inverter.
 - (5) Please check the lamp current not to exceed the "MAX" value in the inverter open/short test.
 - (6) The "MIN" of "Lamp current " is the necessary value which must not be applied to the product for an stable working condition. Please pay attention to keep the "MIN" of "Lamp current" for a light dimmer.
- *3 The lamp frequency should be selected as different as possible from display horizontal synchronous signal (Including harmonic frequency of this scanning frequency) to avoid "Beat "interference which may be observed on the screen as horizontal stripes like moving wave.

This phenomenon is caused by interference between lamp (CCFL) lighting frequency and LCD horizontal synchronous signal.

*4 "Life time" is defined as a lamp maker's warranty value which applied to CCFL only. "Life time" is defined as the lamp brightness decrease to 50% original brightness at IL=MAX; continuous lighting, Ta=25 .



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*5 Value on cor (Hari The "] in the Howe that t It is c in you Espect in nor So, pl *6 Please lead v *7 "Start (1) Start (1) Start	es of "Lamp Volta; nditon of the LCD ison HIU-742A; 1 MAX" of "Starting e LCD module. ver this isn't the he module is inst areful that "Start ir set, inverter mo- cially, the value of rmal temperature ease check your s e do not bring the vire, so as to ensu- ting Voltage" and arting voltage se inverter : HIU transformer 	EDTCA39QRF ge", "Lamp power module drived h 6.5pF). g voltage "means values that we ca alled in your set. ing voltage" is ch ethod, value of ba f "Starting voltage condition, becau et in low temper high voltage with the safety and "Lamp voltage" -742A	r consumption by Matsushi the minimu an assure stan allast capac ge" is higher ature condit re into conta d decrease t are defined (2)	ion" and "Starting volta ita standard inverter um voltage to light norm tability of starting lamp in increase of stray capa- itor in your inverter and r in low temperature co- nce of CCFL is increase tion. act with metallic frame he difference of brightr I as follows. Lamp voltage *Use inverter : HIU-74 transformer load(LCD Module)	19/21 age" are defined mally o on condition acitance ad so on. ndition than d. and the GND ness.					
Lamp Conne	ctor	Use Connector	r : BHR - 03	3VS - 1(JST)						
Pin No.	SYMBOL	FUNC	CTION	REMARKS	S					
1	H	CCFL Power su	pply(High V	/oltage) cable color : I	Red					
2	NC	Non connect	1.70	-	71. • 4					
3	3 L CCFL power supply(Ground) cable color : White									
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<u>7. Attention</u> (1)Because th vibration, i	e liquid crystal di mpact and so on v	isplay panel is ma when installing.	de of glass, especi	ally pay attention	not to give it			
 (2)As for liquid crystal display panel ,the thickness of the liquid crystal layer is very thin with about 5 µ m, and the polarizer on the panel surface is easy to get damaged. So please pay attention to the following points. 1)Don't hold a panel surface strongly. In case that you held a panel surface in the construction process, after leaving for a while, then turn on. 2)In installation, pay attention not to give a stress and damage to the liquid crystal display panel 								
(3)Be careful not to leave long in the high temperature, the high humidity.								
(4)Cleaning Polarizer which covers a display part should be treated carefully because it is extremely delicate.								
Also, when cleaning a display surface, make the following solvent into the soft cloth like the gauze and so on sufficiently and wipe it lightly. · Isopropyl alcohol (recommend) · Ethyl alcohol								
Because it	bruises the surfa	ce of polarizer, ave	oid cleaning with t	the dried cloth.				
Avoid using the following solvents, because they causes the dissolving, the decoloring of the polarizer.								
[.] Ketones	(ex, Acetone)	·Aromatic compo	unds(ex. ; Xylene,	Toluene) • Wate	r			
(5)When inserting the flexible cable of the module to the input connecter, or pulling out it from the input connecter, always, turn off the power supply to input to the module.								
(6)Because CMOS-LSI is used for the circuit in the liquid crystal display panel, pay attention to the static electricity. (Especially, be careful of the interface flexible cable.)								
(7)Because LCD module does't have a protective circuit, please prepare the protective function such as fuses or shut -down circuit in user's power supply circuit.								
(8)Never use in the products which have opportunity to be dropped on hard floor such as concrete. It may be regarded as defectives.								
(9)Storage Co Don't leave In case of p equal to 70 Also, storag non conden	ondition LCD module una oreservation for lo %, and not expose ge condition of mo sing.	ttended for long t ng time, the stora e to direct sunligh re thac 60 shou	ime in high tempe age condition must t and fluorescent l ld be humidity of l	rature be humidity of les light. less than or equal t	to 45% and			
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 (10)Appearance defects shall be claimed at or before the customer's inspection. After the customer's inspection, we consider that the defects are caused in the customer's production process. Appearance defects include stains and scratches on the polarizer and fractures in the glass. (11) Revision of specification In case that changes in parts and materials used happen after formally signing the specification, its contents will be informed by prior written notice. Changes are implemented after confirmation of receipt. If new problems happen concerning to this specification , they should be solved by mutual discussion. (12) Warranty period Warranty period of this LCD module is 12 mouths after Manufacturing date code. (13)Caution 							
	<u>_!</u> \	CAUTI	ON OF TREATME	ENT			
CAUTION	 Please do not work during operating of CCFL by connecting inverter to avoid electric shock, because there is very high voltage on wiring between CCFL or EL and output terminal of switching inverter . Please do not harm cable and connectors action with care. Inverter output voltage should be stopped automatically and simultaneously when open-circuit or short-circuit happened between the inverter output and CCFL. (Please design the inverter which has shutdown function in case of no load for inverter output.) Continuos voltage output from the inverter under the open or short circuit may cause excessive leak current and overheat. 						
	 However inverter output voltage is required to remain for on-condition at least 3 seconds, because CCFL needs 1 or 2 seconds as start-up time. ³ Please take care burrs to be injured at the edges LCD metal frame. We would like you to design carefully to de-touch cable with frame edge section. 						
	4 . Please be careful with work to avoid injury by the edjes of LCD panel. We would like you to pay attension to design for avoiding damage of LCD glass by wiring and surrounding components.						
	5 . To make sure safety, please install fuse or shutdown circuit as safety function at power supply section inside of customer products,because there is no protect circuit inside LCD module to coop with short circuited issue of power supply(and so on)in LCD module.						
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