USER'S GUIDE

Dual Subscriber Line Interface Circuit (SLIC) FXS Daughtercard BD-SLIC-1

April 2002

LSI LOGIC®

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Preface

This document is the primary reference and user's guide for the Dual Subscriber Line Interface Circuit (Dual-SLIC) daughtercard. This Dual-SLIC daughtercard provides two standard telephone interfaces which interoperate with the LSI Logic ZSP™ processor families. This daughtercard is designed to mate directly with the LSI Logic ZSP evaluation boards, both EB402 and EB403 series.

The Dual-SLIC daughtercard interfaces to the standard ZSP processor serial TDM interface and provides all the normal programmable telephony BORSCHT (Battery, Overvoltage, Ringing, Supervision, Coding, Hybrid, and Test) features. A programmable 5 REN ringing generator is provided directly on the daughtercard. The daughtercard is fully programmable to meet global telephony standards, allowing designs to be implemented worldwide for a variety short-loop (<2000ft) applications.

Audience

This document assumes that you are familiar with telephony subscriber line interface circuits and digital signal processing devices. The people who benefit from this book are:

- Engineers and managers who are evaluating the LSI Logic ZSP Digital Signal Processor (DSP) for possible use in a system.
- Engineers who are designing the LSI Logic ZSP DSP into a system.
- Engineers developing voice telephony subsystems.

Organization

This document has the following chapters and appendixes:

- Chapter 1, **Introduction**
- Chapter 2, **Installation**
- Chapter 3, **Programmer's Model**

Related Publications

- *LSI402ZX Digital Signal Processor User's Guide*, LSI Logic Corporation
- *EB402 User's Guide*, LSI Logic Corporation
- *ProSLIC Si3210 Data Sheet*, Silicon Laboratories

Conventions Used in This Manual

The first time a word or phrase is defined in this manual, it is *italicized.*

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive. Signals that are active LOW end in an "n."

Hexadecimal numbers are indicated by the prefix "0x" —for example, 0x32CF. Binary numbers are indicated by the prefix "0b" —for example, 0b0011.0010.1100.1111.

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Chapter 1
Introduction

This user's guide describes all the steps necessary to interface the Dual-SLIC daughtercard (BD-SLIC-1) to the LSI Logic ZSP evaluation boards (either EB402 or EB403). The daughtercard provides two (2) separate voice interfaces thereby allowing connection to two subscriber telephony equipment (plain telephone, fax or modem).

The SLIC daughtercard plugs into one of the two SPORT connectors on the EB402 or EB403 evaluation board. The configuration of the serial port is described in Chapter 3, "Programmer's Model."

This users guide describes all hardware details for installation and operation of the SLIC daughtercard.

Section 3.2, "TDM Interface Timing," page 3-6, covers the programming aspects of the serial ZSP TDM interface port to allow proper interfacing and programming to the SLIC daughtercard.

1.1 Product Features

The Dual-SLIC daughtercard (BD-SLIC-1) provides the following features:

- Two completely separate subscriber line interface circuits.
- Board stackable (total two Dual-SLIC cards) for a total of four subscriber interface capability.
- Direct interface to LSI Logic EB402/EB403 evaluation card serial TDM interface connectors.
- Fully programmable from LSI Logic ZSP processor via in-band TDM time slots used for control/monitor functions (reference driver code available).

- DC power supplied directly from evaluation board supply (9 VDC).
- Performs all battery, overvoltage, ringing, supervision, coding, hybrid, and test (BORSCHT) functions.
- Battery voltage generated dynamically with on-chip DC-to-DC converter controller.
- 5 REN ringing generator with programmable waveshape, amplitude frequency, and cadence.
- Programmable AC impedance.
- Programmable ring trip and loop closure detect thresholds.
- On-hook transmission, pulse metering, and polarity reversal.
- Programmable constant loop current feed (20–41 mA).

Chapter 2
Installation

The Dual-SLIC daughtercard may be installed onto either the LSI Logic ZSP EB402 or EB403 evaluation boards. This daughtercard provides two subscriber telephony ports (maximum of four ports if two cards stacked together) to aid in the development of telephony applications on the LSI Logic ZSP processors. This section describes the required software and hardware to configure and use the SLIC daughtercard interfaces.

2.1 Hardware Equipment Required

The following is the minimum recommended list of hardware required to evaluate and use the Dual-SLIC daughtercard.

- LSI Logic EB402 or EB403 ZSP evaluation board. (EB402 shown in Figure 2.2 on page 2-5.)
- Dual-SLIC daughtercard (BD-SLIC-1) (Shown in Figure 2.3 on page 2-7.)
- External telephones, fax, modem or telephony test equipment supporting 2-wire subscriber loop interface.

2.2 Software Requirements

The following is the minimum recommended list of development software and drivers to fully evaluate and use the Dual-SLIC daughtercard.

- LSI Logic SDK Tools version 3.1 or later.
- LSI Logic ZOpen™ Dual-SLIC Driver Peripheral Support Package (PSP).

2.3 Hardware Set-Up for the SLIC Daughtercard

The Dual-SLIC daughtercard may be used with either the LSI Logic EB402 or the EB403 ZSP evaluation boards. The daughtercard is installed onto either the SPORT0 or SPORT1 TDM interface connectors provided on the ZSP evaluation boards. The daughtercards can also be stacked together to provide additional telephony ports for each SPORT interface. The ZSP evaluation boards support a maximum of two (2) Dual-SLIC daughtercards simultaneously.

The Dual-SLIC daughtercard installation procedure is as follows:

1. Set jumper “JP1” for desired power supply in accordance with Table 2.1. This jumper selects the 9VDC power source to be supplied from the ZSP evaluation board (normal setting) or from an external source connected to connector J4. See Figure 2.1 for daughtercard component locations.

Table 2.1 Power Selection

9 VDC Location	Mother board	External Supply Connected to J4 J4-1 (+9 VDC) J4-2 (GND)
JP1	1–2 (Normal Setting)	2–3 (Test Only)

2. Keeping alignment of pin 1’s plug the FXS Interface board into one of the SPORT TDM interface connectors on the desired motherboard. See Figure 2.2 for location of SPORT0 and SPORT1 connectors.
3. Set SW1 to desired stacked board number in binary (0–7) in accordance with Table 2.2. The ZSP evaluation boards can support a total of two (2) daughtercards maximum. There must always be a board configured as card #0 and installed closest to the ZSP evaluation board.
4. Turn the ZSP evaluation board power on (Switch S3 on EB402).
5. Using the ZSP JTAG debugger connected to the evaluation board, load and run the ZOpen peripheral support SLIC driver software as per the instructions provided with the software package.

2.4 Firmware Installation

Example ZOpen SLIC driver firmware is available from LSI Logic. This example software demonstrates the features supported by the BD-SLIC-1 daughtercard. The firmware provides capability to detect a phone On/OFF hook status and also ability to Ring a telephone. It also provides the necessary APIs to enable access to all ProSLIC registers available on the daughtercard.

It is beyond the scope of this Dual-SLIC daughtercard user's guide to detail specific registers available on the ProSLIC device. Therefore, it is recommended that the user obtain both the Silicon Laboratories ProSLIC data sheet as well as the LSI Logic ZOpen SLIC driver support package.

The LSI Logic ZOpen SLIC driver support package executes on the ZSP 402zx DSP processor available on the EB402 evaluation board. This driver support package may also be easily ported to the ZSP403LP device available on the EB403 evaluation board.

Please reference the LSI Logic SLIC driver support package for detailed instructions on installing and executing the SLIC demonstration firmware on the EB402 platform. This driver support package supports the necessary APIs to control a maximum of two (2) Dual-SLIC daughtercards for a total of four (4) telephony 2-wire subscriber ports.

Figure 2.1 SLIC Daughtercard

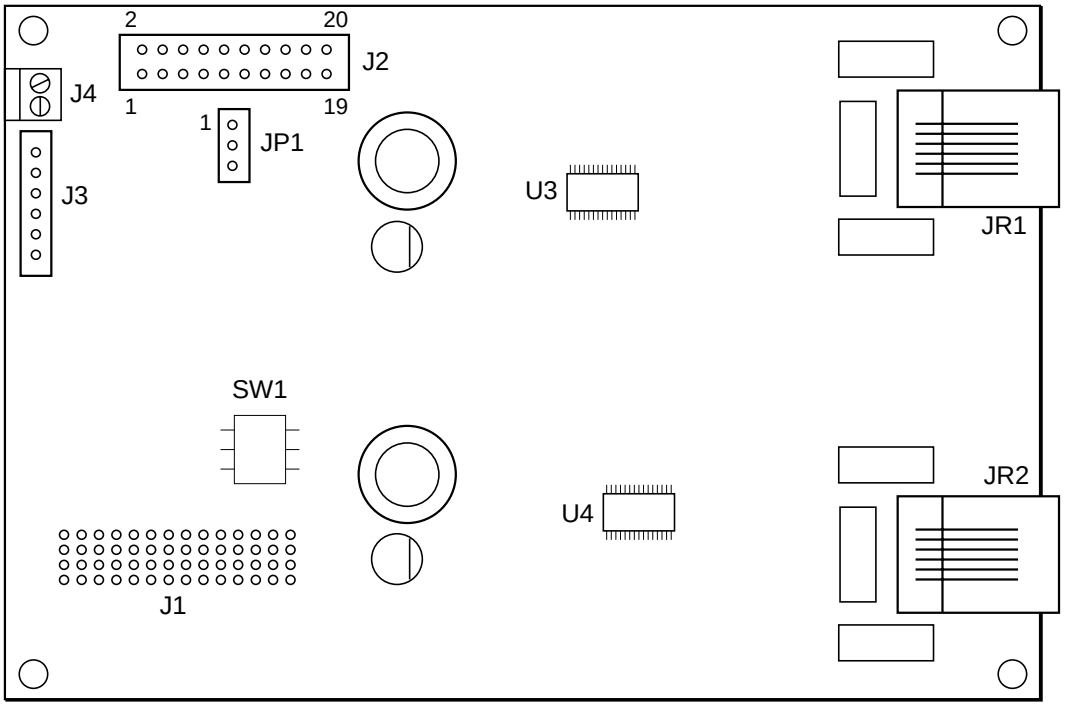
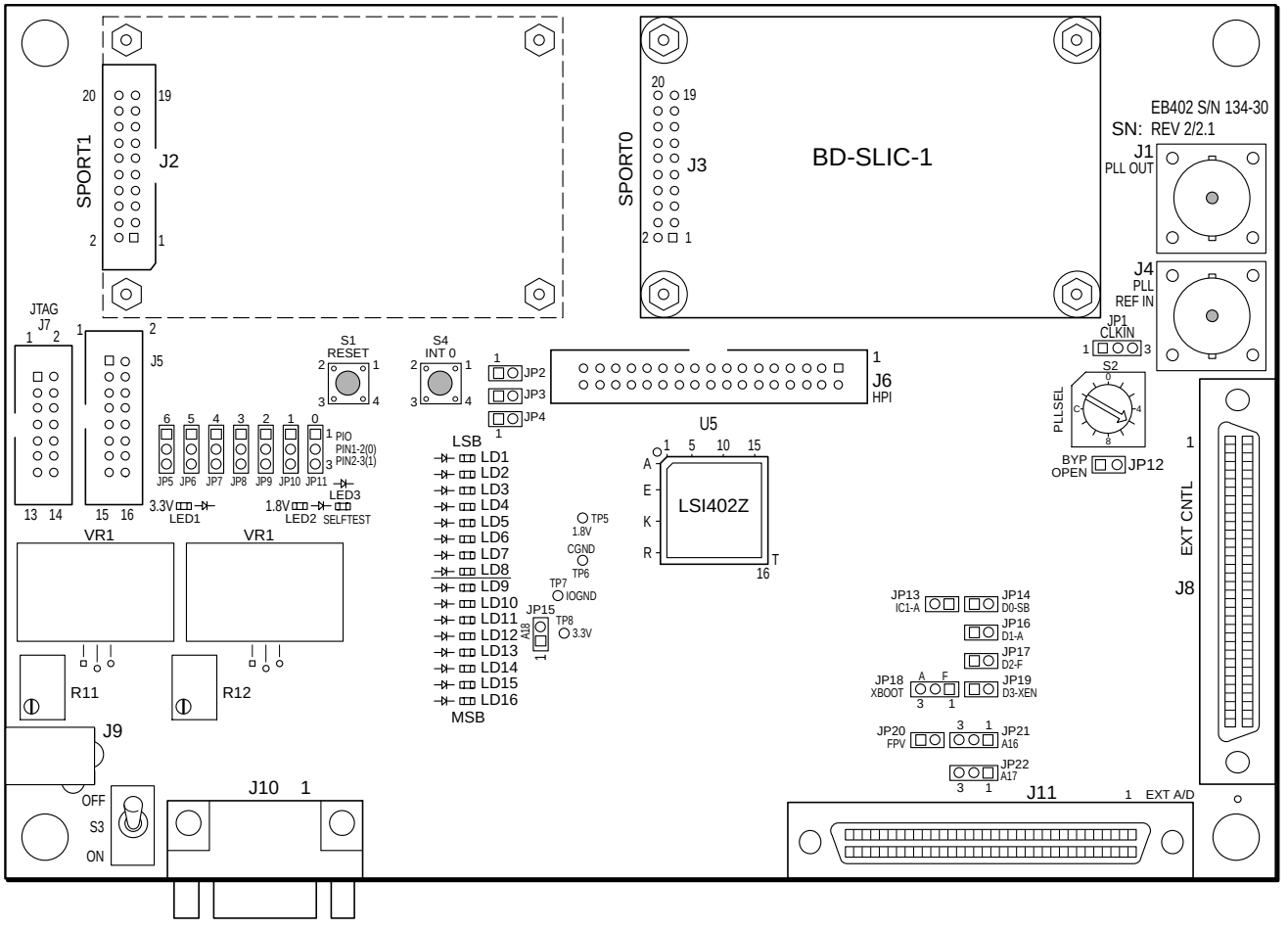


Figure 2.2 EB402 Development Board



2.5 Connection to External Equipment and Operation Overview

This section provides a general overview of a Dual-SLIC daughtercard used in a typical LSI Logic ZSP development system. This development platform provides a multi-channel telephony system for the ZSP processor families.

2.5.1 External Equipment Setup

The SLIC daughtercard is connected as shown in Figure 2.3. A total of two (2) Dual-SLIC daughtercards are supported on either the EB402 or EB403 evaluation boards. The daughtercard configuration can be either of the following:

- Single daughtercard installed on either SPORT0 or SPORT1 interface connectors, or
- One card installed on the evaluation board SPORT0 interface and the second on the SPORT1 interface, or
- Two cards stacked together on the same SPORT interface (either SPORT0 or SPORT1). Refer to Figure 2.4 for board stacking option. The daughercard switch SW1 selects the card number in the stackup (refer to Table 2.2). The bottom card must be configured as card #0, the top card configured as any other number besides card #0. This configuration can provide a total of four telephony interfaces for the ZSP evaluation board.

The external 9 VDC power supply shown in Figure 2.3 is not required and is used for factory testing purposes only.

Figure 2.3 SLIC Daughtercard Setup

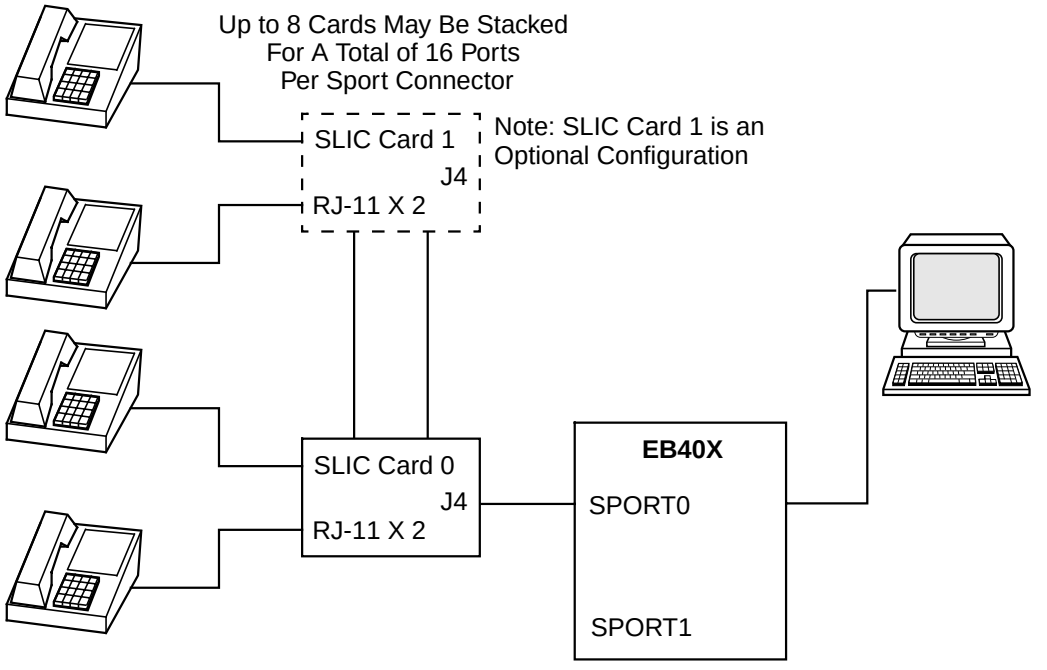
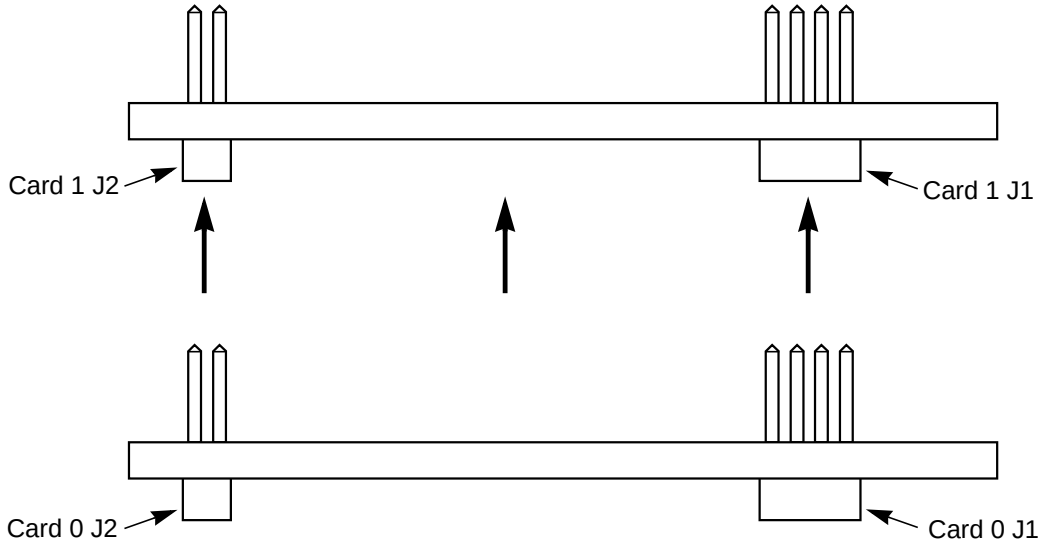


Figure 2.4 Board Stacking



2.5.2 Operation Overview

The Dual-SLIC daughtercard consists of two Silicon Laboratories SI3210 Proslic devices. These Proslic devices, along with their associated external components, provide the following functions; line voltage generation, ring voltage generation, onhook and offhook detection, and the 2-wire to 4-wire line hybrid.

The Dual-SLIC daughtercard connects directly to the LSI Logic ZSP serial TDM SPORT interface available on the ZSP evaluation boards. This serial TDM interface provides support for both the normal digital PCM data transmission as well as the ProSLIC register read/write access by the ZSP processor. Timeslots in the TDM stream are reserved for this specific ProSLIC monitor and control functions and are further described in Chapter 3, “Programmer’s Model.”

An 8.192 MHz clock on the daughtercard sources the clock for this TDM interface between the daughtercard and ZSP processor. This clock frequency configures the TDM interface for a total of 128 available TDM timeslots. Four of these timeslots are used for the normal transfer of PCM data between the daughtercard telephony ports and the ZSP processor. These PCM timeslots are normally configured to begin at timeslots 0–3, however these may be reprogrammed to different timeslots via the ProSLIC configuration registers.

Timeslots 53–61 are reserved and dedicated for the ZSP processor read/write access to the ProSLIC registers (refer to Chapter 3, “Programmer’s Model.”) A “Complex Programmable Logic Device” (CPLD) on the daughtercard converts these dedicated control TDM timeslots into the necessary ProSLIC SPI interface standard. The CPLD translates these ProSLIC register access’ between this serial SPI control interface and the serial TDM interface.

The Dual-SLIC daughtercard supports stacking of up to 2 cards on an individual SPORT Connector. Each card in the stack-up must be set with a unique card address set by SW1 on the daughtercard. The first card in the stack-up must always be configured as card #0 address. Table 2.2 provides the SW1 switch configuration settings to allow board stacking.

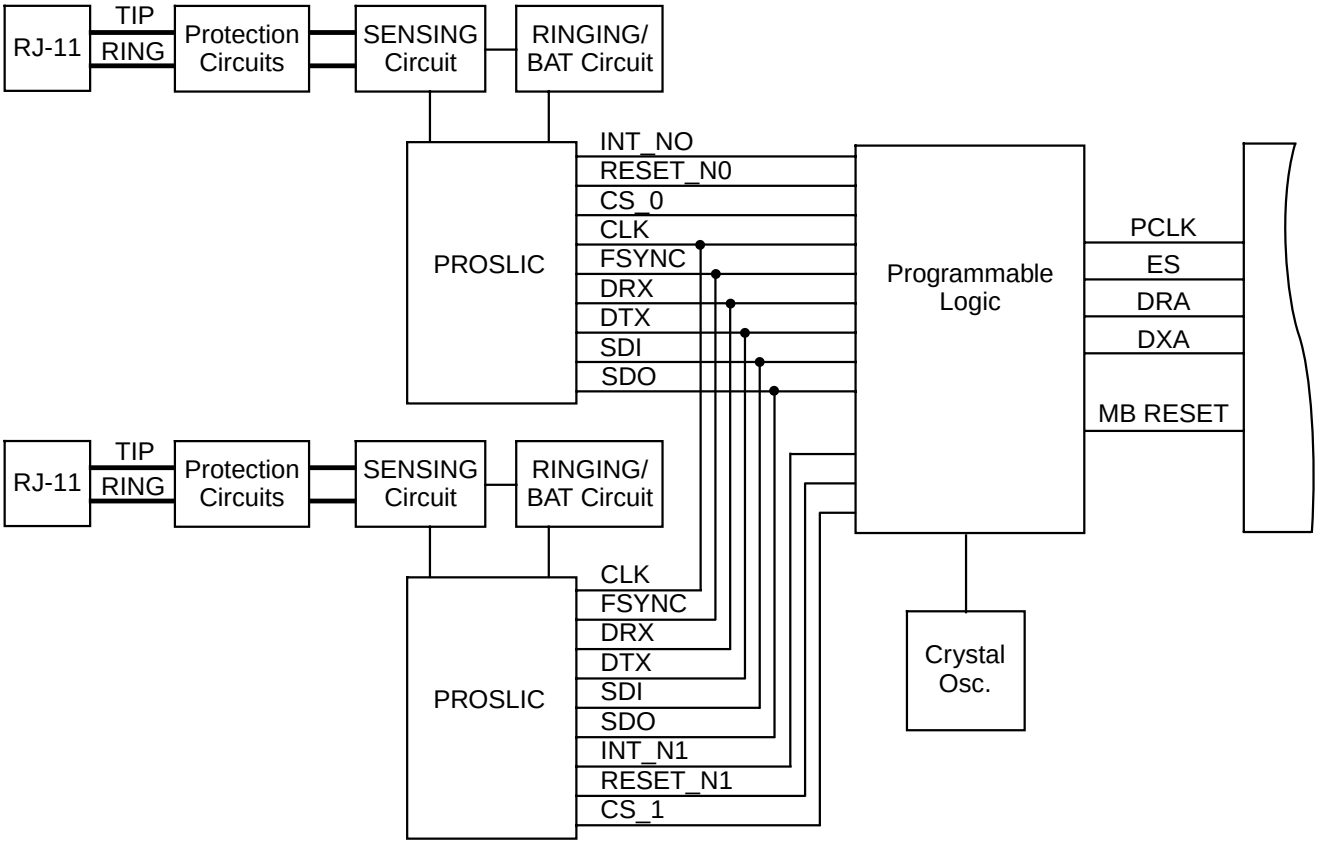
Table 2.2 Switch SWI Settings

SW1 (Pos3, Pos2, Pos1)	Board Number	Note
On, On, On	0	First board in Stack (Closest to EB403 board).
On, On, Off	1	Highest number possible on the EB402 evaluation board.
On, Off, On	2	Currently Not Supported
On, Off, Off	3	Currently Not Supported
Off, On, On	4	Currently Not Supported
Off, On, Off	5	Currently Not Supported
Off, Off, On	6	Currently Not Supported
Off, Off, Off	7	Currently Not Supported

2.5.3 Block Diagram

Figure 2.5 provides a block diagram overview of the Dual-SLIC daughtercard. As is shown, the two major components of the daughtercard consist of the Silicon Laboratories ProSLIC devices (with external components) and a CPLD device. A brief description of the daughtercard circuitry is provided below.

Figure 2.5 Dual-SLIC Block Diagram



The external 2-wire subscriber telephony equipment is connected to either or both of the standard RJ-11 connectors on the daughtercard. Line protection circuitry is provided to protect against excessive line voltages in support of normal short subscriber loop applications (less than 4Kft line).

The ProSLIC device contains the 2-to-4 wire hybrid circuitry to convert the external 2-wire subscriber signals into a 4-wire serial TDM digital interface. Each ProSLIC on the daughtercard provides fully programmable combination SLIC and Codec devices with integrated line battery feed and ringing voltage generation. The ProSLIC control/monitor features are provided over a standard serial SPI control interface. The digital PCM data is provided over a standard TDM serial interface. The CPLD device converts both these ProSLIC interfaces into a compatible TDM SPORT interface which interconnects to the LSI Logic ZSP evaluation boards SPORT interfaces.

The ProSLIC contains internal DC-to-DC converters to generate both the telecom battery voltage feed as well as the high voltage ring generator. These voltages are all derived from the 9 VDC supply provided directly from the LSI Logic ZSP evaluation boards. No external DC supplies are necessary besides the normal evaluation board supply. The ring generator supply supports capability for 5 Ringer Equivalency Number (REN) at a loop length of 2kft. The ringer may also support 3 REN at a reduced loop length of 4kft (maximum loop length supported).

The ProSLIC provides both On/Off hook loop current detection as well as ring trip detection. This status is available to the ZSP processor via the internal ProSLIC status register access.

The CPLD device translates the ProSLIC data and control interfaces to the LSI Logic ZSP compatible TDM SPORT interface. The CPLD provides the master TDM clock source which is derived from an on-board 8.192 MHz oscillator. The available 128 TDM timeslots are divided between PCM data and ProSLIC control timeslots. The PCM data timeslots are normally the first four timeslots in the TDM frame period, however these may be re-programmed via ProSLIC registers to reside in any of the 128 available timeslots. The ProSLIC control timeslots are fixed and dedicated at timeslot locations 53 through 63. The CPLD translates these TDM timeslots to/from the required serial SPI control format on the ProSLIC control interface.

The CPLD located on card address #0 in the daughtercard stack-up also provides timing to all other slave card addresses in this stackup. This provides a synchronous TDM serial bus between the ZSP processor on the evaluation board to all Dual-SLIC daughtercards attached to the evaluation board.

2.5.3.1 Power Requirements

All DC power on the Dual-SLIC daughtercard is derived directly from the 9 VDC and 3.3 VDC sources provided by the ZSP evaluation boards. These DC supply sources are provided on the TDM SPORT interface connectors. The Power requirements for the Dual-SLIC daughtercard are listed in Table 2.3.

Table 2.3 Power Requirements

Card Condition	Amps Drawn from 3.3 VDC	Amps Drawn from 9 VDC
Idle	0.2	0.1
One channel ringing other channel offhook	0.22	0.1
Both channels offhook	0.24	0.122

Chapter 3
Programmer's Model

This chapter describes the ProSLIC control and monitoring interface that is supported via the ZSP TDM SPORT interface. The user is recommended to review the Silicon Laboratories ProSLIC (P/N Si3210) data sheet for full description of register functions and values. This chapter merely describes the method for the ZSP process to access these available ProSLIC registers, not necessarily the detailed contents of each register.

LSI Logic also provides reference ZOpen reference driver firmware which provides the user with standardized APIs to initialize and control the ProSLIC for default operation.

3.1 Interface Timing Diagram

This section describes the serial TDM data and dedicated ProSLIC control timeslot interface definition.

3.1.1 TDM Data Stream Organization

All PCM data and ProSLIC monitor and control register access is provided over the standard 128 time-slot serial TDM interface. The CPLD located on the daughtercard multiplexes the TDM interface from the ZSP SPORT connector between this data and control ProSLIC ports.

The PCM data timeslots are programmable via ProSLIC registers, however these are normally initialized to reside in the first four (0-3) timeslots on the TDM interface.

Timeslots 53 through 63 are reserved and dedicated for the ProSLIC register read/write access by the ZSP processor on the evaluation board. The CPLD translates these specific control time-slots into the required

ProSLIC SPI interface. The following subsections detail these individual control TDM timeslot definitions.

3.1.1.1 TDM TX Control (ZSP to ProSLIC Direction)

This section describes the dedicated control timeslots for the TDM bus TX (write) direction of ZSP toward ProSLIC.

3.1.1.1.1 ProSLIC Command (TS53)

Table 3.1 details the contents of the TDM timeslot 53 byte used for the ProSLIC internal register access by the ZSP processor.

Table 3.1 Time Slot 53 PROSLIC COMAND BYTE

7	6	5	4	3	2	1	0
U	CA2	CA1	CA0	R/W	CS1	CS0	U

U **Unused** **7, 0**
Write as Zero.

CA **SLIC Card Address** **[6:4]**
Binary daughtercard address (0-7) to address boards in a stacked configuration.

CA2 = Card Address MSB
CA0 = Card Address LSB

R/W **Reg. Read/write bit** **3**
0 = Read data from PROSLIC

1= Write data to PROSLIC

CS1 **Chip Select control for PROSLIC Port 1** **2**
0 = ProSLIC Port 1 device not selected.

1 = ProSLIC Port 1 device selected.

CS0 **Chip-select control for PROSLIC Port 0** **1**
0 = ProSLIC Port 0 device not selected.

1 = ProSLIC Port 0 device selected.

3.1.1.1.2 ProSLIC Address Register (TS55)

Table 3.2 details the contents of the TDM timeslot 55 byte used for the ProSLIC internal register access by the ZSP processor.

Table 3.2 Time Slot 55 PROSLIC ADDRESS/REGISTER

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

This time-slot contains the ProSLIC address location for read/write access by the ZSP processor. The ProSLIC contains 108 direct addresses as detailed in the Silicon Laboratories Si3210 data sheet.

7 – ProSLIC Address MSB

0 – ProSLIC Address LSB

3.1.1.1.3 ProSLIC Data Register (TS57)

Table 3.3 details the contents of the TDM timeslot 57 byte used for the ProSLIC internal register access by the ZSP processor.

Table 3.3 Time Slot 57 PROSLIC DATA REGISTER

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

This time-slot contains the ProSLIC data value to be written to the ProSLIC address as indicated in time-slot 55 above. Refer to the Silicon Laboratories Si3210 data sheet for more specific information.

7 – ProSLIC Data MSB

0 – ProSLIC Data LSB

3.1.1.2 TDM RX Control (ProSLIC to ZSP Direction)

This section describes the dedicated control timeslots for the TDM bus RX (Read) direction of ProSLIC toward ZSP processor.

The CPLD loops back the contents of both timeslots 53 and 55 in the TX direction toward the RX direction. This register loop-back provides the necessary information to the ZSP processor to associate read data with a particular ProSLIC address location (i.e. the ProSLIC address location is returned in time-slot 55).

3.1.1.2.1 ProSLIC Command (TS53)

Table 3.4 details the contents of the TDM timeslot 53 byte used for the ProSLIC internal register access by the ZSP processor. This register returns the same value as was written in the TDM TX direction (i.e. direct data byte loop-back).

Table 3.4 Time Slot 53 PROSLIC COMAND BYTE

7	6	5	4	3	2	1	0
U	CA2	CA1	CA0	R/W	CS1	CS0	U

U — **Unused** — **7, 0**

CA — **SLIC Card Address** — **[6:4]**
Binary daughtercard address (0-7) to address boards in a stacked configuration.

CA2 = Card Address MSB
CA0 = Card Address LSB

R/W — **Reg. Read/write bit** — **3**
0 = Read data from PROSLIC
1= Write data to PROSLIC

CS1 — **Chip Select generation control for PROSLIC 1** — **2**
0 = ProSLIC port 1 device not selected.
1 = ProSLIC port 1 device selected.

CS0 — **Chip select generation control for PROSLIC 0** — **1**
0 = ProSLIC port 0 device not selected.
1 = ProSLIC port 0 device selected.

3.1.1.2.2 ProSLIC Address Register (TS55)

Table 3.5 details the contents of the TDM timeslot 55 byte used for the ProSLIC internal register access by the ZSP processor. This register returns the same value as was written in the TDM TX direction (i.e. direct data byte loop-back).

Table 3.5 Time Slot 55 PROSLIC ADDRESS REGISTER

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Returns the ProSLIC internal address location used for the present TDM frame transaction.

7 – ProSLIC Address MSB

0 – ProSLIC Address LSB

3.1.1.2.3 ProSLIC Read Data Register (TS61)

Table 3.6 details the contents of the TDM timeslot 61 byte used for the ProSLIC internal register access by the ZSP processor.

Table 3.6 Time Slot 61 READ DATA RESISTER

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Data read from the internal ProSLIC address as indicated by time-slot 55 above.

7 – ProSLIC Data MSB

0 – ProSLIC Data LSB

3.2 TDM Interface Timing

This section provides the timing details for the serial TDM interface between the Dual-SLIC daughtercard and ZSP evaluation board.

The PCM clock and Frame are generated by the Dual-SLIC daughtercard having a reference frequency of 8.192 MHz. As shown in Figure 3.1, this TDM clock frequency provides for a total of 128 TDM timeslots within a 8 KHz Frame period.

Figure 3.2 and Figure 3.3 provide detailed timing information for the TDM transmit and receive interfaces respectfully. These figures show the timing relationships between the TDM clock, frame, and data for each direction.

Figure 3.1 PCM Frame

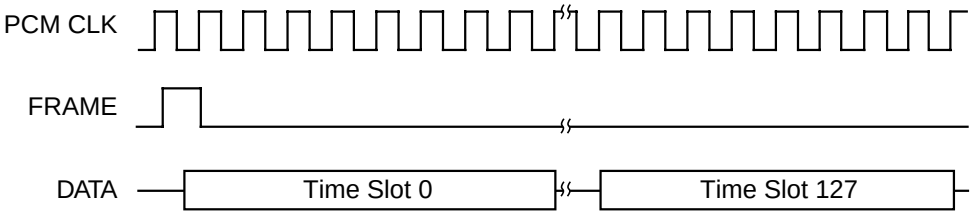


Figure 3.2 PCM Serial Port Transmit

Serial Port Transmit Timing for axfs = 0b10 (XFS/XFS/XCLK as Inputs

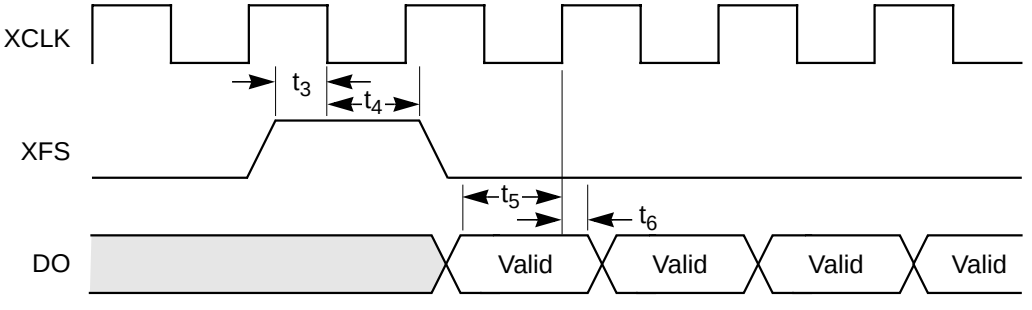


Figure 3.3 PCM Serial Portreceive

Serial Port Transmit Timing for axfs = 0b10 (XFS/XFS/XCLK as Inputs