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SEMICONDUCTOR
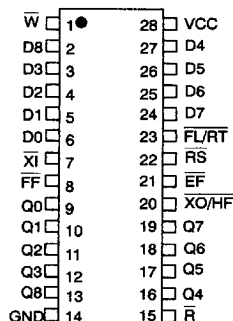
DS2013
8192 x 9 FIFO Chip

FEATURES

- First-in, first-out memory-based architecture

- Flexible 8192 x 9 organization

- Low-power HCMOS technology

- Asychronous and simultaneous read/write

- Bidirectional applications

- Fully expandable by word width or depth

- Empty and full warning flags

- Half-full flag capability in single-device mode

- Retransmit capability

- Available in 50 ns, 65 ns, 80 ns, and 120 ns access times

- Optional industrial temperature range -40°C to +85°C available designated N

PIN ASSIGNMENT

Pin		Pin	
$\overline{W}$	1	28	VCC
D8	2	27	D4
D3	3	26	D5
D2	4	25	D6
D1	5	24	D7
D0	6	23	$\overline{FL/RT}$
$\overline{XI}$	7	22	$\overline{RS}$
$\overline{FF}$	8	21	$\overline{EF}$
Q0	9	20	$\overline{XO/HF}$
Q1	10	19	Q7
Q2	11	18	Q6
Q3	12	17	Q5
Q8	13	16	Q4
GND	14	15	$\overline{R}$

28-Pin DIP (300 and 600 Mil)
See Mech. Drawings – Pgs. 964 & 966

PIN DESCRIPTION

$\overline{W}$	–	WRITE
$\overline{R}$	–	READ
$\overline{RS}$	–	RESET
$\overline{FL/RT}$	–	First Load/Retransmit
D^0_{-8}	–	Data In
Q^0_{-8}	–	Data Out
$\overline{XI}$	–	Expansion In
$\overline{XO/HF}$	–	Expansion Out/Half Full
$\overline{FF}$	–	Full Flag
$\overline{EF}$	–	Empty Flag
V_{CC}	–	5 Volts
GND	–	Ground
NC	–	No Connect

DESCRIPTION

The DS2013 8192 x 9 FIFO Chip implements a first-in, first-out algorithm, featuring asynchronous read/write operations, full, empty, and half-full flags, and unlimited expansion capability in both word size and depth. The DS2013 is functionally and electrically equivalent to the DS2009 512 x 9 FIFO with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to DS2009 512 x 9 FIFO Chip data sheet for detailed device description.

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