SONY CXB1532Q-Y

9, 8, Dual 4-bit Universal Shift Register T-46-09-05

Description

The CXB1532Q-Y is an ultra high speed monolithic Universal Shift Register with variable bit length.

Select inputs S1 and S2 select a function mode from parallel load, hold, shift right, and shift left. S3 and S4 select a bit length. The operation is shown in Function Table.

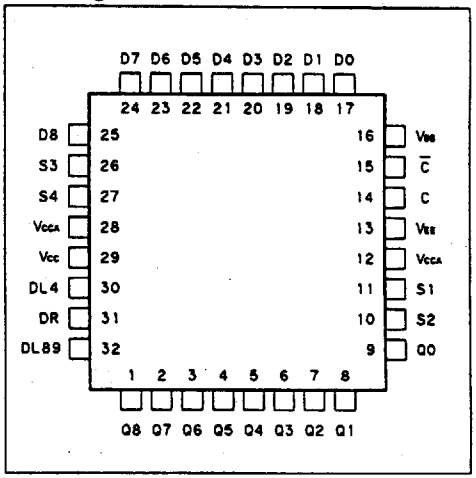
Features

- Typical clock rate up to 1.2GHz
- Variable bit length: 9-bit, 8-bit and 4-bit
- Internal pull down resistors on input pins to maintain logic LOW level the pins left open
- ECL 100K compatible I/O levels
- Differential clock input

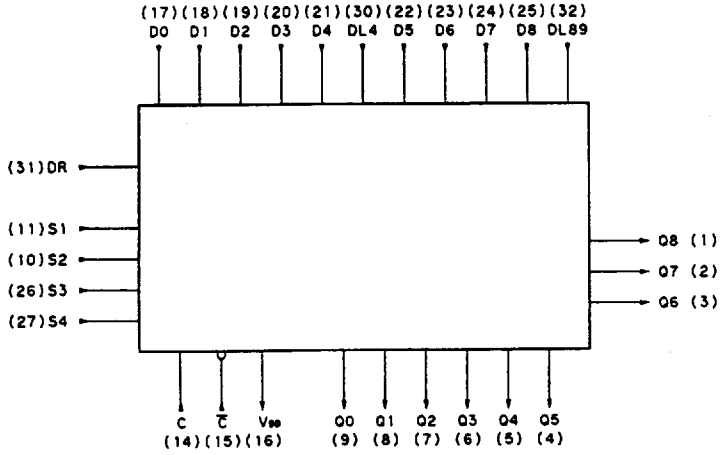
Pin Names

Dn	Data inputs
DR, DL4, DL89	Data inputs
Sn	Select inputs
C, $\overline{C}$	Clock inputs (positive edge trigger)
Qn	Data outputs
V_{BB}	Reference voltage output
Vcc	Circuit ground
V_{CCA}	Circuit ground for outputs
V_{EE}	Negative voltage supply

Pin Assignment



Logic Symbol



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CXB1532Q-Y

T-46-09-05

DC Characteristics

V_{EE} = −4.5±0.3V, V_{CC} = V_{CCA} = GND, V_{TT} = −2.0V, T_C = 0°C to +85°C

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}		−236	−173	−121	mA

AC Characteristics

V_{EE} = −4.5±0.3V, V_{CC} = V_{CCA} = GND, V_{TT} = −2.0V, T_C = 0°C to +85°C, R_T = 50Ω to V_{TT}

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	T_{PLH}	C	Qn		800	1120	1460	ps
	T_{PHL}				770	1080	1410	
Set up time	Ts	Dn, C			210			
		D_R, C	Q_0		190			
		D_{L4}, C	Q_4		220			
		D_{L89}, C	Q_7, Q_8		320			
		S_1, S_2→C	Qn		650			
Hold time	Th	C, Dn			220			
		C, D_R	Q_0		160			
		C, D_{L4}	Q_4		230			
		C, D_{L89}	Q_7, Q_8		10			
		C→S_1, S_2	Qn		−30			
Max. Clock frequency	f_{MAX}	C	Qn		0.8	1.2		GHz
Rise time	T_{TLH}			20% to 80%		480	650	ps
Fall time	T_{THL}					430	580	

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Function Table

Function \ Pin	Inputs								Outputs								
	DR	DL89	DL4	S1	S2	S3	S4	C	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
Load	×	×	×	L	L	×	×	⎍	D0	D1	D2	D3	D4	D5	D6	D7	D8
Shift left 9 bit length	×	DL89	×	L	H	L	L	⎍	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	DL89
Shift left 8 bit length	×	DL89	×	L	H	L	H	⎍	Q1	Q2	Q3	Q4	Q5	Q6	Q7	DL89	DL89
Shift left 4 bit length	×	DL89	DL4	L	H	H	×	⎍	Q1	Q2	Q3	DL4	Q5	Q6	Q7	DL89	DL89
Shift right 9 bit length	DR	×	×	H	L	L	L	⎍	DR	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Shift right 8 bit length	DR	×	×	H	L	L	H	⎍	DR	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Shift right 4 bit length	DR	×	×	H	L	H	×	⎍	DR	Q0	Q1	Q2	L	Q4	Q5	Q6	Q7
Hold	×	×	×	H	H	×	×	×	← No change →								

×: Don't care
⎍: Positive transition edge
H: HIGH voltage level
L: LOW voltage level

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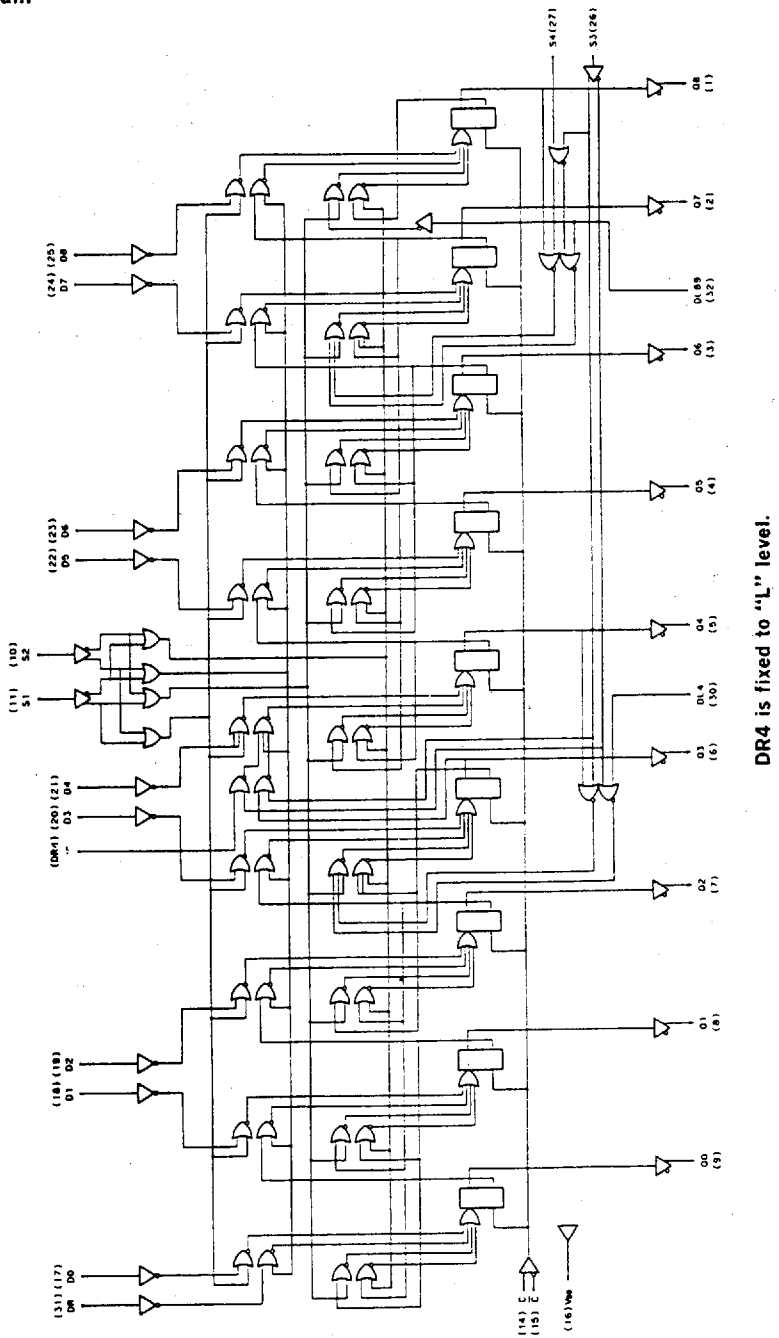
Block Diagram



DR4 is fixed to "L" level.

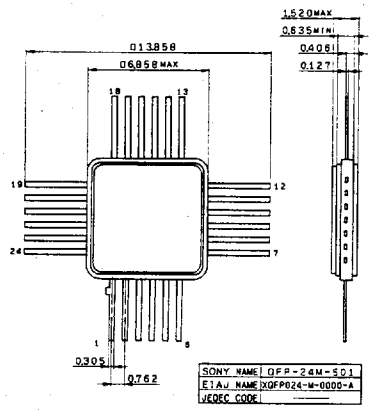
Package Data

T-90-20

Package Outline Uuit: mm

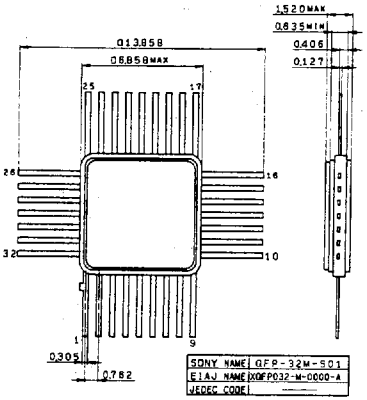
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



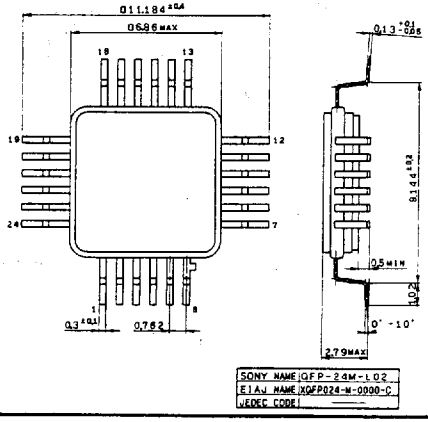
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



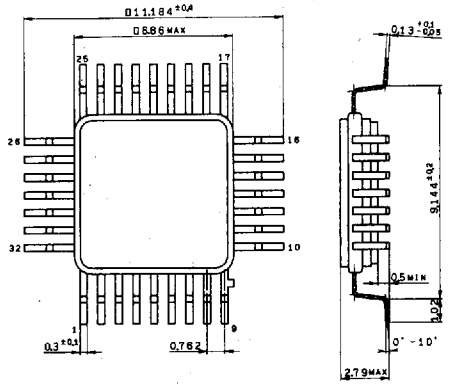
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

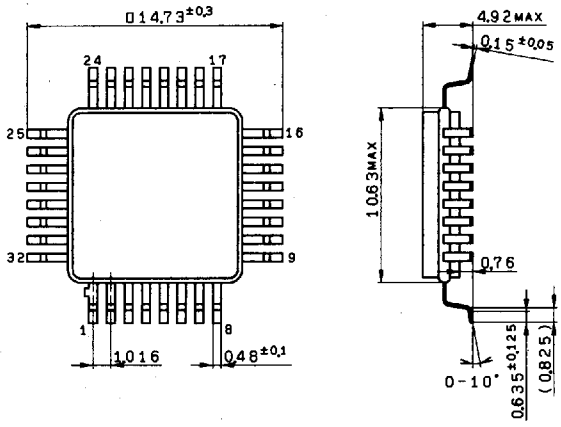
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

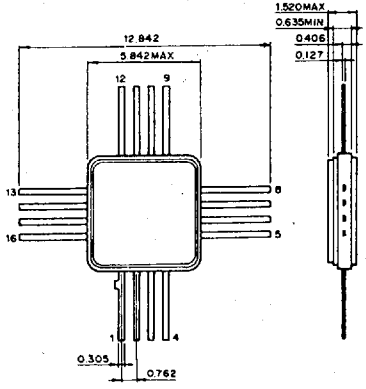
32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP



Package Data

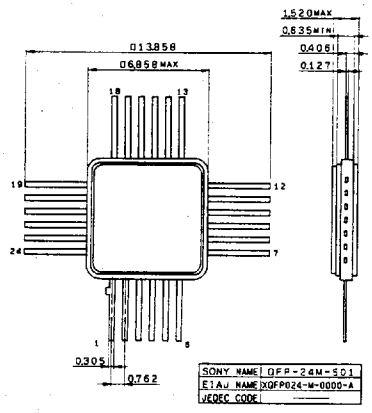
Package Data

T-90-20

Package Outline Uuit: mm

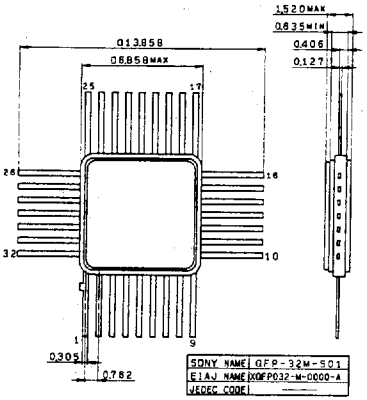
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



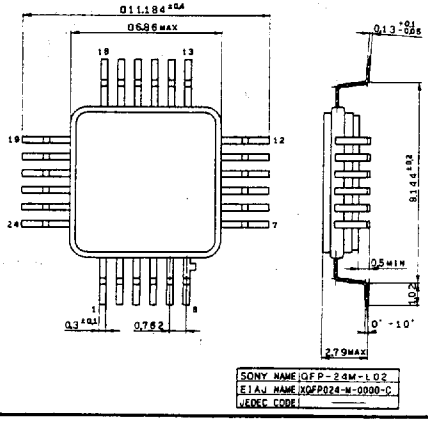
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



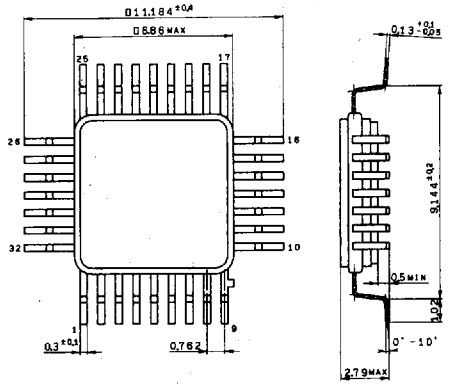
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

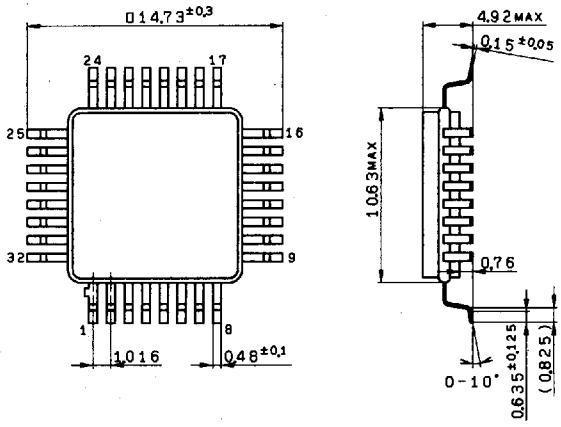
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP