ADC-5210 Series
Adjustment-Free
12-Bit A/D Converters

1

FEATURES

- **13 Microseconds maximum conversion time**
- **Totally adjustment-free**
- **Industry standard converter**
- **High-reliability versions available**
- **Low power consumption**

GENERAL DESCRIPTION

DATEL's ADC-5210 Series are high performance, hybrid, 12-bit successive approximation A/D converters. These devices combine high speed with extreme accuracy to provide the best possible performance in systems that require low power consumption, adjustment free operation, and miniature size.

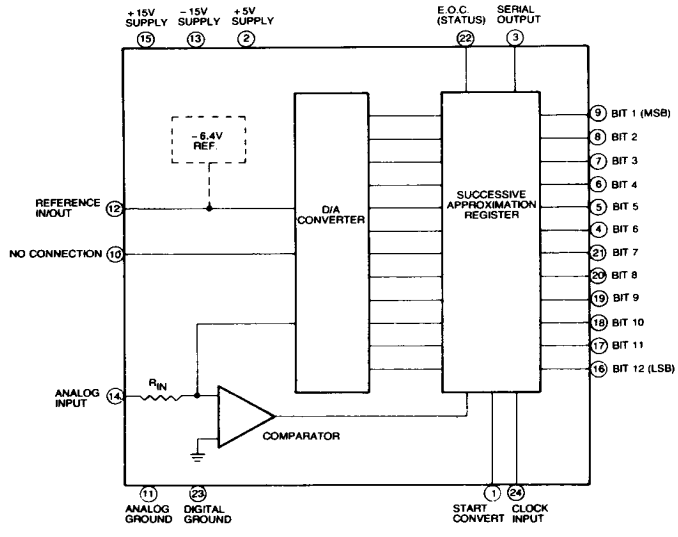
Active laser trimming of highly stable thin-film resistor networks eliminates the need for external adjustment circuits. Full-scale absolute accuracy error is ±0.05% FSR maximum at +25°C and only ±0.4% FSR maximum over the full military operating temperature range. Zero error is a maximum of only ±0.025% FSR. Conversion Time is 13 μseconds maximum, allowing full accuracy with a 1 MHz clock.

These devices are available in three factory set input ranges: 0 to +10V dc, ±5V dc, and ±10V dc. Models are available with an internal reference, or, for improved overall accuracy, requiring an external reference. Each model guarantees no missing codes over the full operating temperature range.

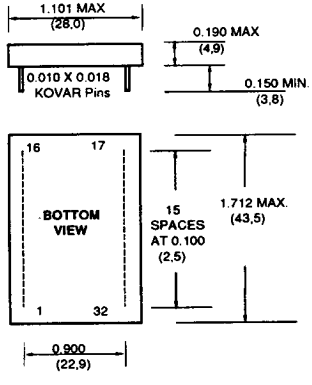
Other significant features include serial or parallel output data, 1W maximum power consumption, and a 10 ppm/°C Gain Tempco. Digital outputs are TTL-compatible and output coding is complementary binary for unipolar operation and complementary offset binary for bipolar operation.

Models are available specified over the full military operating temperature range of −55 to +125°C and commercial, 0°C to +70°, operating temperature ranges.

All models require ±15V dc and +5V dc for operation and are packaged in a 24-pin, hermetically sealed, ceramic package.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STAND OFF FROM CASE, ±0.01

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	START CONVERT	13	−15V SUPPLY
2	+5V SUPPLY	14	ANALOG INPUT
3	SERIAL OUTPUT	15	+15V SUPPLY
4	BIT 6 OUT	16	BIT 12 OUT (LSB)
5	BIT 5 OUT	17	BIT 11 OUT
6	BIT 4 OUT	18	BIT 10 OUT
7	BIT 3 OUT	19	BIT 9 OUT
8	BIT 2 OUT	20	BIT 8 OUT
9	BIT 1 OUT (MSB)	21	BIT 7 OUT
10	NO CONNECTION	22	E.O.C. (STATUS)
11	ANALOG GROUND	23	DIGITAL GROUND
12	REF. IN/OUT*	24	CLOCK INPUT

*THE ADC-5211, 5212, AND 5216 HAVE AN INTERNAL REFERENCE. THE ADC-5214 AND 5215 REQUIRE AN EXTERNAL REFERENCE.

ABSOLUTE MAXIMUM RATINGS	
Operating Temperature Range:	
ADC-521X	0°C to +70°C
ADC-521XH	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply, Pin 15	+18V
Negative Supply, Pin 13	−18V
Logic Supply, Pin 2	−0.5V to +7V
Analog Input, Pin 14	25V
Digital Inputs, Pins 1, 24	−0.5V to +5.5V
Digital Outputs	Logic Supply
Reference Input[1]	0 to −15V

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc supplies, V_{REF} = −10.000V, unless otherwise noted.

ANALOG INPUTS[2]	MODEL NUMBER[1]		MODEL NUMBER[1]	
Input Range (Input Impedance)				
−5V to +5V (5KΩ)	ADC-5211		ADC-5214	
−10V to +10V (10KΩ)	ADC-5212		ADC-5215	
0 to +10V (5 KΩ)	ADC-5216			
TRANSFER CHARACTERISTICS	**TYPICAL**	**MAXIMUM**	**TYPICAL**	**MAXIMUM**
Linearity Error: +25°C	±¼ LSB	±½ LSB	±¼ LSB	±½ LSB
0°C to +70°C	±¼ LSB	±½ LSB	±¼ LSB	±½ LSB
−55°C to +125°C	—	±¾ LSB	—	±¾ LSB
Differential Linearity Error	±½ LSB		±½ LSB	
No Missing Codes	Guaranteed over temperature			
Full-scale Absolute Accuracy Error[3]				
+25°C	±0.025% FSR	±0.05% FSR	±0.025% FSR	±0.05% FSR
0°C to +70°C	±0.1% FSR	±0.2% FSR	±0.05% FSR	±0.1% FSR
−55°C to +125°C	±0.1% FSR	±0.4% FSR	±0.05% FSR	±0.1% FSR
Zero Error: +25°C	±0.01% FSR	±0.025% FSR	±0.01% FSR	±0.025% FSR
0°C to +70°C	±0.025% FSR	±0.05% FSR	±0.025% FSR	±0.05% FSR
−55°C to +125°C	—	±0.05% FSR	—	±0.05% FSR
Zero Error: ADC-5216				
+25°C	—	±0.05% FSR	—	—
0°C to +70°C	—	±0.75% FSR	—	—
−55°C to +125°C	—	±0.75% FSR	—	—
Gain Error	±0.025%	—	±0.025%	—
Gain Drift	±10 ppm/°C	—	±3 ppm/°C	—
Conversion Time[5]	—	13 μsec.	—	13 μsec.
POWER SUPPLIES				
Power Supply Range: ±15V dc supplies	—	±3%	—	±3%
+5V dc supply	—	±5%	—	±5%
Power Supply Rejection[6]: +15V dc supply	±0.005% FSR/%V_S	±0.02% FSR/%V_S	±0.005% FSR/%V_S	±0.01% FSR/V_S
−15V dc supply	±0.01% FSR/%V_S	±0.05% FSR/%V_S	±0.005% FSR/%V_S	±0.01% FSR/V_S
Current Drain: +15V dc supply	+9 mA	28 mA	+9 mA	28 mA
−15V dc supply	−23 mA	−35 mA	−23 mA	−35 mA
+5V dc supply	+35 mA	68 mA	+35 mA	68 mA
±12V dc, +5V dc supplies[11]	—	—	—	—
−10V dc reference[1]	—	—	−1.5 mA	−2 mA
Power Consumption	695 mW	1 W	695 mW	800 mW

DIGITAL INPUTS (All Models)	MINIMUM	TYPICAL	MAXIMUM
Logic Levels: Logic "1"	2.0V	—	—
Logic "0"	—	—	0.8V
Clock Input:			
Pulse Width High	100 nanoseconds	—	—
Pulse Width Low	175 nanoseconds	—	—
Loading High (V_{IN} = 2.4V)	—	2 μA	20 μA
Loading Low (V_{IN} = 0.3V)	—	−0.25 mA	−0.4 mA
Frequency	—	—	1 MHz
Start Convert Input:			
Loading High (V_{IN} = 2.4V)	—	4 μA	40 μA
Loading Low (V_{IN} = 0.3V)	—	−0.25 mA	−0.4 mA
Set-up Time Start Low to Clock[8]	25 nanoseconds	—	—

DIGITAL OUTPUTS (All Models)			
Logic Coding[9]: Unipolar range Bipolar ranges	Complementary Straight Binary Complementary Offset Binary		
Logic Levels: Logic "1" Logic "0" Output Drive Capability, All Outputs[10]: Logic "1" Logic "0"	+2.4V — 8 TTL Loads 2 TTL Loads	+3.6V +0.15V — —	— +0.3V — —
REFERENCE INPUT/OUTPUT[1]			
Internal Reference: Voltage Accuracy Tempco of Drift Maximum External Current External Reference: Voltage Loading	— — — — — —	−6.4V ±2% ±5 ppm/°C — −10.000V —	— — — 100 μA −2 mA

FOOTNOTES:

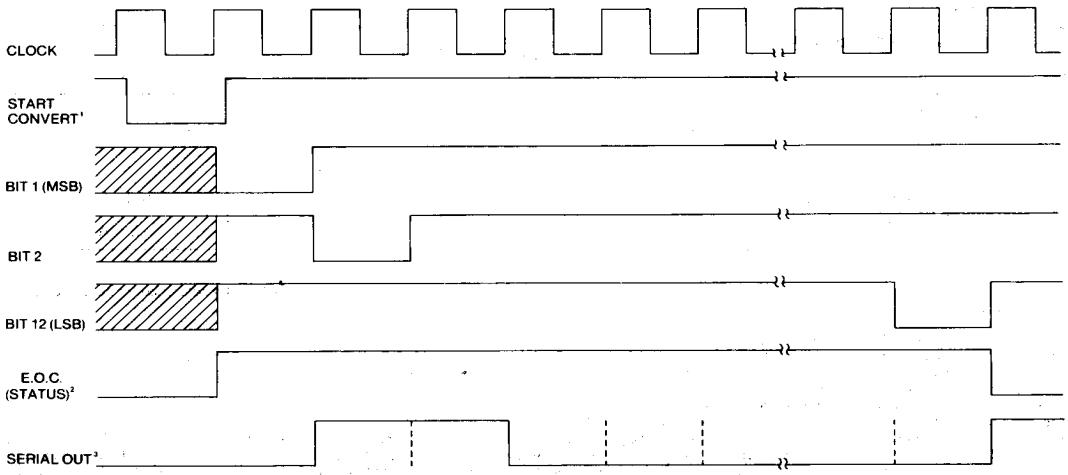
1. The ADC-5211, 5212, and 5216 include a −6.4V internal reference. The ADC-5214 and 5215 require an external −10.000V reference for specified operation.
2. Analog input ranges are internally set at the factory.
3. Absolute Accuracy Error includes offset, gain, linearity and all other errors. See Technical Notes for further information.
4. FSR stands for Full Scale Range and is equal to the peak voltage of the selected analog input range.
5. Conversion Time is defined as the width of the converter's STATUS (E.O.C.) pulse. The ADC-5210 Series will meet all specifications with clock frequencies up to 1 MHz. A 1 MHz clock gives a STATUS pulse that is 12 microseconds wide, however, unless careful timing precautions are taken, it will usually take 13 microseconds to update digital output data.
6. Power Supply rejection is guaranteed over the ±15V ±3% range.
7. The clock may be asymmetrical with minimum positive or negative pulse width.
8. In order to reset the converter, START CONVERT must be brought low at least 25 nanoseconds prior to a low-to-high clock transition. See Timing Diagram.
9. Serial and Parallel output data have the same coding. Serial data is NRZ successive decision pulses out, MSB first, at the clock frequency. Both serial and parallel output data become valid on the same rising clock edge. Serial data is valid on subsequent falling edges, and these edges can be used to clock serial data into receiving registers.
10. One TTL load is defined as sinking 40 μA with a logic 1 applied and sourcing 1.6 mA with a logic 0 applied.
11. For ±12V dc, +5V dc operation, contact the factory.

TECHNICAL NOTES

1. The use of proper layout and decoupling techniques are required to obtain rated performance. The ground pins (pins 11 & 23) are not connected internally, and therefore must be connected externally as directly as possible. They should be connected to the system analog ground, preferably through a large ground plane underneath the package. Power supplies should be bypassed to ground at the supply pins with 1 μF electrolytic capacitors in parallel with 0.01 F ceramic capacitors.
2. These converters can be made to continuously convert by tying the E.O.C. output (Pin 22) to the start convert input (Pin 1). When connected in this manner, the E.O.C. (START CONVERT) will go low at the end of conversion and the next rising edge of the clock will reset the converter and bring the E.O.C. (START CONVERT) high again. The MSB will be set on the next rising clock edge. The E.O.C. (status) will be low for approximately one clock period following each conversion.
3. The absolute accuracy error of an A/D converter is defined as the difference between the theoretical analog input voltage required to produce a given digital output and the unadjusted analog input voltage actually required to produce the same code. Because this error is measured and specified without adjustment, it includes all factors that may affect the devices accuracy at the point of measurement: offset error, linearity error, gain error, and noise error.
4. Because of propagation delays, the LSB of any given conversion may not be valid until a maximum of 30 nanoseconds after the E.O.C. (status) output has returned low. If the E.O.C. is used to strobe latches holding output data, adequate delays must be provided. Gate delays may be employed or the E.O.C. can be made the input of a D flip flop whose clock input is the same as the converter clock. Connected in this manner, the Q output will change one clock period after the E.O.C. changes. If the converter is connected in the continuous mode, the E.O.C. can be NORed with the converter clock to produce a positive strobe pulse ½ period wide, ½ period after the E.O.C. output has gone low. The rising edge of the pulse can be used to latch data after each conversion.
5. Applications of these converters that require the use of sample-hold may be satisfied by DATEL's SHM-4860, a high speed hybrid unit featuring a 200 nanosecond acquisition time and 0.01% accuracy.

TIMING & CONNECTION

TIMING DIAGRAM



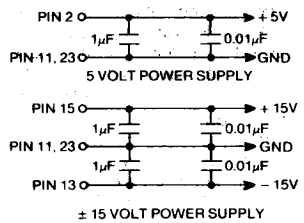
NOTES: 1. The converter is reset by holding the START CONVERT low during a low to high clock transition. The START CONVERT must be low for a minimum of 25 nanoseconds prior to the clock transition. After the START is set high, the conversion will begin on the next rising clock edge. The START CONVERT may be set low at any time during a conversion to reset and begin again.

2. At the end of conversion, the E.O.C. will remain low until the converter is reset. The parallel data is valid for the entire time the E.O.C. is low.
3. The serial output is non-return to zero.

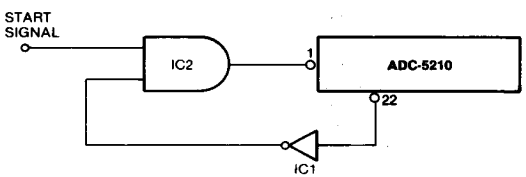
DIGITAL OUTPUT CODING

DIGITAL OUTPUT	ANALOG INPUT VOLTAGE		
	0 TO +10V ADC-5216	±5V ADC-5211, 5214	±10V ADC-5212, 5215
0000 0000 0000	+10.0000V	+5.0000V	+10.0000V
0000 0000 0001	+ 9.9976V	+4.9976V	+ 9.9951V
0111 1111 1111	+ 5.0024V	+0.0024V	+ 0.0049V
1000 0000 0000	+ 5.0000V	0.0000V	0.0000V
1111 1111 1110	+ 0.0024V	−4.9976V	− 9.9951V
1111 1111 1111	0.0000V	−5.0000V	−10.0000V

POWER SUPPLY DECOUPLING



TRIGGERING WITH A POSITIVE EDGE



The ADC-5210 Series A/D's may be made to start converting on a positive going edge by employing the circuit shown. The rising edge of the start signal will drive the output of IC2 low. The converter will reset on the next rising clock edge. When the converter resets, the status output (pin 22) goes high, the output of IC1 goes low; and since the start signal is still high, the output of IC2 goes high allowing the conversion to continue immediately. The start signal should be brought low before the conversion is complete.

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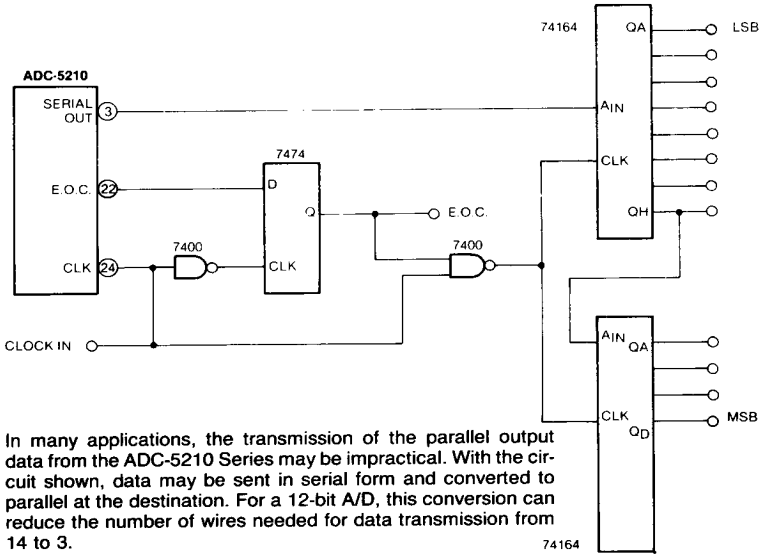
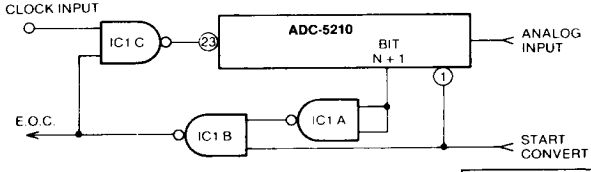
APPLICATIONS

SERIAL TO PARALLEL CONVERSION



In many applications, the transmission of the parallel output data from the ADC-5210 Series may be impractical. With the circuit shown, data may be sent in serial form and converted to parallel at the destination. For a 12-bit A/D, this conversion can reduce the number of wires needed for data transmission from 14 to 3.

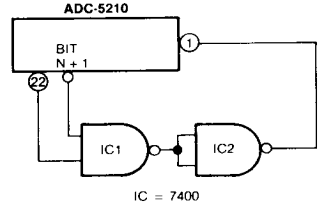
SHORT CYCLE OPERATION



IC1 SN7400N QUAD NAND GATE

If an application requires less than 12 bits resolution, the ADC-5210 Series may be truncated to the desired number of bits, with a proportionate decrease in conversion time, by using the circuit shown. With this circuit the start convert and E.O.C. signals function normally.

SHORT CYCLE — CONTINUOUS CONVERTING



To continuously convert at N bits, the circuit shown may be used. The output of bit (N + 1) acts like a status when one converts at N bits. The START CONVERT input is made the AND function of bit (N + 1) and the STATUS output to prevent the possibility of a lock up condition at power-on.

ORDERING INFORMATION

MODEL NO.	INPUT VOLT. RANGE	REFERENCE	OPERATING TEMP. RANGE
ADC-5211	±5V	Internal	0 to +70°C
ADC-5211H	±5V	Internal	−55 to +125°C
ADC-5212	±10V	Internal	0 to +70°C
ADC-5212H	±10V	Internal	−55 to +125°C
ADC-5214	±5V	External	0 to +70°C
ADC-5214H	±5V	External	−55 to +125°C
ADC-5215	±10V	External	0 to +70°C
ADC-5215H	±10V	External	−55 to +125°C
ADC-5216	0 to +10V	Internal	0 to +70°C
ADC-5216H	0 to +10V	Internal	−55 to +125°C

For military devices compliant to MIL-STD-883, consult the factory.