ADC-5101
Adjustment-Free
8-Bit A/D Converter

1

FEATURES

- **900 Nanoseconds maximum conversion time**
- **Adjustment-free operation**
- **Industry standard converter**
- **−55°C to +125°C Version**
- **Wide power supply range**

GENERAL DESCRIPTION

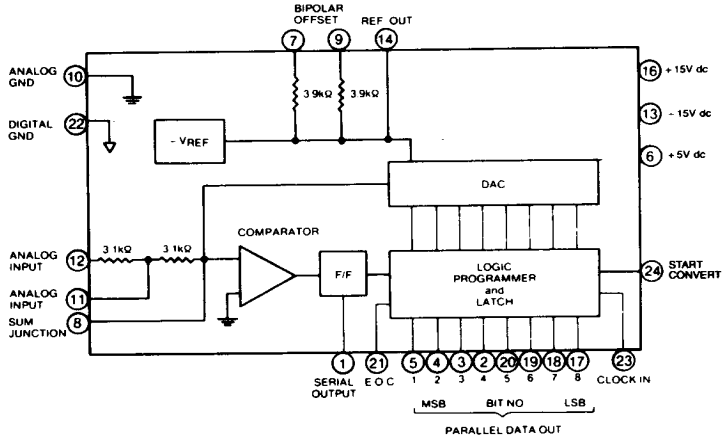
DATEL's ADC-5101 is a high-speed, adjustment-free, 8-bit analog-to-digital converter. Pin-compatible with industry-standard 5101 converters, these devices offer high speed and high accuracy with a full military temperature range version available.

Using the successive approximation method, the ADC-5101 achieves a conversion time of only 900 nanoseconds maximum, making it an ideal choice for high speed, multiplexed data acquisition systems. Active laser trimming of highly stable thin-film resistor networks eliminates the need for external gain or offset adjustments. Overall full-scale absolute accuracy is only ±½ LSB at +25°C and only ±2 LSB over the full military operating temperature range.

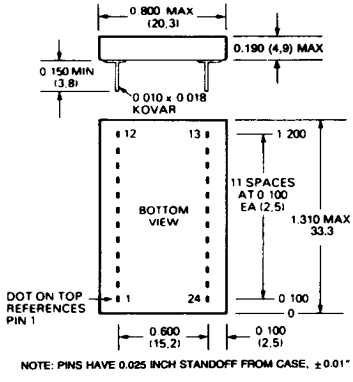
Output coding is straight binary for unipolar operation and offset binary for bipolar operations with both parallel and serial outputs brought out. Digital outputs are TTL-compatible and can drive 5 TTL loads. Nine analog input voltage ranges are programmable by external pin connection.

The ADC-5101H is specified for operation over the full military operating temperature range of −55°C to +125°C. Other models are specified for operation over the commercial 0°C to +70°C operating temperature.

All models require ±15V dc and +5V dc for operation and are packaged in a 24-pin, hermetically sealed ceramic package.



MECHANICAL DIMENSIONS
INCHES (MM)
24-PIN CERAMIC



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	SERIAL DATA OUT	13	− 15V POWER
2	BIT 4 OUT	14	REF. OUT
3	BIT 3 OUT	15	N/C
4	BIT 2 OUT	16	+ 15V POWER
5	BIT 1 OUT (MSB)	17	BIT 8 OUT (LSB)
6	+ 5V POWER	18	BIT 7 OUT
7	BIPOLAR OFF.	19	BIT 6 OUT
8	SUM JUNCTION	20	BIT 5 OUT
9	BIPOLAR OFF.	21	E.O.C. (STATUS)
10	ANALOG GND.	22	DIGITAL GND.
11	ANALOG INPUT	23	CLOCK INPUT
12	ANALOG INPUT	24	START CONVERT

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ABSOLUTE MAXIMUM RATINGS	
Analog Supply	±0.5V dc to ±17V dc
Logic Supply	−0.5V dc to +7V dc
Analog Input	±25V dc
Digital Inputs	−0.5V dc to +5.5V dc

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc and +5V dc supplies, unless otherwise noted.

INPUTS	
Analog Input Ranges, unipolar	0 to −5V dc, 0 to −10V dc, 0 to −20V dc
	0 to +5V dc, 0 to +10V dc, 0 to +20V dc
bipolar	±2.5V dc, ±5V dc, ±10V dc
Input Impedance, 5V range	1.5 kΩ
10V range	3.0 kΩ
20V range	6.0 kΩ
Input Logic Levels, Logic "1", min.	+2.0V
Logic "0", max.	+0.8V
Start Conversion	Negative going pulse with duration of 25 nsec. min. Loading:[2] 2 TTL loads
Clock Input, Pulse width high, min.	20 nsec.
Pulse width low, min.	46 nsec.

OUTPUTS	
Parallel Output Data	8 parallel lines of data held until next conversion command.
Output Logic Levels	
Logic "1", min.	+2.4V
Logic "0", max.	+0.4V
Fanout	5 TTL loads
Coding, unipolar	Straight binary
bipolar	Offset binary
Serial Output Data	NRZ successive decision pulses out, MSB first, at the clock frequency.
End of Conversion (E.O.C.)[4]	Conversion Status Signal. Output is high during reset and conversion, low when conversion is complete
Reference Output Voltage	−6.2V

PERFORMANCE	
Resolution	8 Bits
Conversion Time, max.	900 nsec. max.
Nonlinearity max.	±½ LSB
Differential Nonlinearity, max.	±½ LSB
Absolute Accuracy, max.[5]	±½ LSB
Absolute Accuracy vs. temperature	
0 to +70°C, max.	+1 LSB
−55 to +125°C, max.	±2 LSB
Reference Output Tempco	5 ppm/°C typ., 20 ppm/°C max.
Power Supply Rejection	
Positive Supply	±0.002% FSR[6]/% Supply
Negative Supply	±0.002% FSR/% Supply
Logic Supply	±0.01% FSR/% Supply
No Missing Codes	Over operating temperature range

POWER REQUIREMENTS	
Analog Supply, Pin 16	+10V dc to +16V dc at 35 mA max.
Pin 13	−10V dc to −16V dc at 35 mA max.
Logic Supply, Pin 6	+5V dc ±0.25V dc at 100 mA max.
Power Dissipation, max.	1.2W

PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range,	
ADC-5101	0°C to +70°C
ADC-5101H	−55°C to +125°C
Storage Temp. Range	−65°C to +150°C
Package Type	24 pin hermetically sealed ceramic

FOOTNOTES:

1. Converter will reset on the first edge of the clock after START CONVERT goes low and will convert the MSB on the next rising edge of the clock. If the START CONVERT is held low, the converter will be reset but will not convert the MSB until the first rising edge of clock after the START CONVERT returns high.
2. One TTL load is defined as 40 μA at logic "1" and −1.6 mA at Logic "0".
3. Clock input loading is 1 TTL load.
4. At the end of the conversion, the E.O.C. signal will remain low until the converter is reset. The parallel data is valid for the entire time the E.O.C. signal is low.
5. Absolute accuracy includes offset, gain, linearity, and all other errors. See Technical Note 3.
6. FSR is full-scale range.

TECHNICAL NOTES

1. The use of good high frequency circuit board layout techniques is required for optimum performance. The analog common (Pin 10) and digital common (Pin 22) are not connected internally and therefore should be connected externally as close to the package as possible. For best results, this common connection should be a large ground plane running under the device package.
2. Both analog and digital supplies should be bypassed to ground with 1.0 μF electrolytic capacitors in parallel with 0.1 μF disc ceramic capacitors. Bypass capacitors should be located directly adjacent to, or on, each supply pin.
3. The absolute accuracy error of an A/D converter is defined as the difference between the theoretical analog input voltage required to produce a given digital output and the unadjusted analog input voltage actually required to produce that same code. Because this error is measured and specified without adjustment, it includes all factors that may effect the devices accuracy at the point of measurement: offset error, linearity error, gain error, and noise error.
4. The ADC-5101 should be driven from low impedance sources capable of high frequency current variations. DATEL's AM-452, a wide bandwidth, fast settling, monolithic operational amplifier is recommended for use as a driving amplifier.

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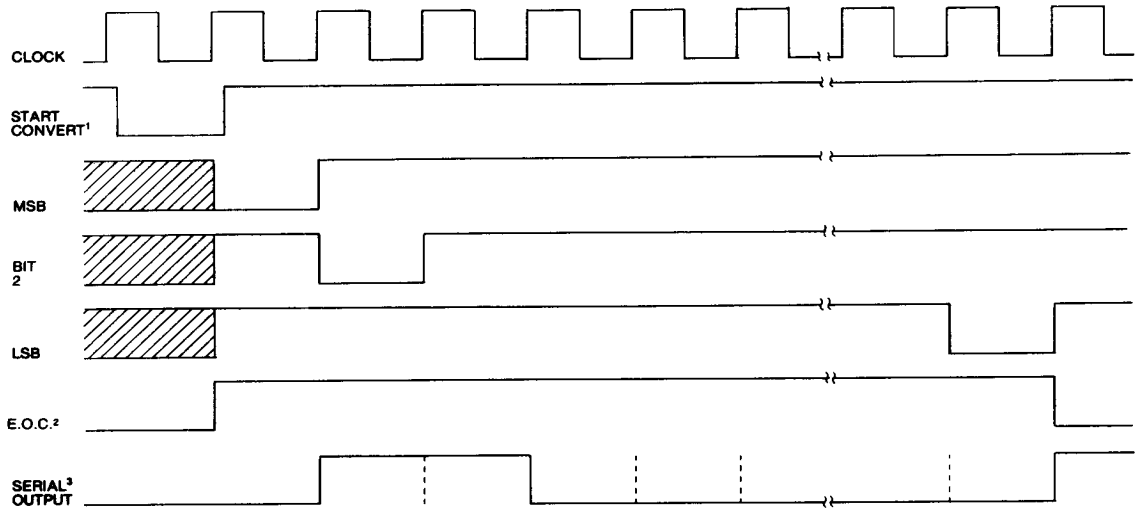
TIMING DIAGRAM



FOOTNOTES:

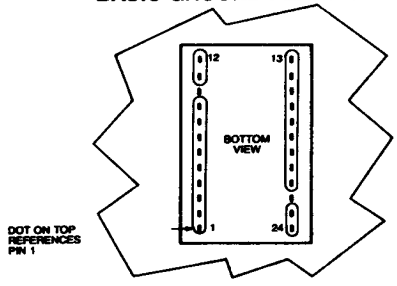
1. The converter is reset by holding the START CONVERT low during a low to high clock transition. The START CONVERT must be low for a minimum of 25 nanoseconds prior to the clock transition. After the START is set high, the conversion will begin on the next rising clock edge. The START CONVERT may be set low at any time during a conversion to reset and begin again.
2. At the end of the conversion, the E.O.C. will remain low until the converter is reset. The parallel data is valid for the entire time the E.O.C. is low.
3. The serial output is non-return to zero.

OUTPUT CODING AND RANGE SELECTION

DIGITAL OUTPUT	ANALOG INPUT—UNIPOLAR RANGES					
	0 TO −5V	0 TO −10V	0 TO −20V	0 TO +5V	0 TO +10V	0 TO +20V
0000 0000	0.000V	0.000V	0.000V	+4.981V	+9.961V	+19.922V
0000 0001	−0.019V	−0.039V	−0.078V	+4.961V	+9.922V	+19.844V
0111 1111	−2.481V	−4.961V	−9.922V	+2.500V	+5.000V	+10.000V
1000 0000	−2.500V	−5.000V	−10.000V	+2.481V	+4.961V	+9.922V
1111 1110	−4.961V	−9.922V	−19.844V	+0.019V	+0.039V	+0.078V
1111 1111	−4.981V	−9.961V	−19.922V	0.000V	0.000V	0.000V

DIGITAL OUTPUT	ANALOG INPUT — BIPOLAR RANGES		
	±2.5V	±5.0V	±10.0V
0000 0000	+2.500V	+5.00V	+10.000V
0000 0001	+2.481V	+4.961V	+9.922V
0111 1111	+0.019V	+0.039V	+0.078V
1000 0000	0.000V	0.000V	0.000V
1111 1110	−2.461V	−4.922V	−9.844V
1111 1111	−2.481V	−4.961V	−9.922V

BASIC GROUND PLANE LAYOUT



THIS BASIC GROUND PLANE LAYOUT SHOULD BE MODIFIED BEFORE IMPLEMENTATION TO INCLUDE UNUSED ANALOG INPUTS.

INPUT RANGE SELECTION

INPUT VOLTAGE RANGE	CONNECT ANALOG INPUT TO PIN	CONNECT PIN 8 TO PIN	CONNECT PIN 10 TO PIN
0 to −5V	11	12	7,9
0 to −10V	11	—	7,9
0 to −20V	12	—	7,9
0 to +5V	11	7,9,12	—
0 to +10V	11	7,9	—
0 to +20V	12	7,9	—
±2.5V	11	9,12	7
±5V	11	9	7
±10V	12	9	7

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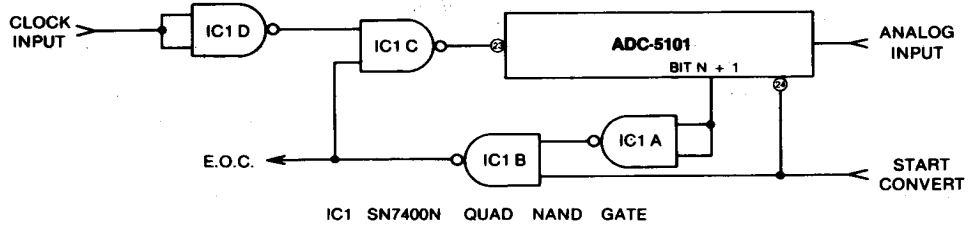

IC1 SN7400N QUAD NAND GATE

When less than 8-bit resolution is required, the ADC-5101 may be operated at higher conversion speeds by truncating the conversion when the desired number of bits have been converted. Connect the converter as shown in the logic diagram. The bit output used to drive gate "A" should be one more than the number of bits to be converted; for example, for 6 bits resolution, connect this gate to the bit 7 output.

MAXIMUM CONVERSION SPEEDS

BITS	CONVERSION SPEED
7	750 nanoseconds
6	650 nanoseconds
5	500 nanoseconds
4	400 nanoseconds

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
ADC-5101	0°C to +70°C
ADC-5101H	−55°C to +125°C

For military versions compliant to MIL-STD-883, contact DATEL.

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