

CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC40H174P/F

TC40H174 HEX D-TYPE FLIP-FLOP

The TC40H174 is a Hex D-type flip flop having common CLOCK and CLEAR terminal.




The logical input applied to input D is transmitted to output Q at the rising edge of CLOCK input.

CLEAR input is active at "L" level.

The pin assignment and function of this flip-flop are the same as those of the TTL74LS174.

Further, the same may be said of the TC40174BP.

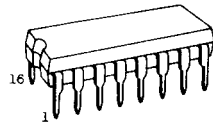
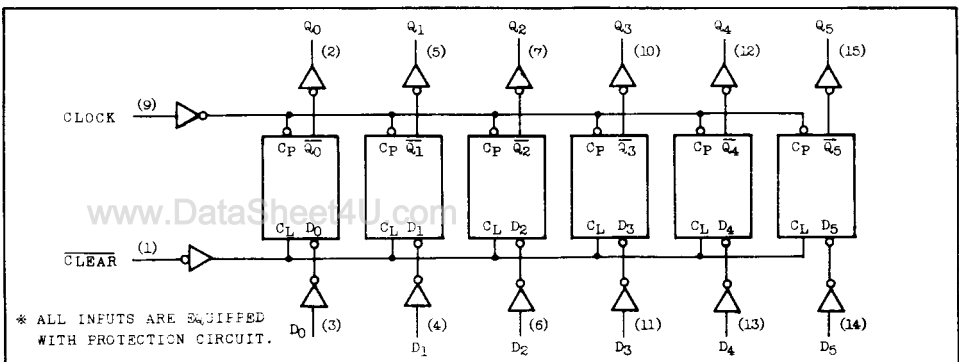
* Don't Care

INPUTS			OUTPUTS
CLOCK	D _n	CLEAR	Q _n
	H	H	H
	L	H	L
	*	H	No Change
*	*	L	L

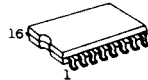
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	V _{SS} -0.5 ~ V _{SS} +10	V
Input Voltage	V _{IN}	V _{SS} -0.5 ~ V _{DD} +0.5	V
Output Voltage	V _{OUT}	V _{SS} -0.5 ~ V _{DD} +0.5	V
Input Current	I _{IN}	±10	mA
Power Dissipation	P _D	300 (DIP) / 180 (MFP)	mW
Storage Temperature	T _{stg}	-65 ~ 150	°C
Lead Temp./Time	T _{sol}	260°C • 10 sec	

LOGIC DIAGRAM

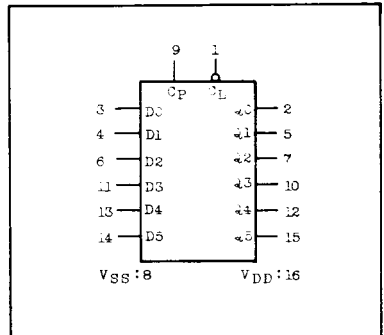


DIP16(3D16A-P)



MFP16(F16GC-P)

BLOCK DIAGRAM



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RECOMMENDED OPERATING CONDITIONS ($V_{SS}=0.0V$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD	-	2.0	-	8.0	V
Input Voltage	V _{IN}	-	0.0	-	VDD	V
Operating Temperature	T _{opr}	-	-40	-	85	°C

ELECTRICAL CHARACTERISTIC ($V_{SS}=0.0V$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	VDD (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V _{OH}	$ I_{OUT} < 1\mu A$ V _{IN} =V _{SS} , V _{DD}	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V _{OL}	$ I_{OUT} < 1\mu A$ V _{IN} =V _{SS} , V _{DD}	5	-	0.05	-	0.0	0.05	-	0.05	
High Level Output Current	I _{OH}	V _{OH} =4.6V V _{IN} =V _{SS} , V _{DD}	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current	I _{OL}	V _{OL} =0.4V V _{IN} =V _{SS} , V _{DD}	5	1.4	-	1.1	-	-	0.8	-	
Input Voltage	"H" Level V _{IH}	$ I_{OUT} < 1\mu A$ V _{OH} =4.5V	5	4.0	-	4.0	-	-	4.0	-	V
	"L" Level V _{IL}	V _{OL} =0.5V	5	-	1.0	-	-	1.0	-	1.0	
Input Current	"H" Level I _{IH}	V _{IH} =8.0V	8	-	0.3	-	10 ⁻⁵	0.3	-	1.0	μA
	"L" Level I _{IL}	V _{IL} =0.0V	8	-	-0.3	-	-10 ⁻⁵	-0.3	-	-1.0	
Quiescent Supply Current	I _{DD}	*V _{IN} =V _{SS} , V _{DD}	5	-	12.5	-	0.005	12.5	-	75	μA

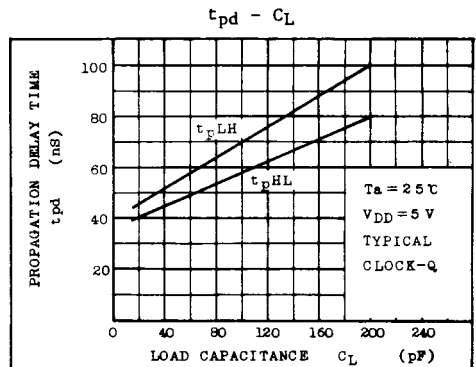
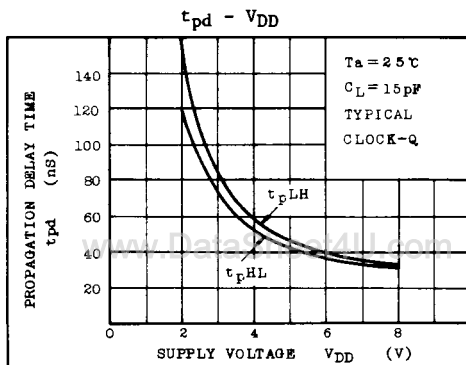
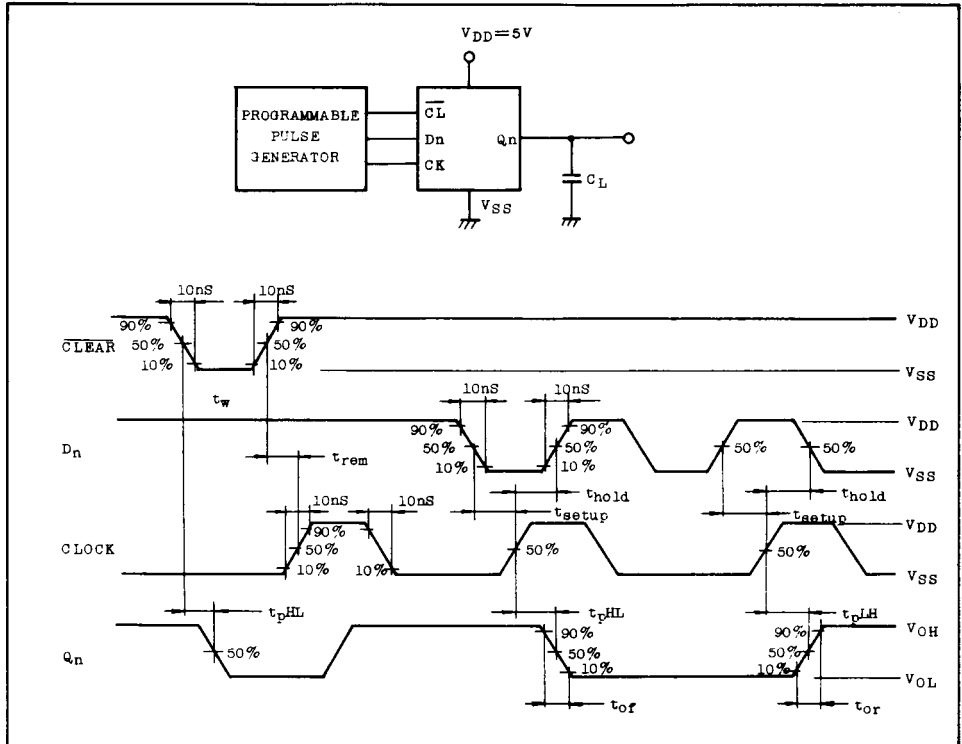
* All valid input combinations.

SWITCHING CHARACTERISTICS (T_a=25°C, V_{SS}=0V, C_L=15pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	VDD(V)	MIN.	TYP.	MAX.	UNIT	
Output Rise Time	t _{or}	-	5	-	20	35	ns	
Output Fall Time	t _{of}	-	5	-	15	30		
Propagation Delay Time	(Low-High)	t _{pLH}	CLOCK - Q	5	-	45	68	ns
	(High-Low)	t _{pHL}		5	-	40	60	
	(High-Low)	t _{pHL}		<u>CLEAR</u> - Q	5	-	48	
Min. Clear Width of Pulse	t _w	<u>CLEAR</u>	5	-	25	44	ns	
Max. Clock Rise Time Fall Time	t _{rφ} , t _{fφ}	-	5	1.0	12	-	μs	
Min. Data Hold Time	t _{hold}	-	5	-	-	5	ns	
Min. Data Setup Time	t _{set-up}	D _n - CLOCK	5	-	-	25	ns	
Max. Clock Frequency	f _{MAXφ}	-	5	10	20	-	MHz	
Input Capacitance	C _{IN}	-	5	-	5	-	pF	
Min. Clear Removal Time	t _{rem}	-	5	-	11	25	ns	

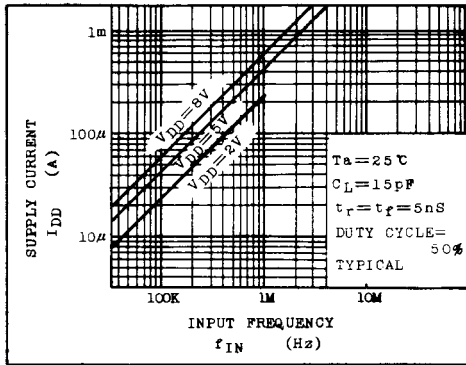
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SWITCHING TIME TEST CIRCUIT AND WAVEFORM

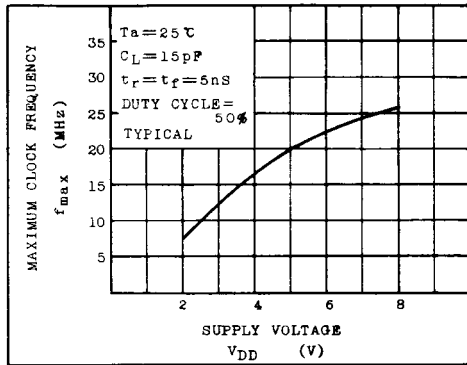


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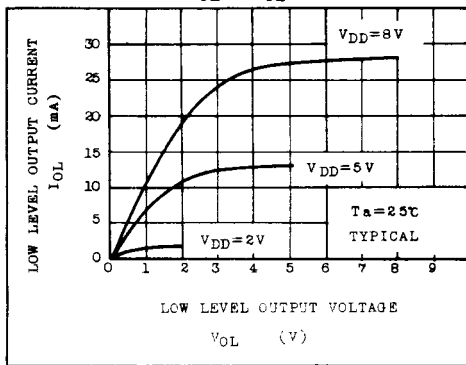
$I_{DD} - f_{IN}$



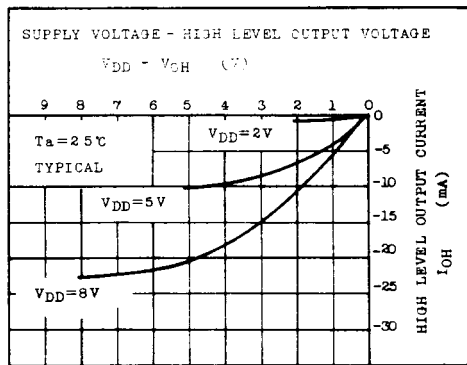
$f_{MAX\phi} - V_{DD}$



$I_{OL} - V_{OL}$



$I_{OH} - (V_{DD} - V_{OH})$



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