GP3842 HIGH PERFORMANCE CURRENT MODE CONTROLERS

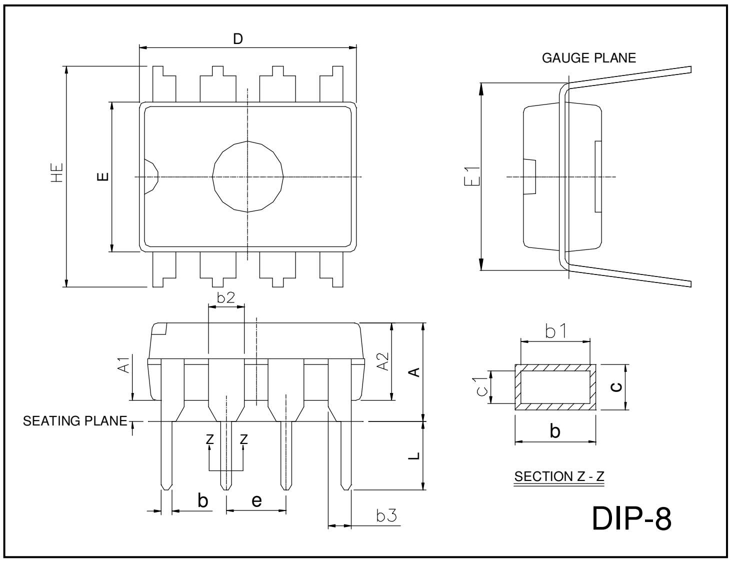
Description

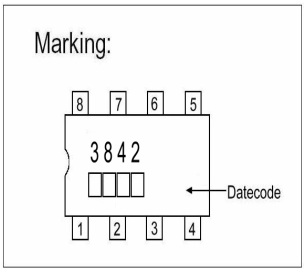
The GP3842 is high performance fixed frequency current mode controllers. This is specifically designed for Off-Line and DC TO DC converter applications offering the designer a cost-effective solution with minimal external components.
These integrated circuits feature a trimmed oscillator for precise duty cycle control. A temperature compensated reference, high gain Error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET. Also Included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, programmable output deadtime, and latch for single pulse metering.

Features

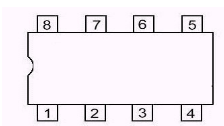
*Trimmed Oscillator for Precise Frequency Control
*Oscillator Frequency Guaranteed at 250kHz
*Current Mode Operation to 500kHz
*Automatic Feed Forward Compensation
*latching PWM for Cycle-By-Cycle Current Limiting
*Internally Trimmed Reference with Undervoltage Lockout
*High Current Totem Pole Output
*Undervoltage Lockout with Hysteresis
*Low Startup and Operating Current

Package Dimensions





REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	-	0.5334	c1	0.203	0.279
A1	0.381	-	D	9.017	10.16
A2	2.921	4.953	E	6.096	7.112
b	0.356	0.559	E1	7.620	8.255
b1	0.356	0.508	e	2.540 BSC	
b2	1.143	1.778	HE	-	10.92
b3	0.762	1.143	L	2.921	3.810
c	0.203	0.356			

DIP-8L	Function	Description
	Pin1:Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
	Pin2:Voltage Feedback	This is the inverting input of the Error Amplifier. It's normally connected to the Switching power supply output through a resistor divider.
	Pin3:Current Sense	A voltage proportional to inductor current is connected to this input .The PWM uses this information to terminate the output switch conduction.
	Pin4:RT/CT	The oscillator frequency and maximum output duty cycle are programmed by connecting resistor RT to Vref and capacitor CT to ground .Operation 500kHz is possible.
	Pin5:Ground	This pin is the combined control circuitry and power ground.
	Pin6:Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1 A are sourced and sunk by this pin.
	Pin7:Vcc	This pin is the positive supply of the control IC.
	Pin8:Vref	This is the reference output .It provides charging current for capacitor CT through resistor RT.

Absolute Maximum Ratings at Ta = 25℃

Parameter	Symbol	VALUE	Unit
Total power Supply and Zener current	(ICC+Iz)	30	mA
Output current,source or sink(note1)	Io	1.0	A
Output energy(capacitive load per cycle)	W	5.0	μJ

Current sense and voltage feedback inputs	Vin	-0.3 to 5.5	V
Error Amplifier Output Sink Current	Io	10	mA
Power Dissipation at Thermal characteristics	PD PθJA	702 178	mW ℃/W
Storage Temperature Range	Tstg	-65 to 150	℃
Operating Junction Temperature	TJ	+150	℃
Operating ambient Temperature	TA	0~+70	℃

Electrical Characteristics (0℃≤TA≤70℃,Vcc=15V[note 2],RT=10k,CT=3.3Nf,unless otherwise specified)

Parameter	SYMBOL	Test Conditions	Min	Typ.	Max.	Unit
Reference Section						
Output Voltage	VREF	Tj=25℃,Io=1mA	4.90	5	5.1	V
Line Regulation	Regline	Vcc=12V to 25V		2.0	20	mV
Load Regulation	Regload	Io=1mA to 20mA		3.0	25	mV
Temperature. Stability	Ts			0.2	-	mV/℃
Total Output Variation	VREF	Line, Load, Temperature	4.82	-	5.18	V
Output Noise Voltage	Vn	F=10kHz to 10Hz,Tj=25℃	-	50	-	μV
Long Term Stability	S	TA=125℃,1000Hrs	-	5	-	mV
Output Short Circuit current	ISC		-30	-85	-180	mA
Oscillator Section						
Frequency		Tj=25℃	49	52	55	KHz
		TA=0℃ to 70℃	48		56	
		Tj=25℃(RT=6.2k,CT=1.0nF)	225	250	275	
Frequency Change with Voltage	Δfosc/ΔV	Vcc=12V to 25V		0.2	1.0	%
Frequency Change with Temperature	Δfosc/ΔT	TA = 0℃ to 70 ℃		0.5		%
Oscillator Voltage Swing(Peak to Peak)	VOSC			1.6		V
Discharge Current	Idischg	Tj=25℃ TA = 0℃ to 70℃	7.8 7.6	8.3	8.8 8.8	mA
Error Amplifier Section						
Voltage Feedback Input	VFB	Vo =2.5V	2.42	2.50	2.58	V
Input Bias Current	IIB	VFB=5.0V		-0.1	-2.0	μA
Open Loop Voltage Gain	AVOL	Vo=2V to 4V	65	90		dB
Unity Gain Bandwidth	BW	Tj=25℃	0.7	1.0		MHz
Power Supply Rejection Ratio	PSRR	Vcc=12V to 25V	60	70		dB
Output Sink Current	Isink	Vo=1.1V,VFB=2.7V	2.0	12		mA
Output Source Current	Isource	Vo=5.0V,VFB=2.3V	-0.5	-1.0		mA
Output Voltage Swing High State	VOH	VFB=2.3V,RL=15K to GND	5.0	6.2		V
Output Voltage Swing Low State	VOL	VFB=2.7V,RL=15K to Vref		0.8	1.1	V
Current Sense section						
Current Sense Input Voltage gain	Av	(Note 3,4)	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold	Vth	(Note 3)	0.9	1.0	1.1	V
Power Supply Rejection Ratio	PSRR	VCC= 12 to 25V (Note 3)		70		dB
Input Bias Current	IIB			-2	-10	μA
Propagation Delay	Tplh(in/out)	Current Sense Input to Output		150	300	ns
Output Low Voltage	VOL	Isink=20mA		0.1	0.4	V
		Isink=200mA		1.6	2.2	V
Output High Level	VOH	Isource=20mA	13	13.5		V
		Isource=200mA	12	13.4		V
Output Voltage with UVLO Activated	VOL (UVLO)	VCC=6.0V,Isink=1.0mA		0.1	1.1	V
Output Voltage Rise Time	tr	Tj=25℃,CL=1nF		50	150	ns
Output Voltage Fall Time	tr	Tj=25℃,CL=1nF		50	150	ns

Under-Voltage Lockout Section						
Startup Threshold	Vth		14.5	16	17.5	V
Min. Operating Voltage After Turn-on(VCC)	VCC(min)		8.5	10	11.5	V
PWM Section						
Maximum Duty Cycle	DC(MAX)		94	96		%
Minimum Duty Cycle	DC(MIN)				0	%
Total Device						
Power Startup Supply Current	ICC+IC	VCC=14V		0.3	0.5	mA
Power Operating Supply Current	ICC+IC	Note 2		12	17	mA
Power Supply Zener Voltage	Vz	ICC=25mA	30	36		V

Note 1: Maximum Package power dissipation limits must be observed.
Note 2: Adject Vcc above the Startup threshold before setting to 15V.
Note 3: This parameter is measured at the latch trip point with VFB=0V.
Note 4: Comparator gain is defined as::

$$AV \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$$

Characteristics Curve

Figure 1. Timing Resistor versus Oscillator Frequency

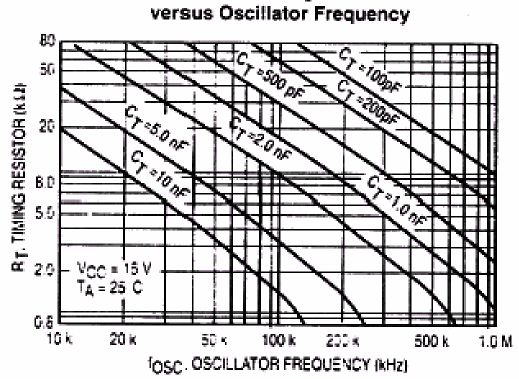


Figure 2. Output Deadtime versus Oscillator Frequency

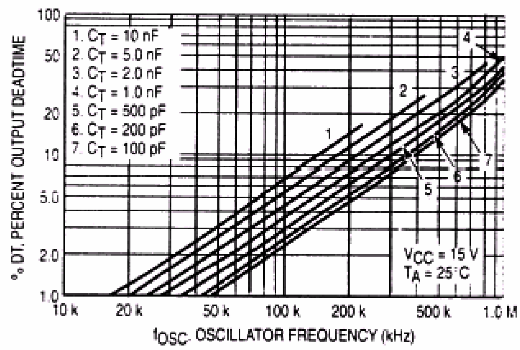


Figure 3. Oscillator Discharge Current versus Temperature

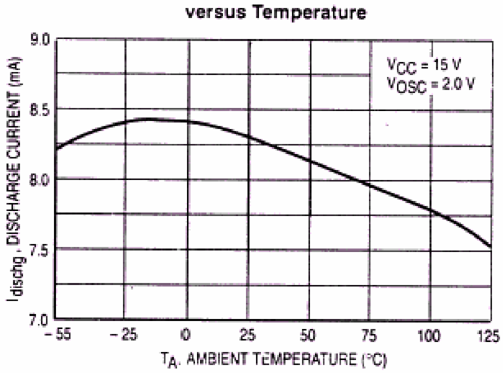


Figure 4. Maximum Output Duty Cycle versus Timing Resistor

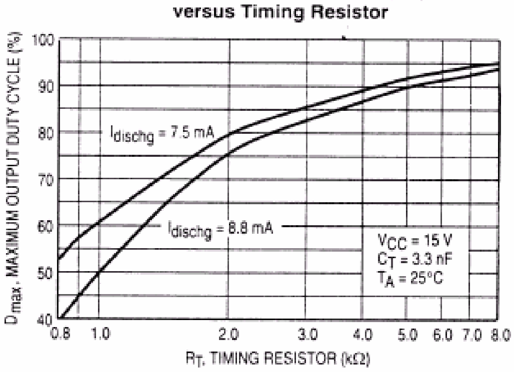


Figure 5. Error Amp Small Signal Transient Response

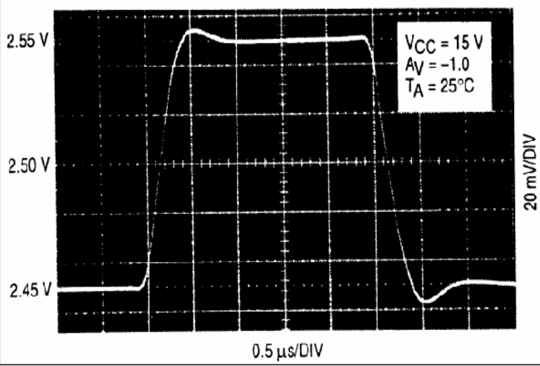


Figure 6. Error Amp Large Signal Transient Response

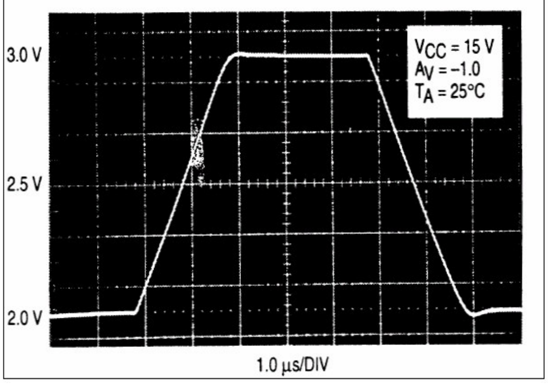


Figure 7. Error Amp Open Loop Gain and Phase versus Frequency

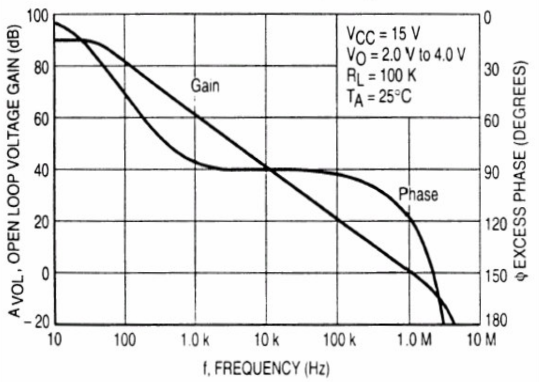


Figure 8. Current Sense Input Threshold versus Error Amp Output Voltage

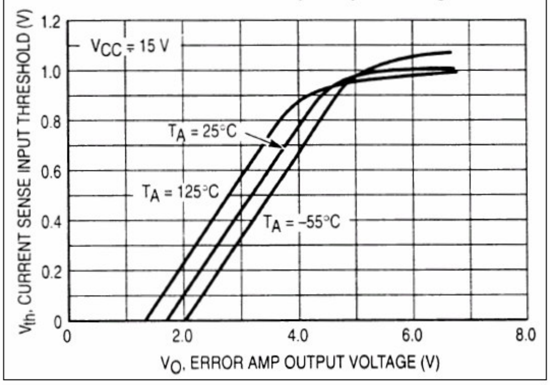


Figure 9. Reference Voltage Change versus Source Current

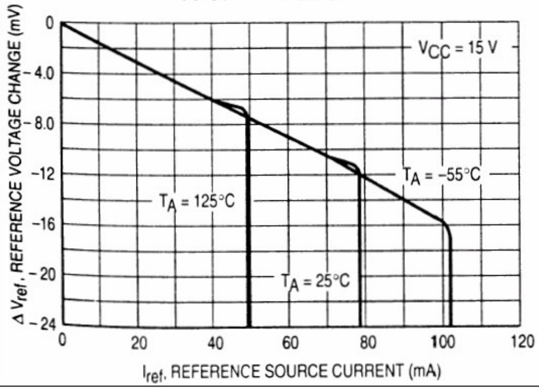


Figure 10. Reference Short Circuit Current versus Temperature

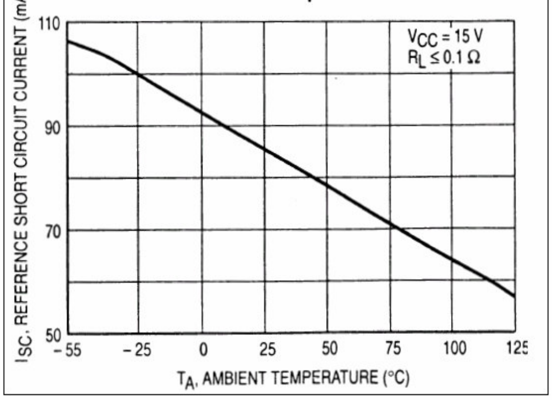


Figure 11. Reference Load Regulation

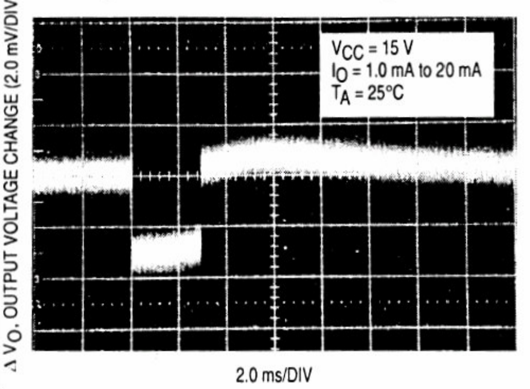


Figure 12. Reference Line Regulation

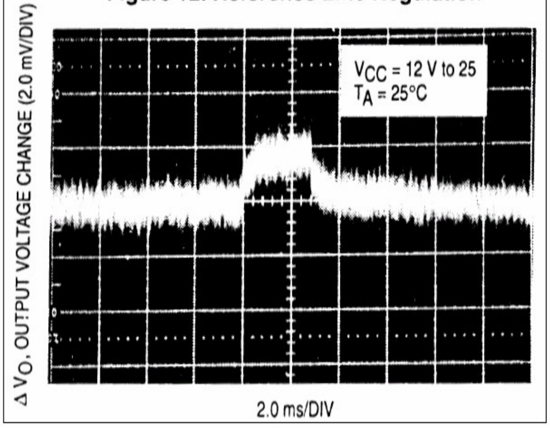


Figure 13. Output Saturation Voltage versus Load Current

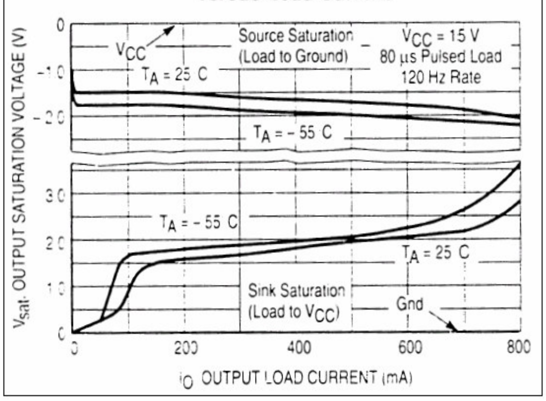


Figure 14. Output Waveform

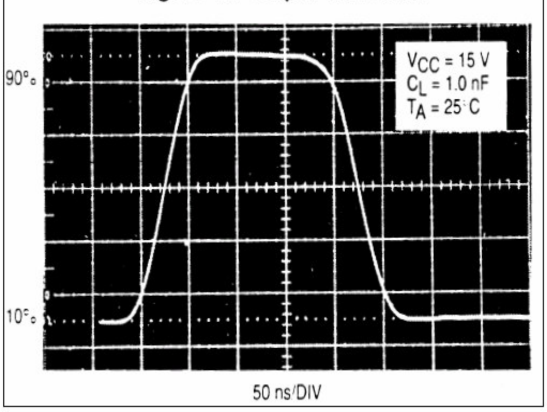


Figure 15. Output Cross Conduction

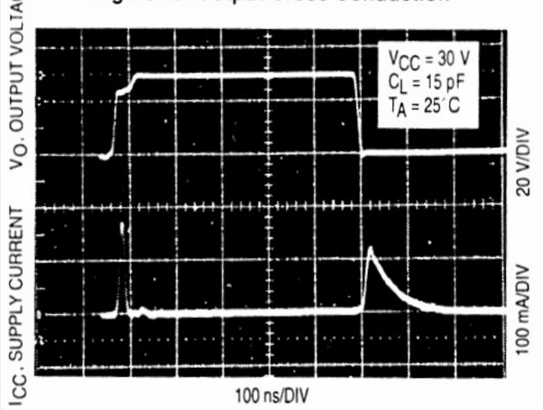
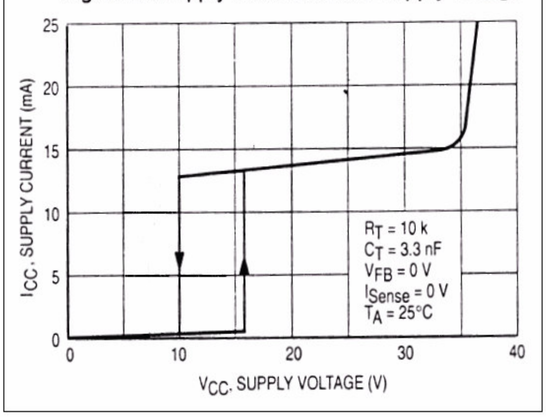
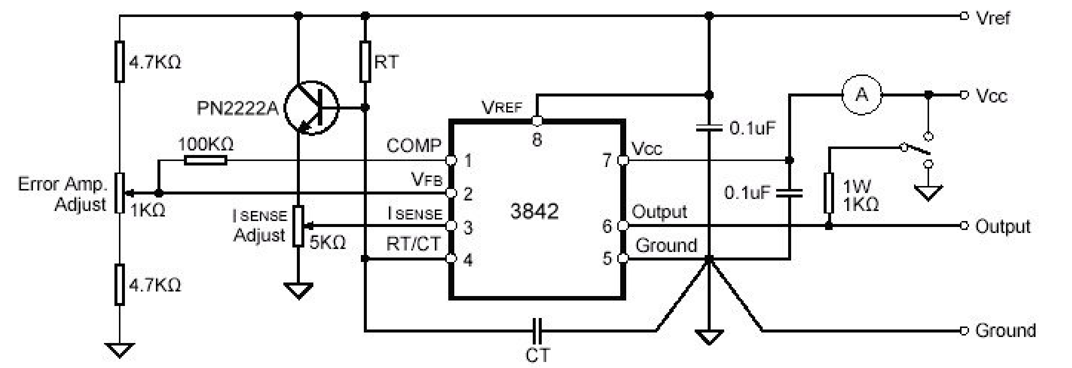


Figure 16. Supply Current versus Supply Voltage



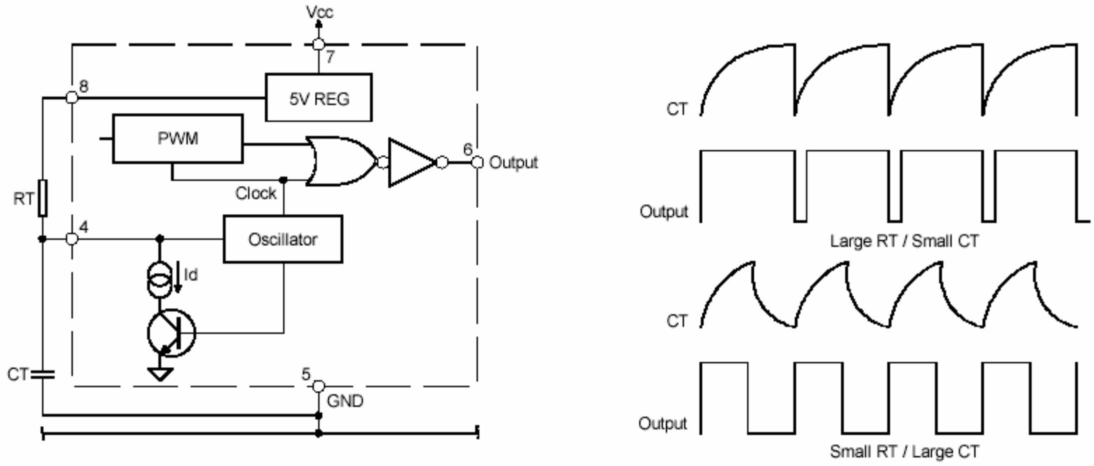
Application Information

Open Loop Test Circuit

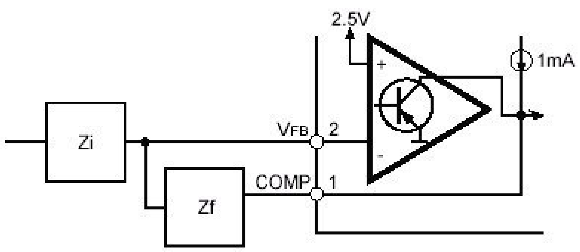


High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin5 in a single point ground. The transistor and 5KΩ potentiometerare used to samplethe oscillator waveform and apply an adjustable ramp to pin3.

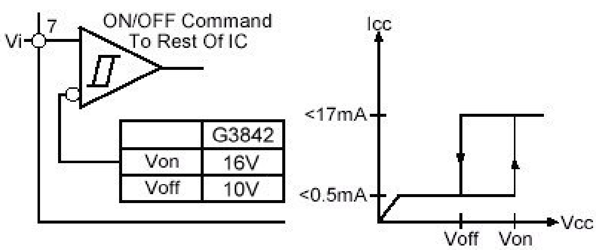
Oscillator and Output Waveforms



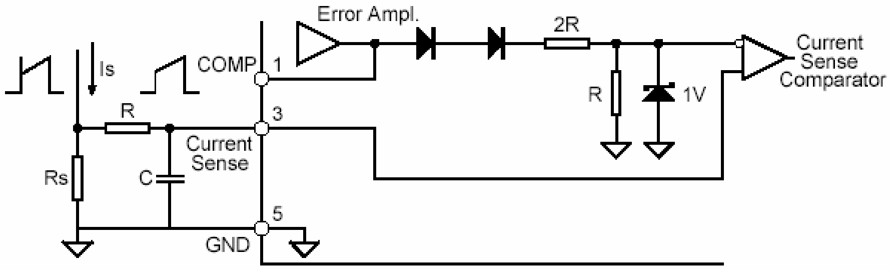
Error Amp Configuration



Under Voltage Lockout



Current Sense Circuit

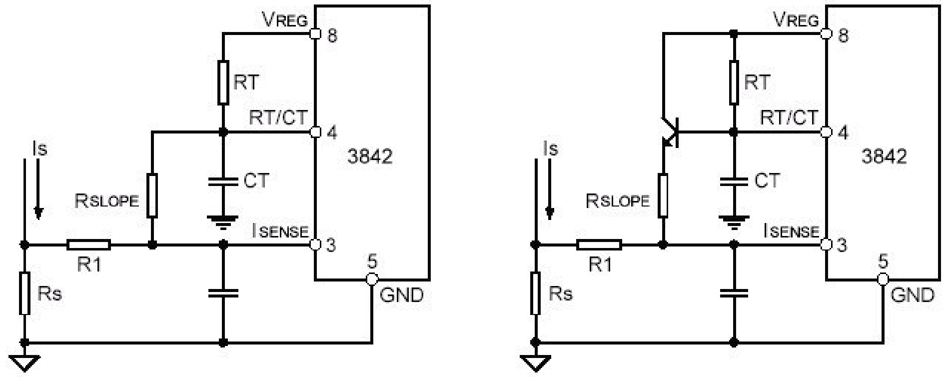


Peak current (Is) is determined by the formula

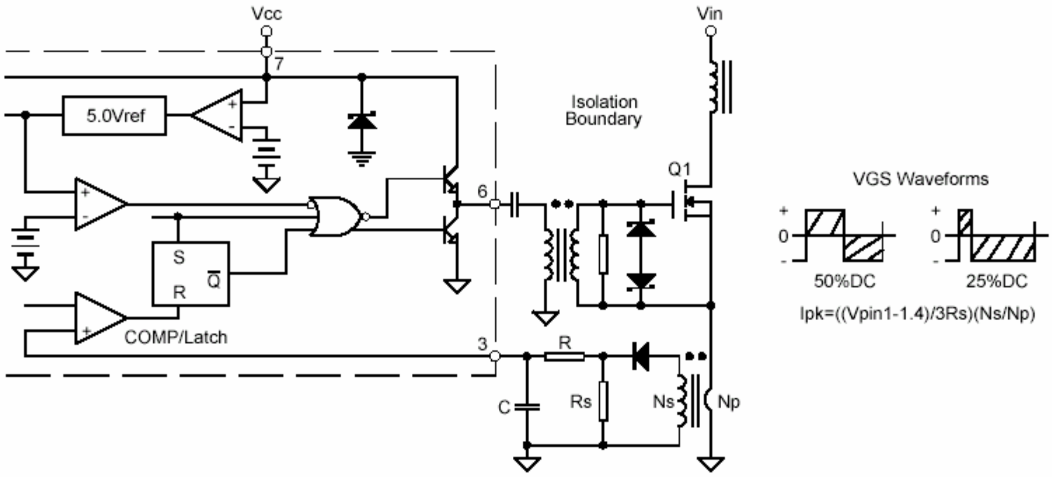
Is(max.) ≈ 1V/Rs

A small RC filter may be required to suppress switch transients.

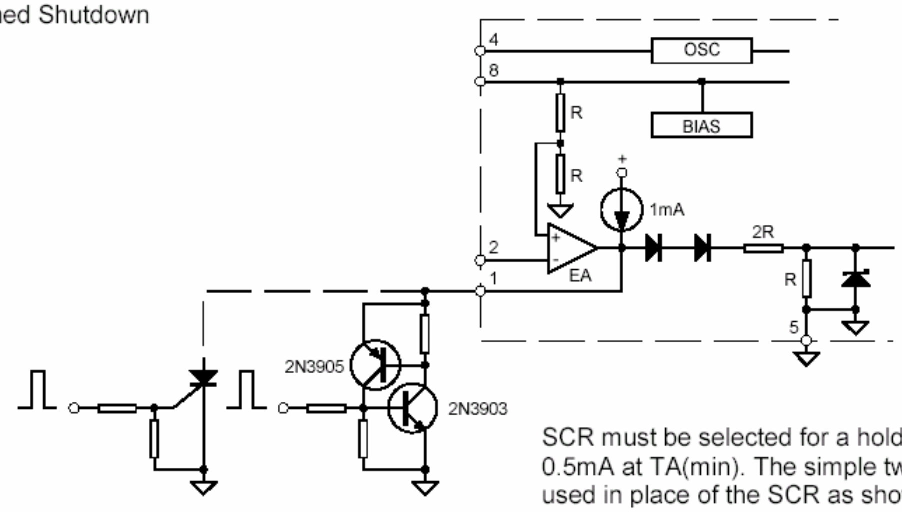
Slope Compensation Techniques



Isolated MOSFET Drive and Current Transformer Sensing

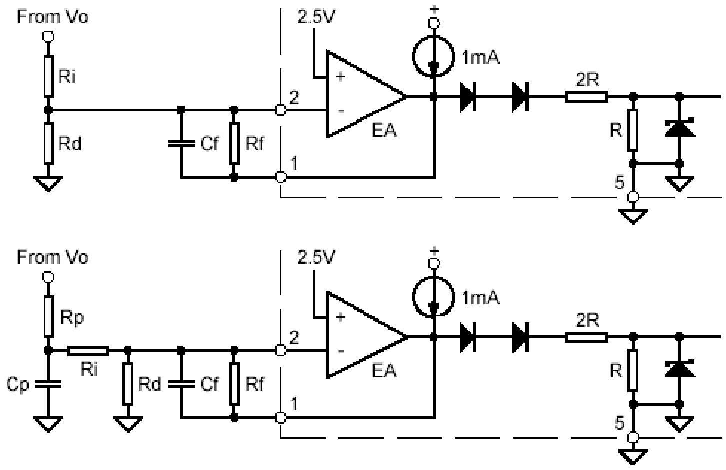


Latched Shutdown



SCR must be selected for a holding current of less than 0.5mA at TA(min). The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10K.

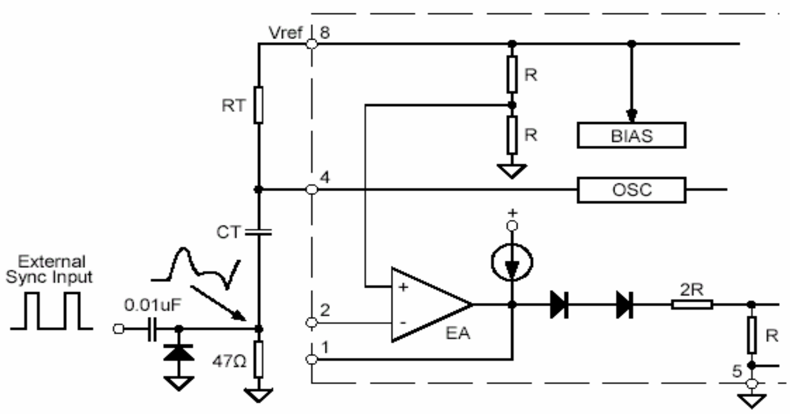
Error Amplifier Compensation



Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current

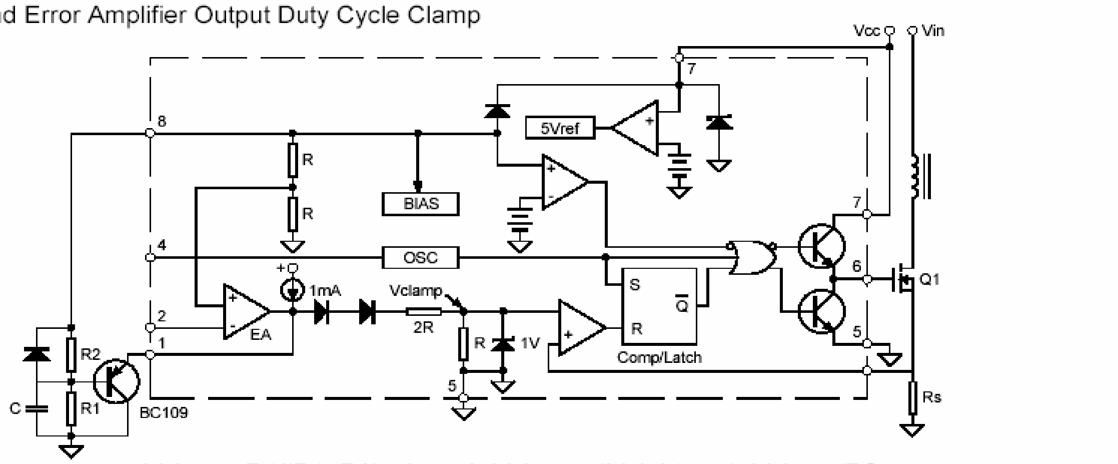
Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

External Clock Synchronization



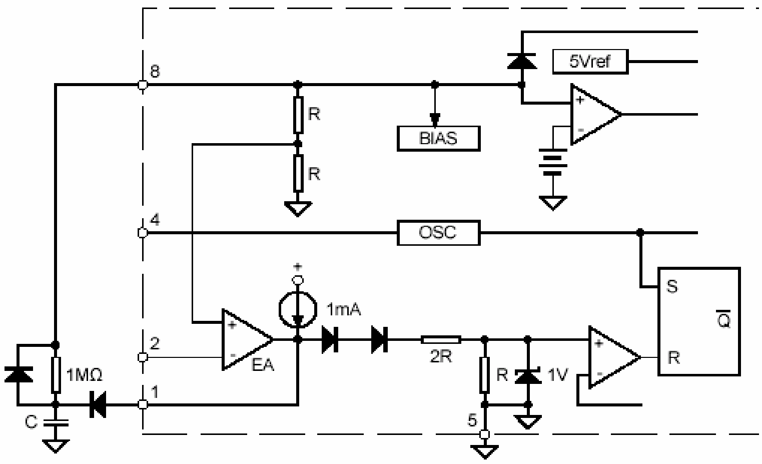
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of CT to go more than 300mV below ground

Soft-Start and Error Amplifier Output Duty Cycle Clamp

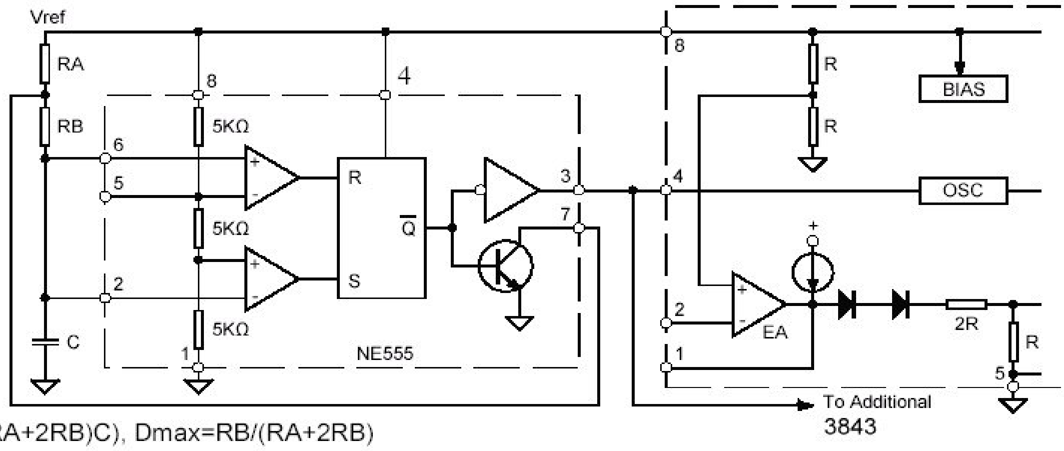


Vclamp=R1/(R1+R2) where 0<Vclamp<1V, Ipk(max)=Vclamp/RS

Soft-Start Circuit



External Duty Cycle Clamp and Multi Unit Synchronization



f=1.44/((RA+2RB)C), Dmax=RB/(RA+2RB)

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