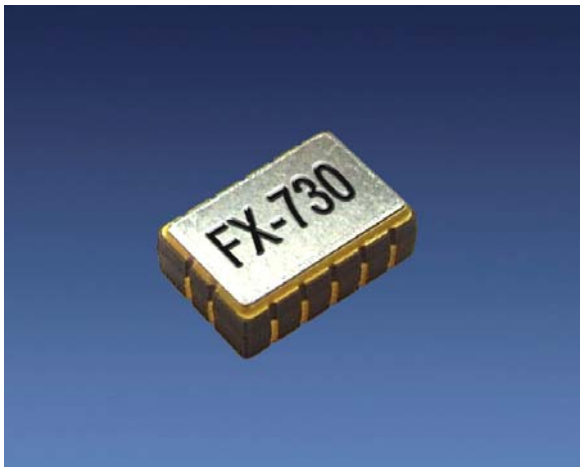
FX-730
Low Jitter VCSO Frequency Translator



Features

- 5 x 7.5 x 2.5 mm Package
- Frequency Translation up to 850 MHz
- VCSO based PLL for Ultra-Low Jitter
- CMOS / LVDS / LVPECL Inputs compatible
- Differential LVPECL or LVDS Output
- CMOS Lock Detect
- External Divider for Input Frequencies < 19 MHz
- 0°/70°C or -40°/+85°C Temperature Range
- Fully Compatible for Lead Free Assembly

Description

The FX-730 is a low jitter precision frequency translator used to translate input frequencies such as 19.44, 38.88, 77.76 MHz, etc. to a binary multiple frequency as high as 850 MHz. The FX-730's superior jitter performance is achieved through the PLL's integrated VCSO. The FX-730 is housed in a hermetically sealed leadless surface mount package offered on tape and reel.

Applications

Description	Standard
1-2-4 Gigabit FC	INCITS 352-2002
10 Gigabit FC	INCITS 364-2003
10GbE LAN / WAN	IEEE 802.3ae
OC-192	ITU-T G.709
SONET / SDH	GR-253-CORE Issue 3
FEC (Forward Error Correction) Scaling	

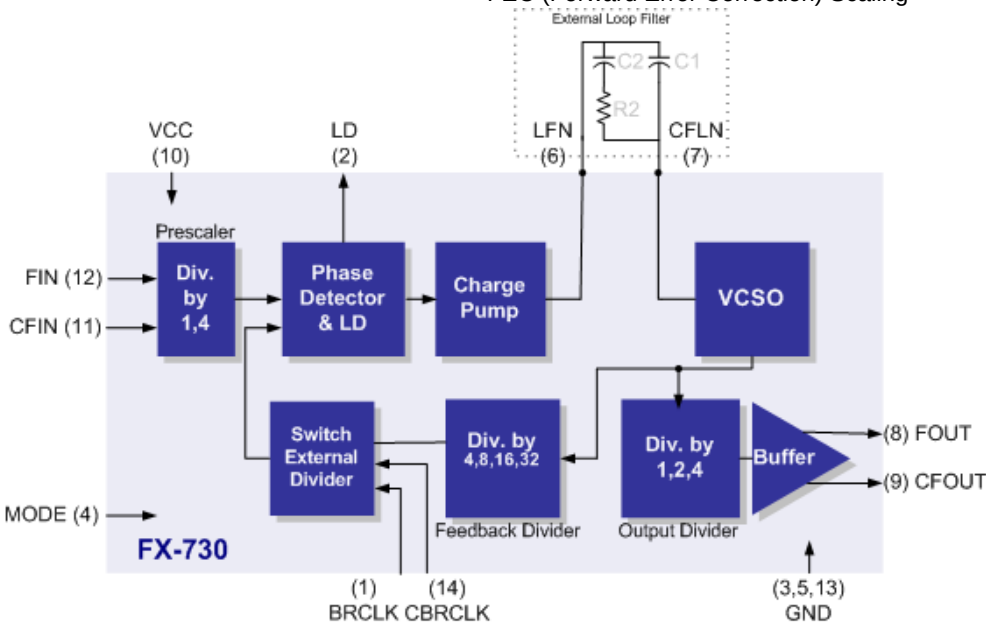


Figure 1. Functional Block Diagram

Table 1. Electrical Performance

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Frequency						
Input Frequency	F_{IN}	19.44		850	MHz	1,2,3
Output Frequency	F_{OUT}	125		850	MHz	1,2,3
Capture Range *(ordering option)*	APR	±32, ±50, or ±100			ppm	1,2,3
Supply						
Voltage	V_{CC}	2.97	3.3	3.63	V	2,3
Current (No Load)	I_{CC}			100	mA	3
LVCMOS Input						
Input High Voltage	V_{IH}	2		V_{CC}	V	2,3
Input Low Voltage	V_{IL}	0		0.8	V	
LVPECL Input						
Peak-Peak Amplitude Swing		0.20		3.00	V	6,7
Lock Detect Output						
Output High Voltage	V_{OH}	0.9*V_{CC}			V	
Logic Low Voltage	V_{OL}			0.1*V_{CC}	V	
Outputs						
Mid Level - LVPECL		V_{CC}-1.4	V_{CC}-1.25	V_{CC}-1.0	V	2,3
Swing - LVPECL		450	600	950	mV-pp	2,3
Mid Level - LVDS		V_{CC}-2.0	V_{CC}-1.6	V_{CC}-1.3	V	2,3
Swing - LVDS		250	410	450	mV-pp	2,3
Current	I_{OUT}			20	mA	5
Rise Time	t_R			400	ps	4,5
Fall Time	t_F			400	ps	4,5
Symmetry	SYM	45	50	55	%	2,3
Jitter Generation - 622.08 MHz output						
(12 kHz – 20 MHz BW)	Φ_J		0.21	0.5	ps-rms	5
(50 kHz – 80 MHz BW)	Φ_J		0.12	0.4	ps-rms	5
Operating Temp. *(ordering option)*	T_{OP}	0/70, -40/85			°C	1,3

1. See Standard Frequencies and Ordering Information.
2. Parameters are tested with production test circuit below (Fig 1).
3. Parameters are tested at ambient temperature with test limits guard banded for specified operating temperature.
4. Measured from 20% to 80% of a full output swing (Fig 2).
5. Not tested in production, guaranteed by design, verified at qualification.
6. Minimum Input Low Voltage not to exceed 2.125 V. Minimum Input High Voltage not to go below 1.49 V.
7. AC coupling is recommended. There is an internal pull-up and pull-down resistor on all clock inputs (Fin, BRCLK).

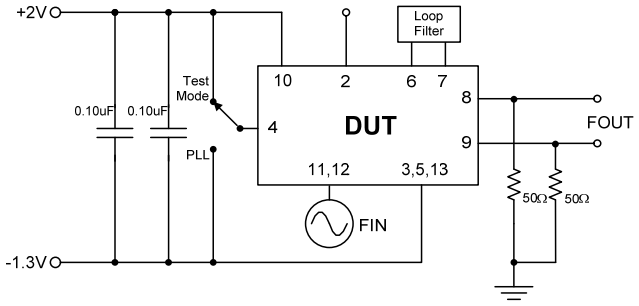


Figure 1. LVPECL Test Circuit

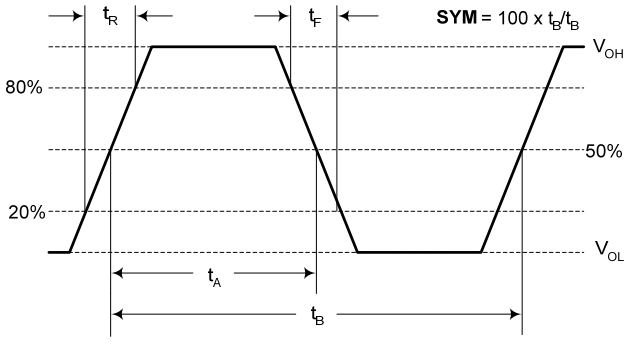


Figure 2. 10K LVPECL Waveform

Outline Diagram

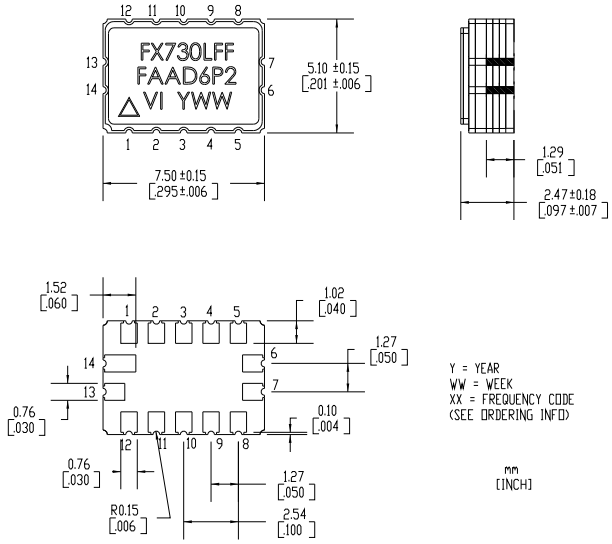


Figure 3.

Suggested Pad Layout

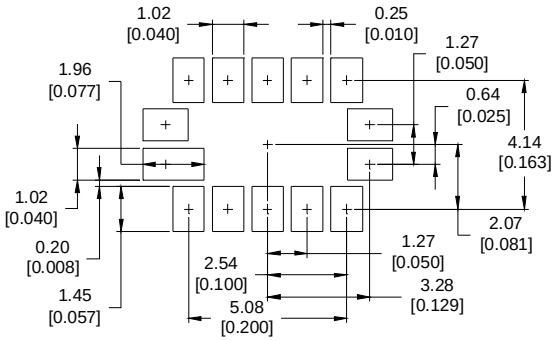


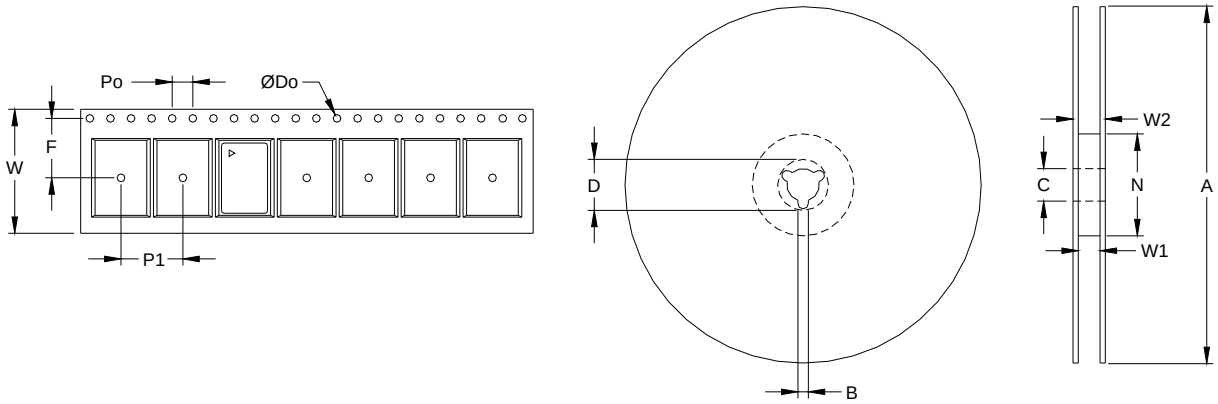
Figure 4.

Table 2. Pin Out

Pad #	Symbol	I/O	Level	Function
1	BRCLK	I	NC or LVPECL, LVDS	NC or For external divider applications = PD Feedback Frequency
2	LD[1]	O	CMOS	Lock Detect Logic "0" = FX Locked Logic "1" = No input Output transitioning = Out of Lock
3	GND	GND	Supply	Case and Electrical Ground
4	MODE[2]	I	CMOS	FX Operating Mode Logic "0" = Standard PLL Operation *Normal setting* Logic "1" = FIN coupled to FOUT
5	GND	GND	Supply	Case and Electrical Ground
6	LFN		Analog	Loop Filter Node
7	CLFN		Analog	Complementary Loop Filter Node
8	FOUT	O	LVPECL or LVDS	Frequency Output
9	CFOUT	O	LVPECL or LVDS	Complementary Frequency Output
10	VCC	I	Supply	Power Supply Voltage (+3.3V ±5%)
11	CFIN	I	LVPECL	Complementary Input Frequency For CMOS inputs, AC-couple unused input to ground or negative supply.
12	FIN	I	CMOS or LVPECL	Input Frequency
13	GND	GND	Supply	Case and Electrical Ground
14	CBRCLK	I	NC or LVPECL, LVDS	NC or For external divider applications = Comp. PD Feedback Frequency

1. It is recommended that a buffer driver is used for best noise isolation.
2. Do not leave the MODE pin floating, it should be set to logic 0 or ground for normal operation.
3. BRCLK and CBRCLK should be left floating if not used.
4. FIN, CFIN, BRCLK, and CBRCLK have internal pull-up/pull-down resistors and it is recommended to AC couple these inputs.

Tape and Reel (EIA-481-2-A)



Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	Reel
FX-730	16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{CC}	0 to 6	V
Input Current	I_{IN}	100	mA
Output Current	I_{OUT}	25	mA
Storage Temperature	T_{STR}	-55 to 125	°C
Soldering Temperature/Duration	T_{PEAK} / t_P	260 / 40	°C/sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Also, exposure to these absolute maximum ratings for extended periods can adversely affect device reliability. Functional operation is not implied at these or any other conditions in excess of those represented in the operational sections of this data sheet. Permanent damage is also possible if any device input draws greater than 100 mA.

Application Circuits

Please contact Vectron application engineering for assistance.

Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The FX-730 family is undergoing the following qualification tests:

Table 4. Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016
Moisture Sensitivity Level Rating	MSL 1

Handling Precautions

Although ESD protection circuitry has been designed into the FX-730 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM), a charged-device model (CDM), and machine model (MM) for ESD susceptibility testing and design protection evaluation.

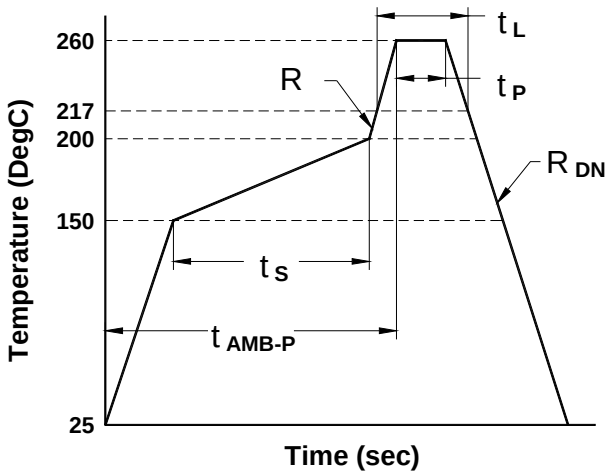
Table 5. ESD Ratings – LVPECL Output

Model	Class	Minimum	Conditions
Human Body Model	1A	350 V	MIL-STD 883, Method 3015
Charged Device Model	C5	1000 V	JEDEC, JESD22-C101
Machine Model	M1	50 V	ESD STM5.2-1999

Table 6. Reflow Profile (IPC/JEDEC J-STD-020C)

Parameter	Symbol	Value
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The device has been qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The FX-730 device is hermetically sealed so an aqueous wash is not an issue.



Standard Frequencies (MHz)

18.7500	EE	28.7040	F1	42.6600	JZ	65.5360	J6	114.0000	L3	318.7500	PV	665.6256	PC
19.2000	DD	29.4912	F5	44.2095	KX	66.0000	JA	120.0000	LC	320.0000	PP	666.5143	P5
19.3927	DX	29.5000	F9	44.4343	LF	70.0000	KB	122.8800	LB	322.2656	PW	669.1281	R2
19.4400	D6	30.0000	HE	44.6218	JW	70.6560	KC	124.4160	L7	328.7109	PX	669.3266	R3
19.5313	DZ	30.7200	H1	44.7360	J3	71.6100	KF	125.0000	L4	333.2571	PY	669.6429	R1
19.6608	DB	30.8800	HF	44.9280	JE	73.7280	K8	130.0000	LD	334.6633	RB	670.8386	R7
19.6990	DK	31.2500	H8	45.1584	JG	74.1250	K1	139.2640	L5	336.0813	RC	672.1627	R5
19.7190	DH	32.0000	H2	45.8240	JM	74.1758	KA	150.0000	M8	353.6763	RD	673.4566	RA
19.9219	ED	32.7680	H3	46.7200	JK	74.2500	K7	150.1440	M6	375.0000	RF	684.2554	R9
20.0000	E2	33.0000	H7	46.8750	JY	75.0000	KH	155.5200	M2	409.6000	RE	690.5692	R4
20.1416	E3	33.3330	HC	48.0000	JV	76.8000	K4	156.2500	M3	491.5200	PM	693.4830	R6
20.4800	E4	34.3680	H6	49.1520	J7	77.7600	K2	159.3750	M7	531.0000	PH	693.7500	R8
20.5444	EF	34.5600	HB	49.4080	J2	78.1250	K3	160.0000	M1	531.2500	P8	704.3806	TG
20.7135	E1	36.8640	HG	50.0000	JD	78.6432	K5	161.1328	M4	568.9286	PJ	707.3527	TC
20.8286	EB	37.0560	H4	50.0480	KD	79.6875	KG	164.3554	M9	569.1964	P9	710.9486	T2
20.9165	EH	37.1250	H9	51.8400	J4	80.0000	K9	166.6286	M5	595.0560	PL	716.5732	T1
21.0051	EJ	37.5000	HK	52.0000	JP	80.5664	KJ	167.3316	N2	600.0000	PR	718.7500	T5
22.0000	E9	38.8800	H5	53.3300	JU	82.1777	KL	168.0407	N3	622.0800	P2	719.7344	T3
22.1048	EK	39.0625	HH	54.7460	JL	82.9440	K6	170.0000	N4	624.6938	PD	748.0709	T6
22.2171	E5	39.3216	HD	55.0000	JX	83.3142	KN	176.8381	NA	624.7048	P6	750.0000	T7
22.5792	E8	39.8438	HJ	60.0000	JR	83.6658	KR	182.0160	N8	625.0000	P3	777.6000	T4
24.0000	EC	40.0000	JF	61.3800	KY	84.0203	KU	187.5000	N5	627.3296	P7	779.5686	T8
24.5760	E6	40.2831	KK	61.4400	J5	88.4190	KW	195.0000	N7	629.9878	PA	780.8810	TD
24.7040	E7	40.9600	J1	62.2080	J8	97.5000	KE	200.1920	N6	637.5000	PG	781.2500	T9
25.0000	F7	41.0889	KM	62.5000	J9	100.0000	L8	201.4160	N1	640.0000	PN	796.8750	TB
25.1658	F8	41.6571	KP	62.9145	LE	105.0000	L6	245.7600	N9	644.5313	P4	805.6641	TA
25.6000	F6	41.8329	KT	63.3600	JJ	106.2500	L9	262.1440	NB	647.2394	PE	809.0635	TE
25.9200	F2	42.0000	JB	63.8976	JN	108.0000	LA	300.0000	PT	647.2508	PK	819.2000	TH
26.0000	F3	42.0102	KV	64.0000	JT	110.0000	L1	311.0400	P1	649.9703	PF	821.7773	TF
27.0000	F4	42.5000	JC	64.1520	JH	112.0000	L2	312.5000	PU	657.4219	PB		

Ordering Information

FX-730 - X X X - X X X - XX-XX

Product Family
FX: Frequency Translator

Package
730: 5.0 x 7.5 x 2.2 mm

Supply Voltage
L: 3.3 Vdc

Output
F: LVPECL (45/55% symmetry)
P: LVDS (45/55% symmetry)

Operating Temperature
C: 0 to 70°C
F: -40 to 85°C

Lock(APR) Range
F: ± 32 ppm
G: ± 50 ppm
H: ± 100 ppm

Feedback Divider[2]
A: Factory set
B: External divider, prescaler = 1
C: External divider, prescaler = 4

Output Divider[2,3]
A: Factory set

Input Frequency[1,2]
See Above

Output Frequency[1,3]
See Above

1. Not all combinations are possible. Please consult with your Vectron marketing representative for application assistance. Other frequencies available upon request.
2. When ordering the FX-730 with the external divider option, the prescaler must be specified (i.e., 1 or 4). The "XX" place holder should be used for the input frequency.
3. Note that the Output Frequency = Internal VCSO/Output Divider. 500 MHz ≤ VSCO Frequency ≤ 850 MHz.

For Additional Information, Please Contact:

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Revision History:

Revision	Date	PLM Approval	Eng req'd	Engineer Approval	Date	Description
1	11/15/06	BW				Original Release
1.1	6/19/07	BW				Added “C” option to Feedback Divider field under Ordering Information. Updated Standard Frequencies.
1.2	7/24/07	BW				Input amplitude, APR, frequency codes, ordering information.