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Preliminary

uP6210

Compact Dual-Phase
Synchronous-Rectified Buck Controller

General Description

The uP6210 is a compact dual-phase synchronous-rectified Buck controller specifically designed to deliver high quality output voltage for high power applications. This part is capable of delivering up to 60A output current thanks to its embedded bootstrapped drivers that support 12V + 12V driving capability. The uP6210 features configurable gate driving voltage for maximum efficiency and optimal performance. The built-in bootstrap diode simplifies the circuit design and reduces external part count and PCB space.

The output voltage is precisely regulated to the reference input that is dynamically adjustable by external voltage divider. The uP6210 adopts DCR current sensing technique for over current protection and droop control. The adjustable current balance is achieved by $R_{DS(ON)}$ current sensing technique.

This part features comprehensive protection functions including over current protection, input/output under voltage protection, over voltage protection and over temperature protection.

Other features include adjustable soft start, adjustable operation frequency, and quick response to step load transient. With aforementioned functions, this part provides customers a compact, high efficiency, well-protected and cost-effective solutions. This part comes to VQFN4x4-24L package.

Ordering Information

Order Number	Package Type	Remark
uP6210AQAG	VQFN 4x4-24L	

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 and RoHS requirements. They are 100% matte tin (Sn) plating and suitable for use in SnPb or Pb-free soldering processes.

Features

☐ **Operate with Single Supply Voltage**

☐ **±2.0% Over Line Voltage and Temperature**

☐ **Simple Single-Loop Voltage-Mode Control**

☐ **12V Bootstrapped Drivers with Internal Bootstrap Diode**

☐ **Adjustable Over Current Protection by DCR Current Sensing**

☐ **Adjustable Current Balancing by $R_{DS(ON)}$ Current Sensing**

☐ **Adjustable Operation Frequency form 50kHz to 1MHz Per Phase**

☐ **External Compensation**

☐ **Dynamic Output Voltage Adjustment**

☐ **Adjustable Soft Start**

☐ **VQFN4x4-24L Package**

☐ **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

☐ **Middle-High End GPU Core Power**

☐ **High End Desktop PC Memory Core Power**

☐ **Low Output Voltage, High Power Density DC-DC Converters**

☐ **Voltage Regulator Modules**

Pin Configuration

VQFN4x4-24L
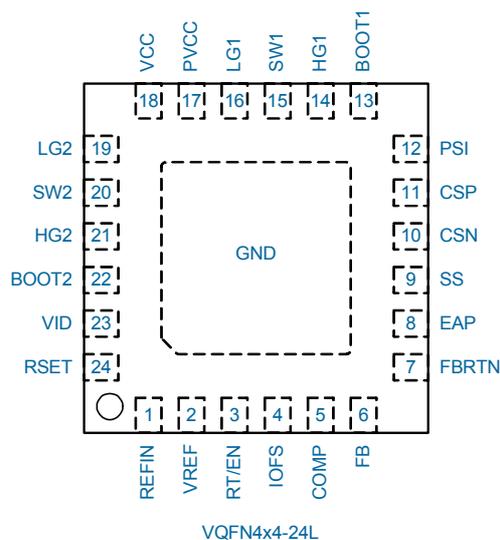
Typical Application Circuit
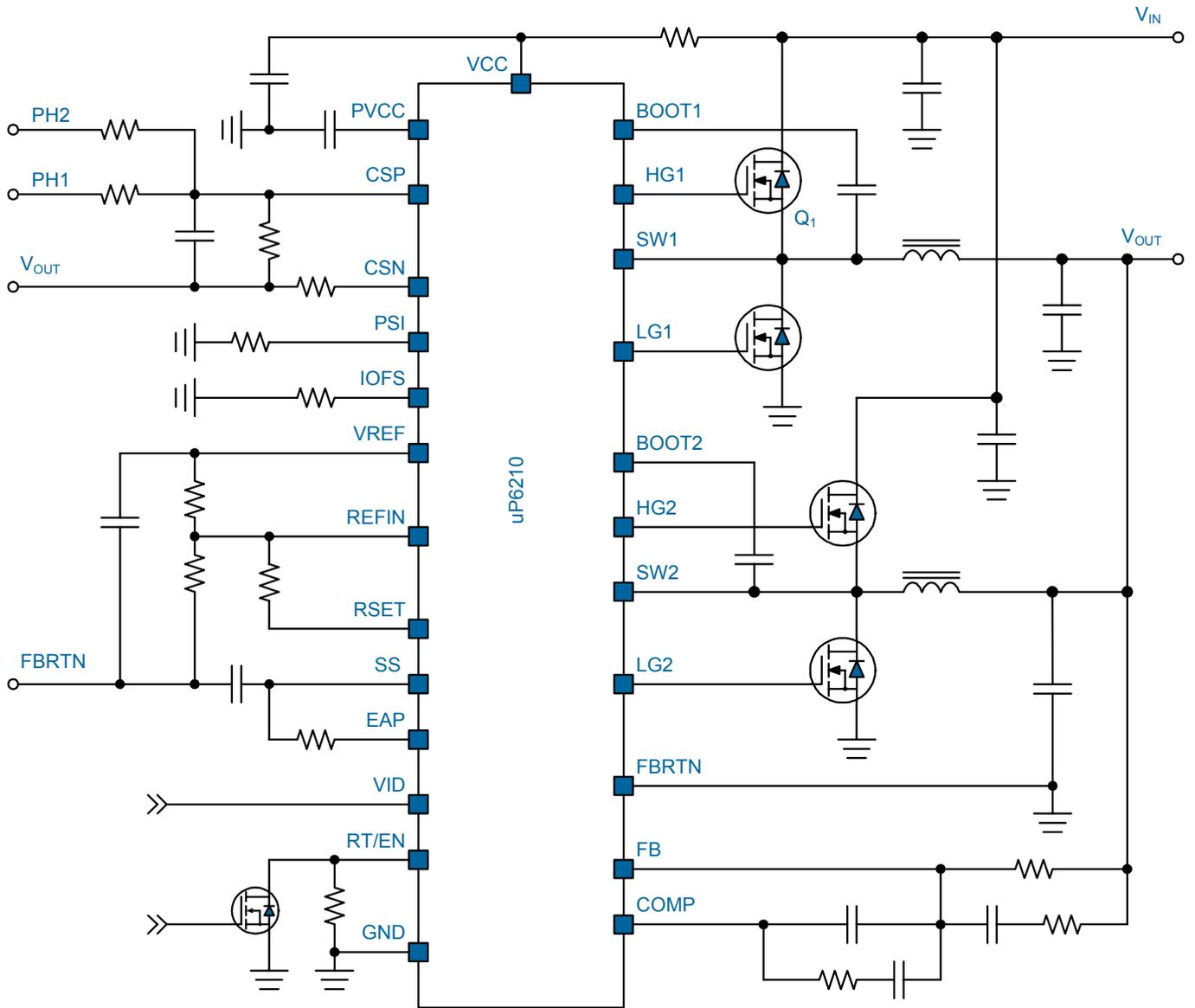
Functional Pin Description

No.	Pin Name	Pin Function
1	REFIN	**External Reference Input.** This is input pin of external reference voltage. Connect a voltage divider from VREF to REFIN to FBRTN to set the reference voltage.
2	VREF	**Output for Reference Voltage.** This is the output pin of high precision 2V reference voltage. Bypass this pin with a 1uF ceramic capacitor to FBRTN.
3	RT/EN	**Operation Frequency Setting.** Connecting a resistor between this pin and GND to set the operation frequency. Pull this pin to ground to shut down the uP6210.
4	IOFS	**Current Balance Adjustment.** Connect a resistor from this pin to VREF or GND to adjust the current sharing.
5	COMP	**Error Amplifier Output.** This is the output of the error amplifier (EA) and the non-inverting input of the PWM comparators. Use this pin in combination with the FB pin to compensate the voltage-control feedback loop of the converter.
6	FB	**Feedback Voltage.** This pin is the inverting input to the error amplifier. Use this pin in combination with the COMP pin to compensate the voltage control feedback loop of the converter.
7	FBRTN	**Feedback Return.** Connect this pin to the gound pin where the output voltage is to be regulated.
8	EAP	**Non-Inverting Input of Error Amplifier.** Connect a resistor to SS pin to set the droop slope.
9	SS	**Soft Start Output.** Connect a capacitor to FBRTN to set the soft start interval.
10	CSN	**Negative Input for Current Sensing Amplifier.**
11	CSP	**Positive Input for Current Sensing Amplifier.**
12	PSI	**Power Saving Mode.** Connect a resistor from PSI to GND to set the power saving mode threshold current level. Connect this pin to VREF for always two phase operation. Short this pin to ground for always single phase operation.
13	BOOT1	**Bootstrap Supply** for the floating upper gate driver of channel 1. Connect the bootstrap capacitor C_{BOOT} between BOOT1 pin and the SW1 pin to form a bootstrap circuit.
14	HG1	**Upper Gate Driver Output for Channel 1.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
15	SW1	**Switch Node for Channel 1.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
16	LG1	**Lower Gate Driver Output for Channel 1.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
17	PVCC	**Supply Voltage for Gate Driver.** This pin is the output of internal 9V LDO. This pin provides current for gate drives. Bypass this pin with a minimum 1uF ceramic capacitor.
18	VCC	**Supply Voltage.** This pin provides current for internal control circuit and 9V LDO. Bypasse this pin with a minimum 1uF ceramic capacitor next to the IC.

Preliminary   **uP6210**

Functional Pin Description

No.	Pin Name	Pin Function
19	LG2	**Lower Gate Driver Output for Channel 2.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
20	SW2	**Switch Node for Channel 2.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the HG2 driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
21	HG2	**Upper Gate Driver Output for Channel 2.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
22	BOOT2	**Bootstrap Supply** for the floating upper gate driver of channel 2. Connect the bootstrap capacitor C_{BOOT} between BOOT2 pin and the SW2 pin to form a bootstrap circuit.
23	VID	**VID Input.** This pin is used to adjust reference voltage. Logic high turns on the internal MOSFET connected to RSET pin.
24	RSET	**Reference Voltage Setting.** This pin is an open drain output that is pulled low when VID = high. Connect a resistor from this pin to REFIN pin to set the reference voltage.
Exposed Pad GND		**Power Ground.** Tie this pin to the ground island/plane through the lowest impedance connection available.

Functional Block Diagram

Functional Description

The uP6210 is a compact dual-phase synchronous-rectified Buck controller specifically designed to deliver high quality output voltage for high power applications. This part is capable of delivering up to 60A output current thanks to its embedded bootstrapped drivers that support 12V + 12V driving capability. The uP6210 features configurable gate driving voltage for maximum efficiency and optimal performance. The built-in bootstrap diode simplifies the circuit design and reduces external part count and PCB space.

The output voltage is precisely regulated to the reference input that is dynamically adjustable by external voltage divider. The uP6210 adopts DCR current sensing technique for over current protection and droop control. The adjustable current balance is achieved by $R_{DS(ON)}$ current sensing technique.

This part features comprehensive protection functions including over current protection, input/output under voltage protection, over voltage protection and over temperature protection.

Other features include adjustable soft start, adjustable operation frequency, and quick response to step load transient. With aforementioned functions, this part provides customers a compact, high efficiency, well-protected and cost-effective solutions. This part comes to VQFN4x4-24L package.

Power On Reset and Initialization

The uP6210 works with a single supply voltage at VCC pin. The VCC voltage is continuously monitored for power on reset (POR) to ensure the supply voltage is high enough for normal operation of the device. The POR threshold level is typically 9V at VCC rising.

9V LDO for Gate Drivers

The uP6210 provides flexible gate driving voltage for maximum efficiency and optimal performance. A linear regulator provides 9V voltage at PVCC pin for gate drives. 9V driving voltage reduces the power dissipation at uP6210 to an acceptable level at large gate capacitance and high switching frequency applications. Bootstrap diodes are embedded to facilitates PCB design and reduce the total BOM cost. No external Schottky diode is required.

Chip Enable Oscillation Frequency Programming

A resistor R_{RT} connected to RT pin programs the oscillation frequency as:

$$f_{OSC} = \frac{10000}{R_{RT}(k\Omega)} \qquad \text{(kHz)}$$

Figure 1 shows the relationship between oscillation frequency and R_{RT}.
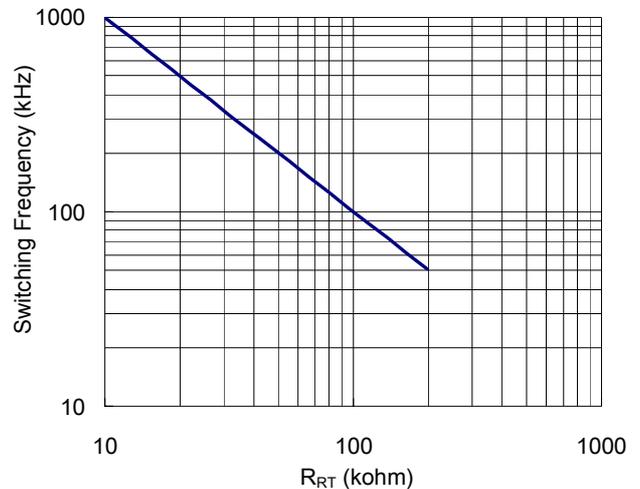
Figure 1. Switching Frequency vs. R_{RT}.

When released, the RT/EN pin voltage is regulated at 1V. Pulling the RT/EN pin to ground shuts down the uP6210.

Voltage Control Loop

Figure 2 shows the simplified voltage control loop of uP6210. VREF is a reference voltage output with 1% accuracy and up to 1mA sourcing capability. RSET is an open drain output that is controlled by VID pin. RSET is pulled to FBRTN when VID = 1 and is set high impedance when VID = 0. Therefore, the reference input voltage at REFIN pin is calculated as:

$$V_{REFIN} = V_{REF} \times \frac{R2}{R1 + R2} \qquad \text{for VID = 0}$$

$$V_{REFIN} = V_{REF} \times \frac{R2 // R3}{R1 + (R2 // R3)} \qquad \text{for VID = 1}$$

Users can control VID pin to get two reference voltage level.

The current-limited buffer receives input at the VREFIN pin and output a voltage source at SS pin. The output capability of the buffer is limited to 20uA during soft start and 200uA after soft start end. A capacitor C_{SS} connected from SS to FBRTN sets the voltage slew rate.

$$\frac{dV_{SS}}{dt} = \frac{C_{SS}}{I_{SS}} = \frac{C_{SS}}{20uA} \qquad \text{during soft start.}$$

$$\frac{dV_{SS}}{dt} = \frac{C_{SS}}{I_{SS}} = \frac{C_{SS}}{200uA} \qquad \text{after soft startend.}$$

These slew rate are used to control the output voltage slew at soft start and V_{REFIN} jumping respectively.
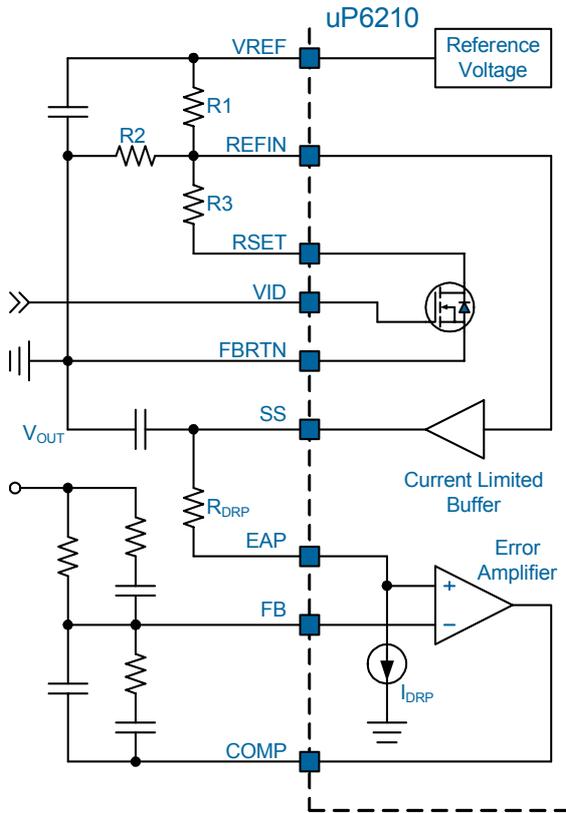
Figure 2. Voltage Control Loop

The FB voltage is tightly regulated to the positive input of the error amplifier, EAP. The output current is sensed and mirrored to the EAP pin, resulting in a voltage droop between SS and EAP.

$$V_{EAP} = V_{SS} - R_{DRP} \times I_{DRP}$$

where I_{DRP} is a current signal proportional to output current. Consequently, at steady state, the output voltage can be expressed as:

$$V_{OUT} = V_{REF} \times \frac{R2}{R1+R2} - R_{DRP} \times I_{DRP} \qquad \text{for VID = 0}$$

$$V_{OUT} = V_{REF} \times \frac{R2//R3}{R1+(R2//R3)} - R_{DRP} \times I_{DRP} \quad \text{for VID = 1}$$

Soft Start

The uP6210 initiates its soft start cycle when the RT/EN pin released from ground once the the POR is granted as shown in Figure 3.
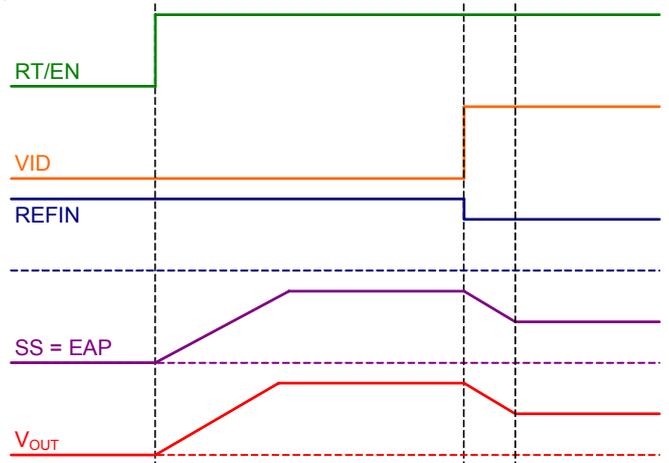

Figure 3. Soft Start Cycle, $R_{DRP} = 0\Omega$

As mentioned in the above section, slew rate of voltage transition at SS and output voltage during soft start and V_{REFIN} jumping is controlled by the capacitor connected to the SS pin. This reduces inrush current to charge/discharge the large output capacitors during soft start and VID changing. and prevents OCP, OVP/UVP false trigger.

The SS buffer sinking/sourcing capability is limited to 20uA during soft start and 200uA after soft start end. Therefore, the slew rate of voltage ramping up/down at SS, EAP and FB pin during soft start or VID changing is calculated as:

$$\frac{dV_{SS}}{dt} = \frac{dV_{EAP}}{dt} = \frac{dV_{FB}}{dt} = \frac{20uA}{C_{SS}} \qquad \text{during soft start.}$$

$$\frac{dV_{SS}}{dt} = \frac{dV_{EAP}}{dt} = \frac{dV_{FB}}{dt} = \frac{200uA}{C_{SS}} \qquad \text{after soft start.}$$

The uP6210 features pre-bias start-up capability. If the output voltage is pre-biased with a voltage, say V_{BIAS}, that accordingly makes V_{FB} higher than reference voltage ramping V_{EAP}. The error amplifier keeps V_{COMP} lower than the valley of the sawtooth waveform and makes PWM comparators output low until the ramping V_{EAP} catches up the feedback voltage. The uP6210 keeps both upper and lower MOSFETs off until the first pulse takes place.

Output Current Sensing

Figure 4 illustrates the output current sensing block of the uP6210. The voltage V_{CS} across the current sensing capacitor C_{CS} can be expressed as:

$$V_{CS} = I_{OUT} \times R_{DC} / 2$$

if the following condition is true.

$2 \times L / R_{DC} = R_{CSP} \times C_{CS}$

where L is the output inductor of the buck converter, R_{DC} is the parasitic resistance of the inductor, R_{CSP} and C_{CS} are the external RC network for current sensing.

The GM amplifier will source a current I_{CSN} to the CSN pin to let its inputs virtually short circuit.

$I_{CSN} \times R_{CSN} = V_{CS}$

Therefore the output current signal I_{CSN} can be expressed as:

$$I_{CSN} = \frac{I_{OUT} \times R_{DC}}{2 \times R_{CSN}}$$

The output current signal I_{CSN} is used as droop tuning, automatic phase reductin, and output over current protection. Please see the related section for details.
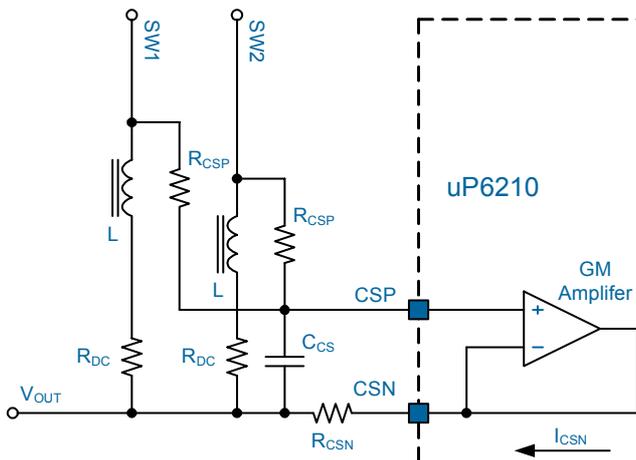

Figure 4. Output Current Sensing of uP6210.

The sourcing capability of the GM amplifier is 100uA. It is recommended to scale *I_{AVG} = 30uA* at rated output current and set the OCP current as twice the rated output current. Take a 60A converter for example. Assume $R_{DC} = 2m\Omega$, select the sense resistor according to

$$R_{CSN} = \frac{60A \times 2m\Omega}{2 \times 30uA} = 2k\Omega$$

Over Current Protection

The sensed current signals are monitored for over current protection. If I_{CSN} is higher than 60uA, the over current protection OCP is activated. Take the above case for example, the OCP level is calculated as:

$$I_{OCP} = \frac{2 \times 60uA \times 2k\Omega}{2m\Omega} = 120A$$

The OCP is of latch-off type and can be reset by toggling

RT/EN or VCC POR.

Figure 5, and Figure 6 illustrate the OCP behaviors during soft start and after soft start end respectively.

Current Balance

The uP6210 extracts phase currents for current balance by parasitic on-resistance of the lower switches when turned on as shown in Figure 5.
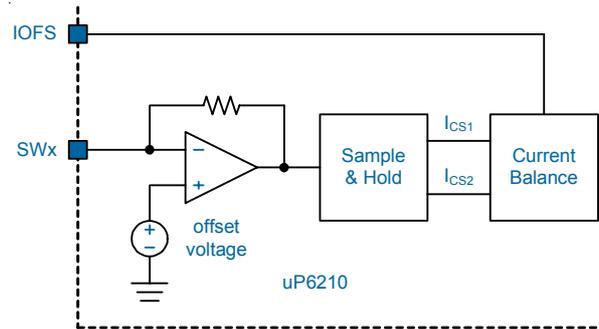

Figure 5. $R_{DS(ON)}$ Current Sensing Scheme

The GM amplifier senses the voltage drop across the lower switch and converts it into current signal each time it turns on. The sampled and held current is expressed as:

$$I_{CSX} = I_{LX} \times R_{DS(ON)} \times 10^{-3} + 6.6uA$$

where I_{LX} is the phase X current in Ampere, $R_{DS(ON)}$ is the on-resistance of low side MOSFET in Ω, 6.6uA is a constant to compensate the offset voltage of the current sensing circuit.

The uP6210 fine tunes the duty cycle of each channel for current balance according to the sensed inductor current signals as shown in Figure 6. If the current of channel 1 is smaller than the current of channel 2, the uP6210 increases the duty cycle of the corresponding phase to increase its phase current accordingly, vice verse.
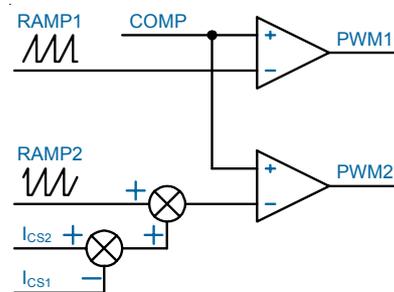

Figure 6. Current Balance Scheme of uP6210.

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Functional Description

Offset Current Tuning

The uP6210 features an IOFS pin for tuning the offset current between phase. The IOFS pin voltage is nominal 0.5V when connecting a resistor to GND and 1.5V when connecting a resistor to VREF. Connecting a resistor from IOFS pin to GND generate a current source as:

$$I_{OFS} = 0.5V / R_{OFS}$$

This current is add to phase 1 current signal I_{CS1} for current balance. Consequently, phase 2 will share more percentage of output current.

Connecting a resistor from IOFS pin to VREF generates a current source as:

$$I_{OFS} = (2V - 1.5V) / R_{OFS}$$

This current is add to phase 2 current signal I_{CS2} for current balance. Consequently, phase 1 will share more percentage of output current.

Automatic Phase Reduction

The uP6210 features automatic phase reduction that turns off phase 2 at light load condtion and reduces both switching and conduction losses. The automatic phase reduction maintains high power conversion efficiency over the output current range.

The output current is sensed and mirrored to PSI pin as:

$$I_{PSI} = I_{CSN} = \frac{I_{OUT} \times R_{DC}}{2 \times R_{CSN}}$$

The I_{PSI} creates a voltage V_{PSI} as:

$$V_{PSI} = R_{PSI} \times I_{PSI} = \frac{I_{OUT} \times DCR \times R_{PSI}}{2 \times R_{CSN}}$$

The uP6210 operates in dual phase if V_{PSI} is higher than 0.6V and in single phase if V_{PSI} is lower than 0.4V. There is a 200mV hystersis at the phase change threshold. There is a 1ms delay when entering single phase operation and no time delay when entering dual phase operation. When operating single phase, both HG2 and LG2 are turned off.

Take the about case for example, with R_{PSI} = 80kΩ, the threshold level of output current for entering single phase operation is calculated as:

$$0.4V = \frac{I_{OUT} \times DCR \times R_{PSI}}{2 \times R_{CSN}}$$

$$I_{OUT} = \frac{0.4V \times 2 \times 2k\Omega}{2m\Omega \times 80k\Omega}$$

$$I_{OUT} = 10A$$

The threshold level of output current for entering dual phase operation is calculated as:

$$0.6V = \frac{I_{OUT} \times DCR \times R_{PSI}}{2 \times R_{CSN}}$$

$$I_{OUT} = \frac{0.6V \times 2 \times 2k\Omega}{2m\Omega \times 80k\Omega}$$

$$I_{OUT} = 15A$$

Note that when operated in single phase, the rated current is reduced to **80 percents** of normal level. Continuous demanding high current may damage the converter.

Connect PSI pin to VREF to disable the automatic phase reduction function. Since the VREF has no sinking capability, make sure the external loading is higher than 100uA when connecting PSI pin to VREF. Otherwise, VREF may loss its regulation.

Over Voltage and Under Voltage Protection

The FB voltage is continuously monitored for over voltage and under voltage protection. The uP6210 asserts over voltage protection if $V_{FB} > V_{SS} + 300mV$ and turns on the lower MOSFETs and shuts down the converter. The uP6210 asserts under voltage protection if $V_{FB} < V_{SS} - 300mV$ and shuts down the converter. The UVP function is disabled during soft start.

Both UVP and OVP are latch-off type and can be reset only by toggling the RT/EN pin ro by VCC power on reset.

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Absolute Maximum Rating

Supply Input Voltage, VCC (Note 1) --- -0.3V to +15V
SW to GND
    DC --- -0.3V to 15V
    < 200ns -- -5V to 30V
BOOT to SW --- 15V
BOOT to GND
    DC --- -0.3V to PHASE +15V
    < 200ns -- -0.3V to 42V
Input, Output or I/O Voltage --- -0.3V to +6V
Storage Temperature Range -- -65°C to +150°C
Junction Temperature -- 150°C
Lead Temperature (Soldering, 10 sec) -- 260°C
ESD Rating (Note 2)
    HBM (Human Body Mode) --- 2kV
    MM (Machine Mode) --- 200V

Thermal Information

Package Thermal Resistance (Note 3)
    VQFN4x4-24L θ_{JA} --- 40°C/W
Power Dissipation, P_D @ T_A = 25°C
    VQFN4x4-24L --- 2.5W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) -- -40°C to +125°C
Operating Ambient Temperature Range --- -40°C to +85°C
Supply Input Voltage, V_{CC} --- 10.8V to 13.2V

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Voltage	V_{CC12}		4.5	--	13.2	V
Supply Current	I_{CC}	HG and LG Open; V_{CC} = 12V, Switching	--	5	--	mA
Quiescent Supply Current	I_{CC_Q}	No Switching, I_{PCC} = 0mA	--	4	--	mA
Regulated Supply Voltage	V_{PCC}	RT/EN = 0V, I_{PCC} = 0mA	8	9	10	V
POR Threshold	V_{CCRTH}		8	9	10	V
POR Hysteresis	V_{CCHYS}		--	1.0	--	V
Chip Enable/Frequency Setting						
RT/EN Sourcing Current	$I_{RT/EN}$	RT/EN = GND.	100	150	200	uA
RT/EN Voltage	$V_{RT/EN}$	$R_{RT/EN}$ = 33kΩ	--	1	--	V
Switching Frequency Setting Range			50	--	1000	kHz
Free Run Switching Frequency	f_{OSC}	$R_{RT/EN}$ = 33kΩ	270	300	330	kHz
Switching Frequency Accuracy	Δf_{OSC}	f_{OSC} = 200kHz ~ 500kHz	-15	--	15	%

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Soft Start						
Soft Start Current	I_{SS}	During soft start.	--	20	--	uA
Supply Current	I_{CC}	After soft start end.	--	200	--	
Oscillator						
Maximum Duty Cycle			--	85	--	%
Maximum Duty Cycle			--	0	--	%
Ramp Amplitude	ΔV_{OSC}	V_{CC} = 12V.	--	3.5	--	V
Power Saving Mode						
Threshold Voltage for Entering Dual Phase	V_{PSI}	V_{PSI} rising.	0.55	0.6	0.65	V
Hysteresis Voltage for Entering Single Phase	ΔV_{PSI}	V_{PSI} falling.	--	200	--	mV
Reference Voltage						
Reference Voltage Accuracy	V_{REF}	I_{REF} = 100uA	1.98	2.00	2.02	V
Reference Voltage Load Regulation	ΔV_{REF}	I_{REF} = 0 ~ 2mA	-5	--	5	mV
Output Voltage Accuracy	V_{FB}	$|V_{REFIN} - V_{FB}|$, V_{CC} = 12V, No Load, R_{DRP} = 0Ω, V_{REFIN} = 0.8V ~ 1.6V.	--	--	5	mV
Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by design.	70	80	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF, Guaranteed by design.	20	--	--	MHz
Slew Rate	SR	Guaranteed by design.	15	20	--	V/us
Maximum Current (Sink & Source)	I_{COMP}	V_{COMP} = 1.6V	1.5	2.0	--	mA
Total Current Sense						
Maximum Sourcing Current	I_{CSN_MAX}		100	--	--	uA
GM Amplifier Offset			-1	0	1	mV
Over Current Protection Threshold Level	I_{CSN_OCP}		--	60	--	uA
Droop Accuracy		I_{DRP}/I_{CSN}	90	100	110	%
PSI Accuracy		I_{PSI}/I_{CSN}	90	100	110	%
Phase Current Sense						
Trans-conductance			--	1.0	--	mS
IOFS Voltage	V_{OFS}	100kΩ from IOFS to VREF	--	1.5	--	V
		100kΩ from IOFS to GND	--	0.5	--	

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VID Control Input						
Logic High Threshold Level	V_{IL}		1.2	--	--	V
Logic Low Threshold Level	V_{IL}		--	--	0.4	V
On Resistance of RSET MOSFET	R_{RSET}	VID = High	--	20	--	Ω
Leakage of RSET Pin	I_{RSET}	V_{RESET} = 2V, VID = 0V	--	--	0.1	uA
Gate Driver						
Upper Gate Sourcing	R_{HG_SRC}	I_{HG} = 100mA sourcing	--	2	4	Ω
Upper Gate Sinking	R_{HG_SNK}	I_{HG} = 100mA sinking	--	1.5	3	Ω
Lower Gate Source	R_{LG_SRC}	I_{LG} = 100mA sourcing	--	2	4	Ω
Lower Gate Sink	R_{LG_SNK}	I_{LG} = 100mA singking	--	1	2	Ω
Dead Time	T_{DT}		--	30	--	ns
Protection						
Over Voltage Protection		V_{FB} - V_{SS}	--	300	--	mV
Under Voltage Protection		V_{FB} - V_{SS}	--	-300	--	mV
Over Temperature Protection			--	150	--	^{O}C
Over Temperature Hysteresis			--	20	--	^{O}C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

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Power On Waveforms
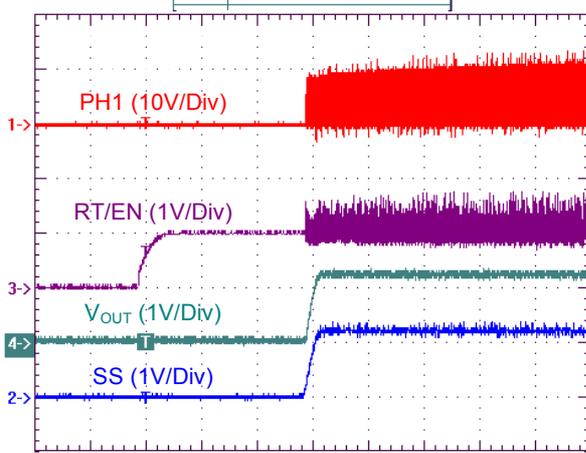
Time (2ms/Div)
V_{IN} = 12V, I_{OUT} = 40A

Power Off Waveforms
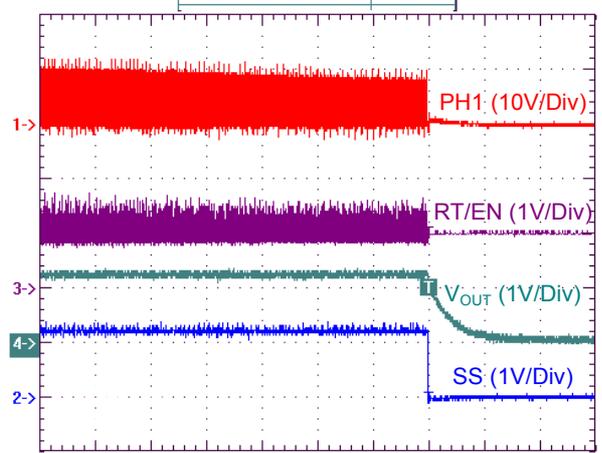
Time (200us/Div)
V_{IN} = 12V, I_{OUT} = 40A

Turn On Waveforms
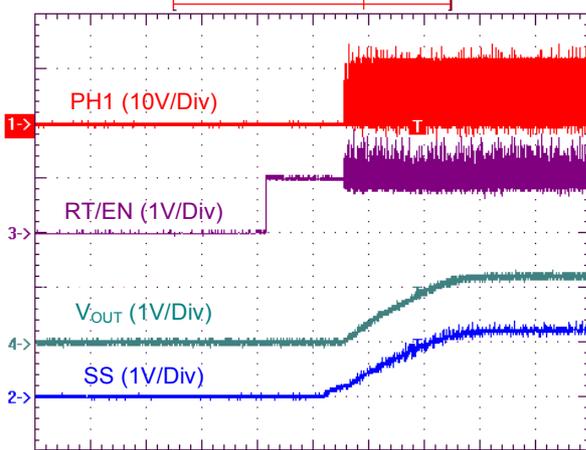
Time (200us/Div)
V_{IN} = 12V, I_{OUT} = 40A

Output Voltage Load Regulation
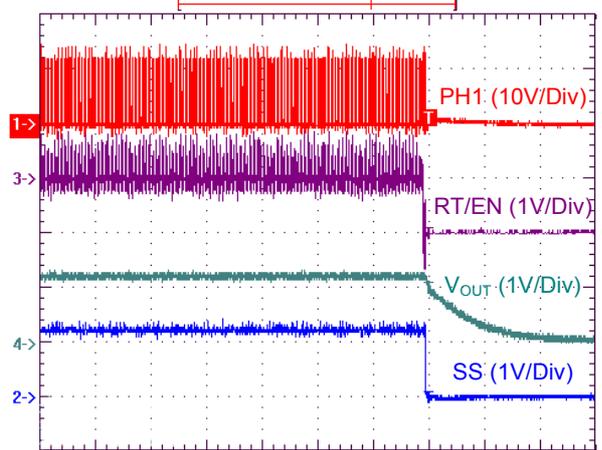
Time (100us/Div)
V_{IN} = 12V, I_{OUT} = 40A

UG1 Falling Waveforms
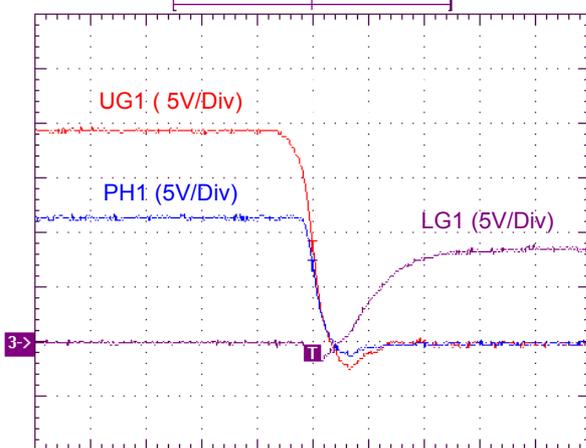
Time (40ns/Div)
V_{IN} = 12V, I_{OUT} = 40A, 20MHz Bandwidth Limited

UG1 Rising Waveforms
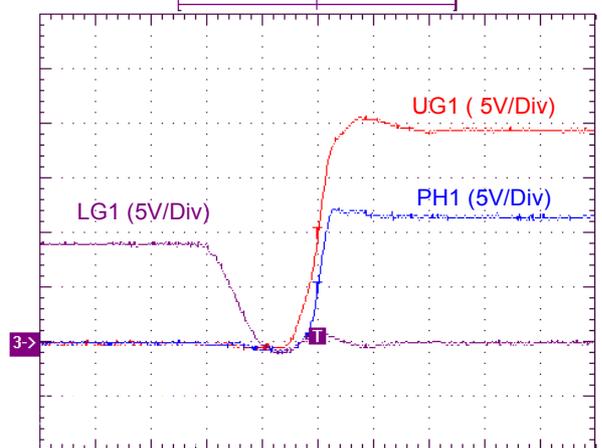
Time (40ns/Div)
V_{IN} = 12V, I_{OUT} = 40A, 20MHz Bandwidth Limited

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Typical Operation Characteristics

Over Voltage Protection

FB (1V/Div)

PH1 (10V/Div)

LG1 (10V/Div)

Time (2us/Div)

Power Off Waveforms

V_OUT (1V/Div)

PSI (1V/Div)

PH1 (10V/Div)

PH2 (10V/Div)

Time (20us/Div)

Turn On Waveforms

PSI (1V/Div)

PH1 (10V/Div)

PH2 (10V/Div)

Time (2ms/Div)
V_{IN} = 12V, I_{OUT} = 0A to 40A
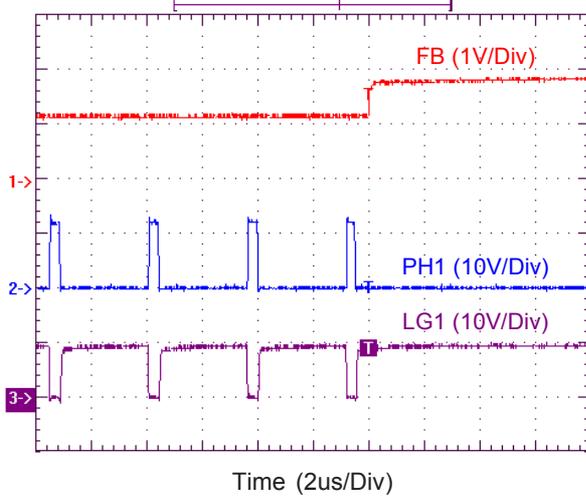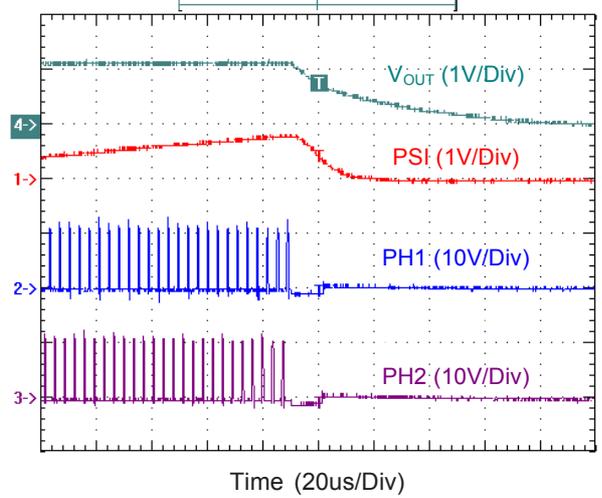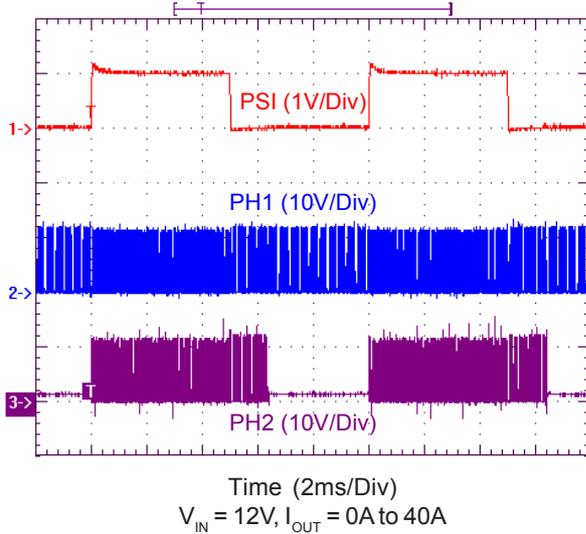
VCC9 Line Regulation
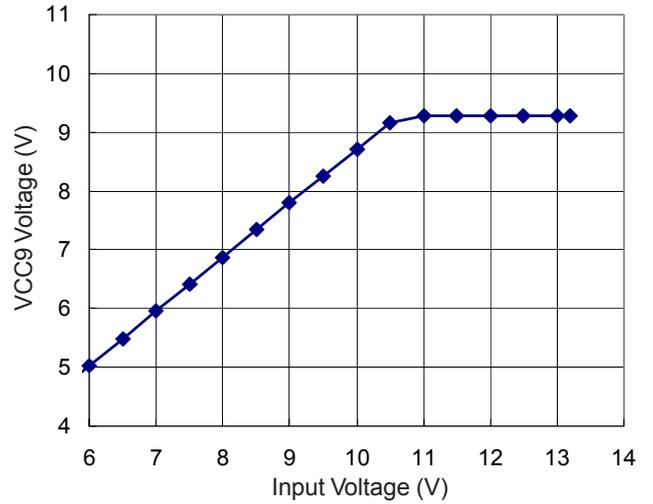
VREF Load Regulation

VREF Line Regulation

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POWER INTELLECT

Typical Operation Characteristics

Frequency vs. RT

Efficiency vs. Output Current with Auto PSI

VCC9 Voltage vs. Tempereture

VREF Voltage vs. Temperature

Switching Frequency vs. Tempereture
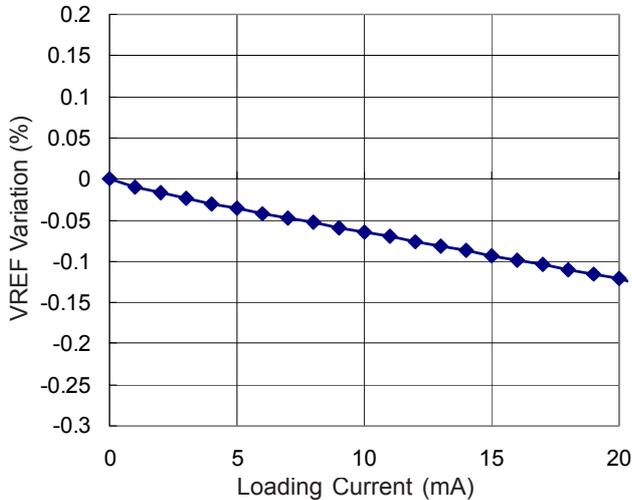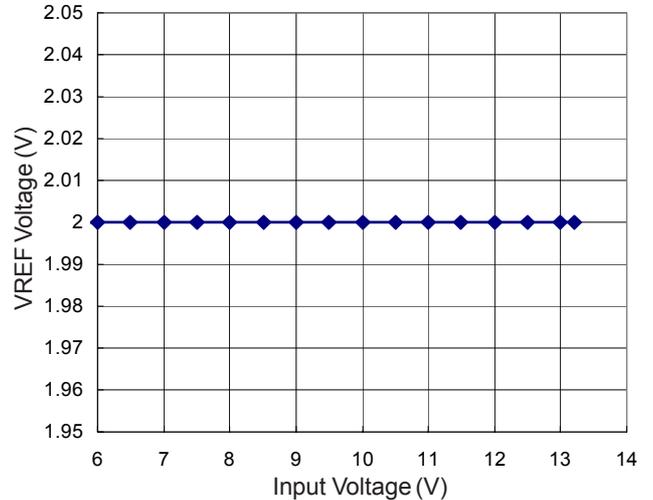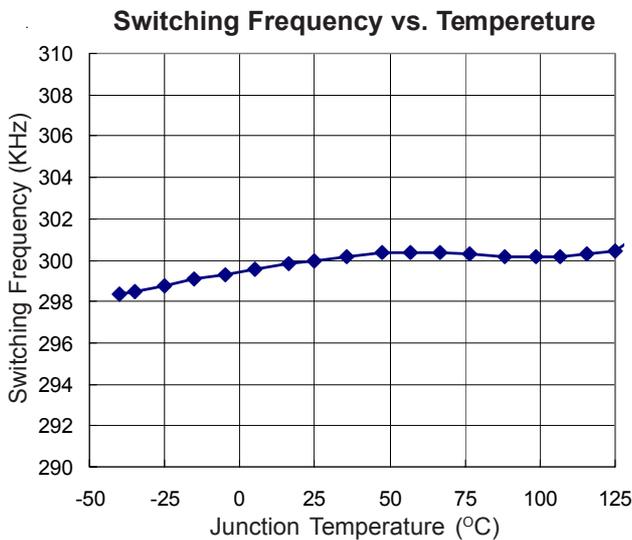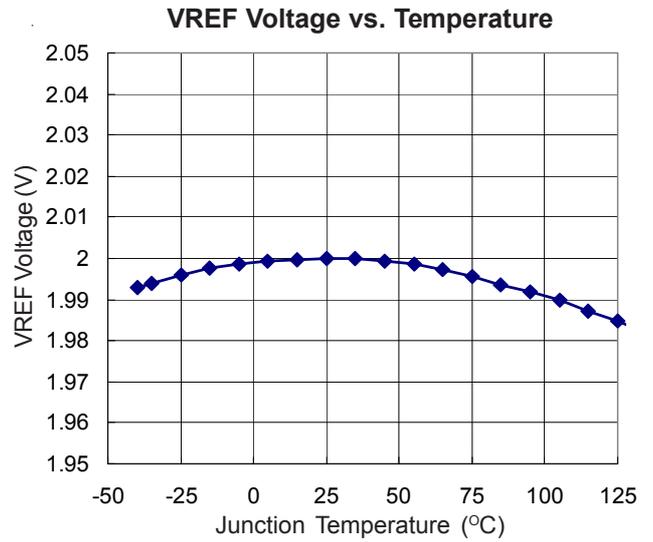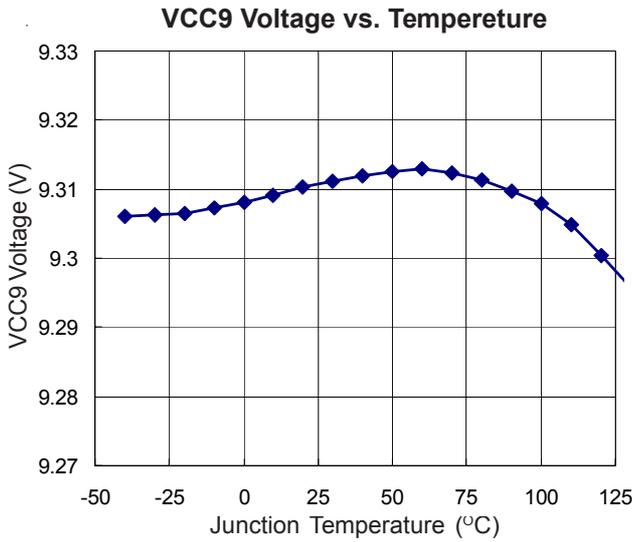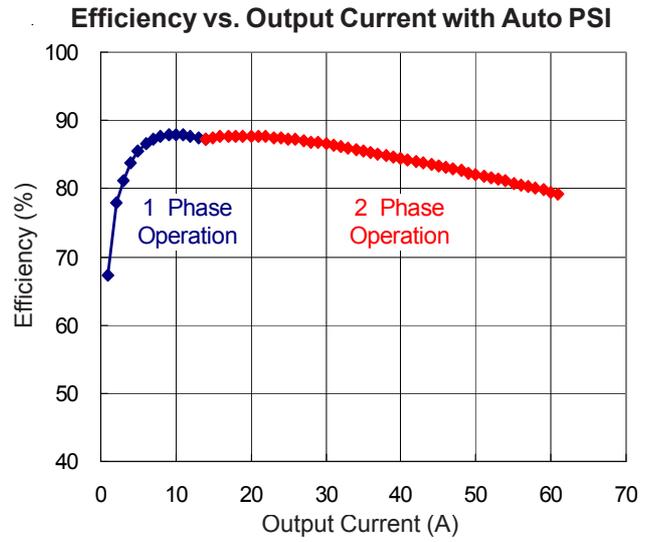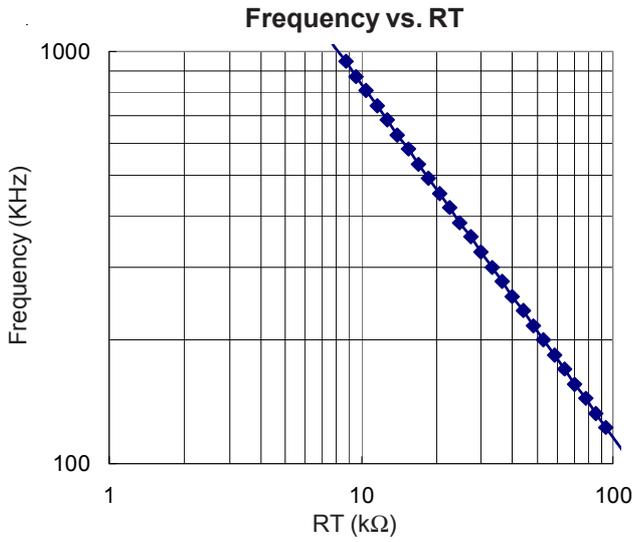
FBRTN Configuration

Since the reference voltage V_{REF} is measured with respective to FBRTN, connect circuits related to VREF, REFIN, and SS pin to FBRTN locally with short traces as shown in the *Typical Application Circuit*.

Total Current Sensing

In the real application, PCB trances are not ideal and have certain parasitic resistances R_{PCB1} and R_{PCB2} as shown in Figure 1. When these parasistic resistances are not identical, the voltages at inductor terminals are not the same, contributing meausrement error on total current sensing. Two 1Ω resistors, connecting directly to inductor terminals are recommended to elimiate the effects of parasitic resistance.

A 0.1uF capacitor C_{BYP} is also recommended to bypassing noise when the uP6210 is far away from the output inductors. Place the C_{BYP} physically near the IC.
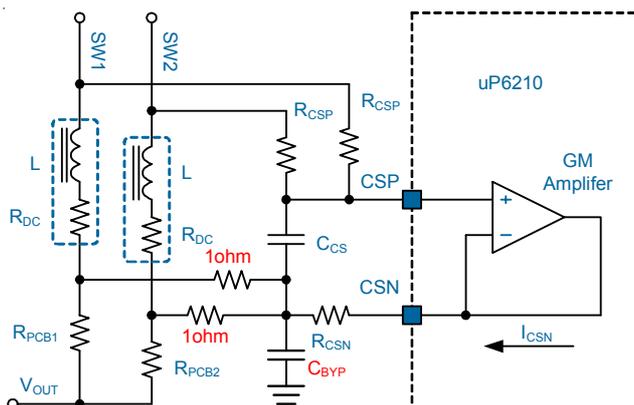

Figure 1. Parasitic Resistance of PCB

Pin 1 mark
(Note 6)

Bottom View - Exposed Pad

Recommended Solder Pad Pitch and Dimensions
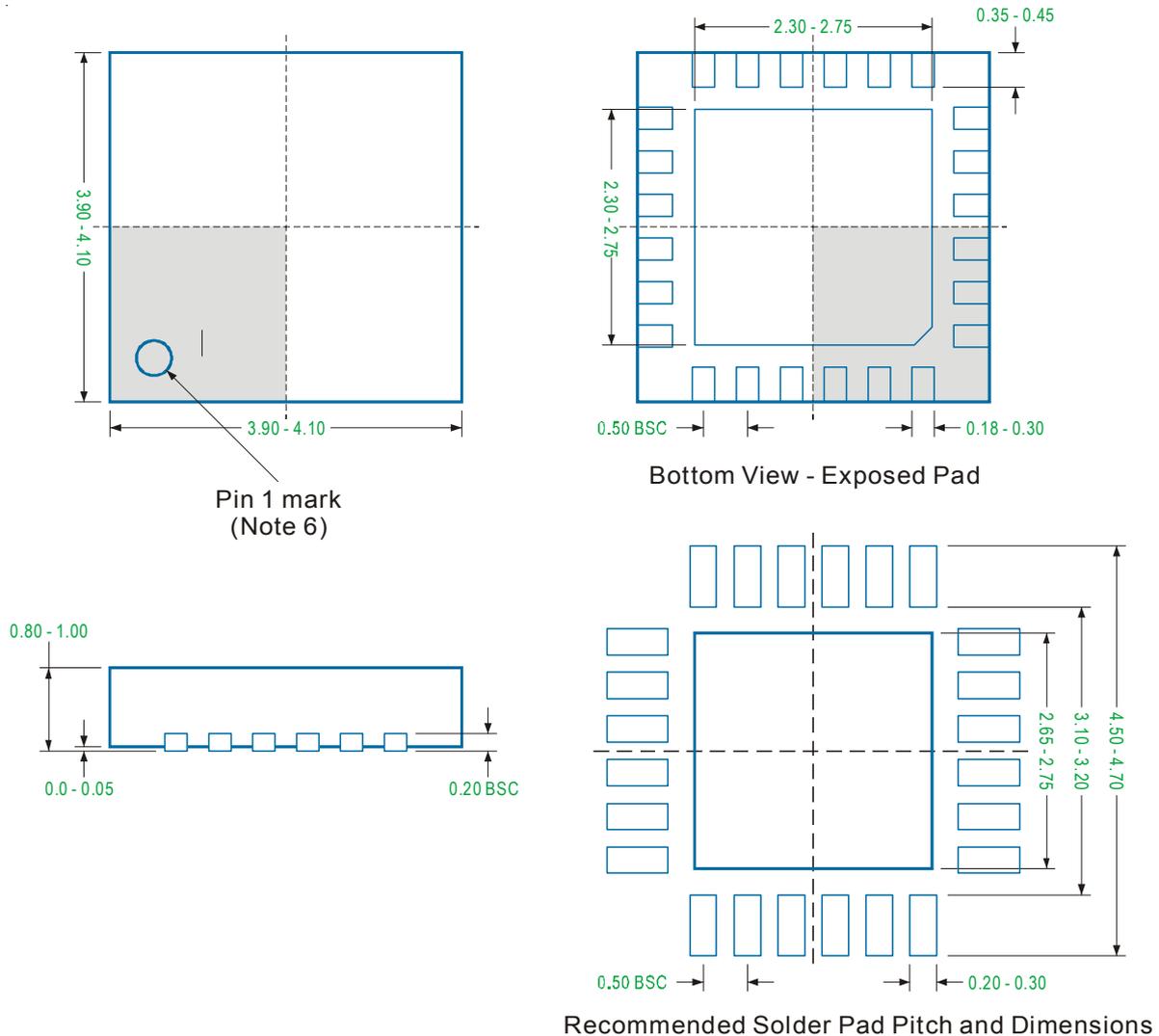
Note

1. Package Outline Unit Description:

   BSC: Basic. Represents theoretical exact dimension or dimension target

   MIN: Minimum dimension specified.

   MAX: Maximum dimension specified.

   REF: Reference. Represents dimension for reference use only. This value is not a device specification.

   TYP. Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

3. Drawing not to scale.

4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.