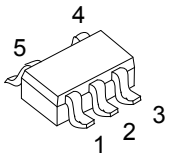
500mA HIGH PSRR LDO REGULATORS



SOT-25

■ DESCRIPTION

The UTC **L1923** is a low supply current, low dropout linear regulator. It is operating at 2.5V - 5.5V. The supply current is as low as 55μA in the no–load condition. In the shutdown mode, the maximum supply current is less than 1μA.

A built-in over-temperature protection circuit is designed to protect the device from being damaged by thermal overload. The over-current protection limit is set at 800mA (TYP.)

The UTC **L1923** can be operated on the following two modes. When the SET pin is connected to ground, the output of **L1923** is a pre-set value and the external components are not needed to decide the output voltage. When an output other than the preset value is needed, two external resistors should be used as voltage dividers and then the output voltage is decided by the resistor ratio.

The UTC **L1923** is generally used in notebook computers, cellular phones, PDAs, digital still camera and video recorders and other hand-held devices.

■ FEATURES

* Low No-Load Supply Current: 90μA
* Guaranteed 500mA Output Current
* Dropout Voltage is 200mV @ 250mA Load
*OTP(Over-Temperature Protection) and Short-Circuit Protection
* Two Modes Of Operation:
Fixed Mode：3.3V，3.5V，3.9V
Adjustable Mode: 1.25V - 5.5V
* Maximum Supply Current In Shutdown Mode is Less than 1μA
* Low Output Noise at 238μVRMS
* Stability with Lost Cost Ceramic Capacitors

■ ORDERING INFORMATION

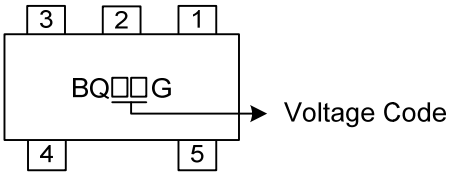
Ordering Number	Package	Packing
L1923G-xx-AF5-R	SOT-25	Tape Reel

Note: xx: Output Voltage, refer to Marking Information.

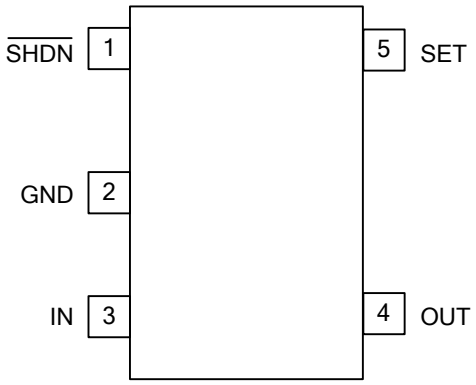
L1923G-xx-AF5-R
(1)Packing Type
(2)Package Type
(3)Output Voltage Code
(4)Halogen Free

(1) R: Tape Reel
(2) AF5: SOT-25
(3) xx: Refer to Marking Information
(4) G: Halogen Free

■ MARKING INFORMATION

PACKAGE	VOLTAGE CODE	MARKING
SOT-25	33:3.3V 35:3.5V 39:3.9V	

■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	$\overline{\text{SHDN}}$	Active-Low Shutdown Input. A logic low reduces the supply current to less than 1μA. Connect to IN for normal operation.
2	GND	Ground. This pin also functions as a heatsink. Solder to large pads or the circuit board ground plane to maximize thermal dissipation.
3	IN	Regulator Input. Supply voltage can range from +2.5V to +5.5V. Bypass with 1μF to GND
4	OUT	Regulator Output. Fixed or adjustable from 1.25V to +5.5V. Sources up to 500mA. Bypass with a 4.7μF, ＜0.2Ω typical ESR capacitor to GND.
5	SET	Feedback Input for Setting the Output Voltage. Connect to GND to set the output voltage to the preset output voltage. Connect to an external resistor divider for adjustable-output operation.

■ BLOCK DIAGRAM

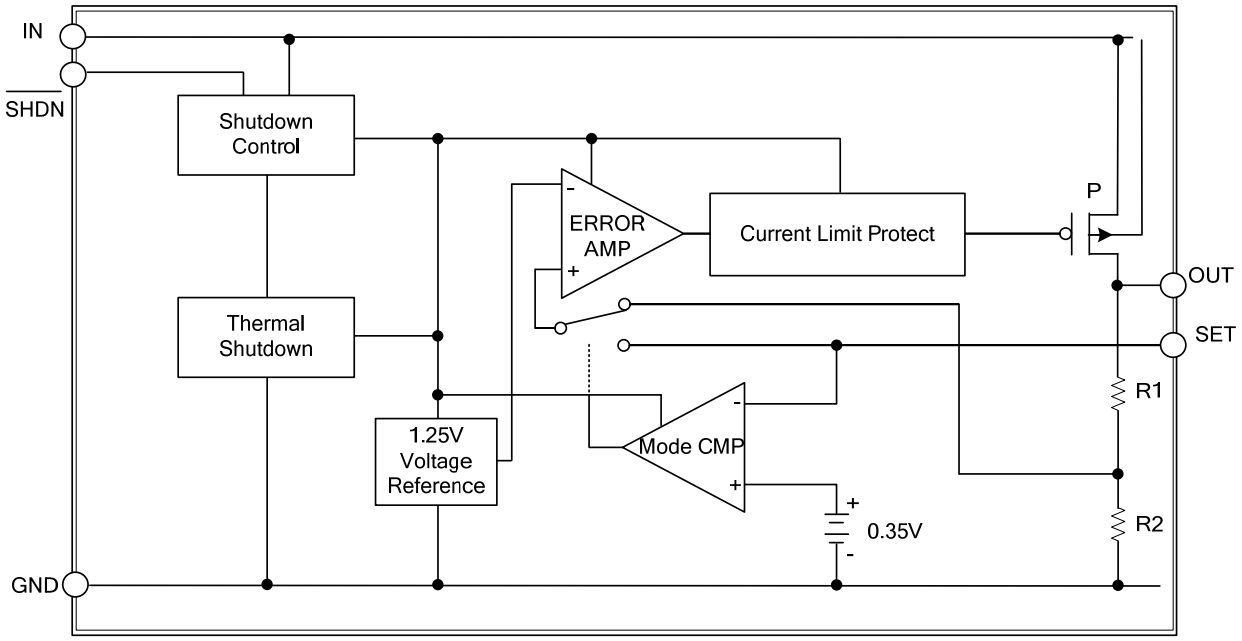


Figure 1. Functional Diagram

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
V_{IN} to GND		-0.3~7	V
Output Short-Circuit Duration		Infinite	
SET to GND		-0.3~7	V
$\overline{SHDN}$ to GND		-0.3~7	V
$\overline{SHDN}$ to IN		-7~0.3	V
OUT to GND		-0.3~(V_{IN}+0.3)	V
Continuous Power Dissipation (T_A=25°C)	P_D	520	mW
Junction Temperature	T_J	150	°C
Operating Temperature	T_{OPR}	-40~85	°C
Storage Temperature	T_{STG}	-65~160	°C

Notes: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	240	°C/W

■ ELECTRICAL CHARACTERISTICS

(V_{IN} =+3.6V, $V_{\overline{SHDN}}$ =V_{IN}, T_A =T_J =+25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Voltage (Note 2)	V_{IN}			2.5		5.5	V
Output Voltage Accuracy	V_{OUT}	Variation from specified V_{OUT}, I_{OUT}=1mA		-2		2	%
Adjustable Output Voltage Range (Note 3)	V_{OUT}			V_{SET}		5.5	V
Maximum Output Current				500			mA
Current Limit (Note 4)	I_{LIMIT}			600	800		mA
Short Circuit Current	Isc				120		mA
Ground Pin Current	I_Q				90	120	μA
Dropout Voltage (Note 5)	V_{DROP}	I_{OUT}=250mA			200		mV
		I_{OUT}=500mA			400	500	
Line Regulation	ΔV_{LNR}	SET=GND, V_{IN}=$V_{(STD)}$+0.1V ~ 5.5V , I_{OUT}=10mA			0.06	0.12	%/V
Load Regulation	ΔV_{LDR}	I_{OUT}= 10mA ~500mA			0.02	0.1	%/mA
Ripple Rejection	PSRR	F=100Hz, 0.45V_{P-P}, I_{OUT}=10mA			65		dB
Output Noise	Noise	F≤100kHz, I_{OUT} =0A			136		μV (RMS)
		F≤100kHz, I_{OUT} =250mA			238		
		F≤100kHz, I_{OUT} =500mA			253		
SHUTDOWN							
SHDN Input Threshold	V_{IH}	Regulator enabled		1.5			V
	V_{IL}	Regulator shutdown				0.4	
$\overline{SHDN}$ Input Bias Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$= V_{IN}	T_A= +25°C		0.003	0.1	μA
Shutdown Supply Current	I_{QSHDN}	V_{OUT}= 0V	T_A= +25°C		0.2	1	μA
SET INPUT							
SET Reference Voltage (Note 3)	V_{SET}	V_{IN}= 2.5V ~ 5.5V, I_{OUT}= 1mA	T_A= +25°C	1.225	1.25	1.275	V
			T_A= T_{MIN} to T_{MAX}		1.25		
SET Input Leakage Current (Note 3)	I_{SET}	V_{SET}= 1.3V	T_A= +25°C		5	30	nA
THERMAL PROTECTION							
Thermal Shutdown Temperature	T_{SHDN}				145		°C
Thermal Shutdown Hysteresis	ΔT_{SHDN}				25		°C

Notes: 1.Limits is 100% production tested at T_A= +25°C. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2.Guaranteed by line regulation test.
3.Adjustable mode only.
4.Not tested. For design purposes, the current limit should be considered 600mA minimum to 800mA maximum.
5.The dropout voltage is defined as (V_{IN}-V_{OUT}) when V_{OUT} is 100mV below the target value of V_{OUT}.

■ APPLICATION INFORMATION

The UTC **L1923** contains an error amplifier, 1.25V bandgap reference, PMOS output transistor, internal feedback voltage divider, mode comparator, shutdown logic, over current protection circuit, and over temperature protection circuit as shown in the block diagram.

The process of operation is like this: the mode comparator compares the voltage of SET pin with a pre-set voltage reference of 0.35V. If the voltage of SET pin is smaller than 0.35V, the internal feedback voltage divider's central tap is connected to the error amplifier's non-inverting input. Then, the error amplifier compares non-inverting input with the 1.25V bandgap voltage reference. If the feedback voltage is larger than the voltage reference 1.25V, the error amplifier's output becomes higher. This makes the PMOS output transistor's V_{GS} (gate-to-source voltage) smaller, in that condition, the current carrying capability of the PMOS output transistor is reduced, as a result the output voltage decreases until the feedback voltage becomes equal to 1.25V. Similarly, when the feedback voltage is less than 1.25V, the error amplifier causes the output PMOS to conductor more current to pull the feedback voltage up to 1.25V. Thus, through this feedback action, the error amplifier, output PMOS, and the voltage dividers effectively form a unity-gain amplifier with the feedback voltage force to be the same as the 1.25V bandgap reference.

The output voltage, V_{OUT}, can be calculated as follows:

$$V_{OUT} = 1.25\ (1 + R1/R2). \qquad (1)$$

Alternatively, the relationship between R1 and R2 is expressed in the following:

$$R1 = R2\ (V_{OUT}/1.25 - 1). \qquad (2)$$

In order to reduce power dissipation and loop stability, it is recommended that R2 is 100KΩ. For UTC **L1923-330**, R1 is 164K, and the pre-set V_{OUT} is 3.30V.

In Figure 2, the SET pin voltage will be larger than 350mV when external voltage divider functions in the operation. The non-inverting input of the amplifier will be connected to the external voltage divider. The conditions of equations 1 and 2 are still true since the operation of the feedback loop is the same. Equation 1 still presents the output voltage.

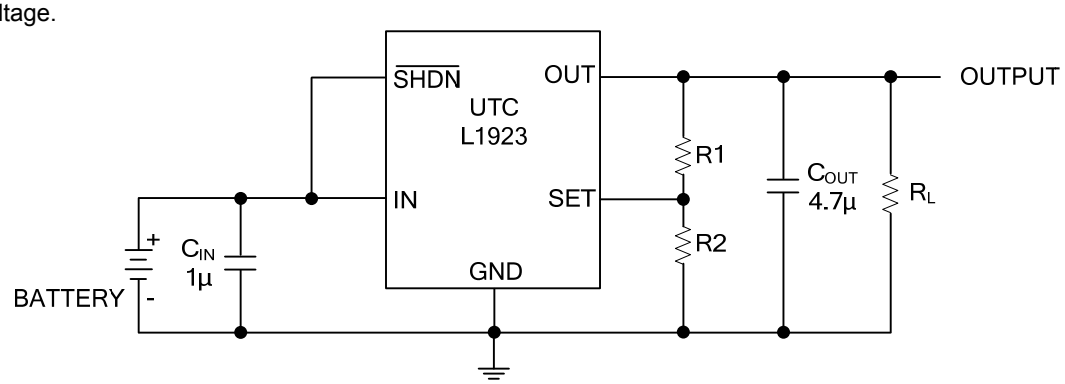


Figure 2. Adjustable Output Using External Feedback Resistors

Over Current Protection

To monitor the output current, the UTC **L1923** applies a current mirror. A portion of the PMOS output transistor's current is mirrored to a resistor such that the voltage across this resistor is proportional to the output current. Once the output current exceeds limit threshold, UTC **L1923** would be protected with a limited output current. Further more, when the output is short to ground, the output current would be folded-back to a less limit.

Over Temperature Protection

Over-temperature protection circuit is designed to prevent this device from being damaged due to abnormal temperature during operation. It is used to turn off the output MOSFET if the temperature is higher than 145°C, the switch does not turn on until the temperature drops to 120°C.

Shutdown Mode

The UTC **L1923** enters shutdown mode if the $\overline{SHDN}$ pin is applied to a logic low voltage. Under the shutdown state, all the analog circuits are turned off completely, which reduces the current consumption to only the leakage current. The UTC **L1923** output pass transistor would get into high impedance level. There is an internal discharge path to help to shorten discharge delay time.

■ APPLICATION INFORMATION (Cont.)

Operating Region and Power Dissipation

The UTC **L1923** is a linear regulator, so the power dissipation can be expressed by: $P = I_{OUT} (V_{IN} – V_{OUT})$. And the maximum power dissipation is calculated by:

$P_{D(MAX)} = (T_J–T_A)/\theta_{JA}$,=(150°C -25°C)/240°C/W= 520mW

(Where $(T_J–T_A)$ is the temperature difference the die and the ambient air; θ_{JA}, is the thermal resistance of the chosen package to the ambient air.)

For surface mount device, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. The die attachment area of the UTC **L1923**'s lead frame is connected to pin 2, which is the GND pin. Therefore, the GND pin of UTC **L1923** can carry away the heat of the UTC **L1923** die very effectively. Connecting the GND pin to ground using a large ground plane near the GND pin can improve the power consumption.

Capacitor Selection and Regulator Stability

A 1μF capacitor on the input and a 4.7μF capacitor on the output are recommended for most applications of the U TC **L1923**. To get a better supply-noise rejection and transient response, input capacitors with larger values and lower ESR are needed. A higher-value input capacitor (10μF) may be necessary if large, fast transients are anticipated and the device is located several inches from the power source.

Power-Supply Rejection and Operation from Sources Other than Batteries

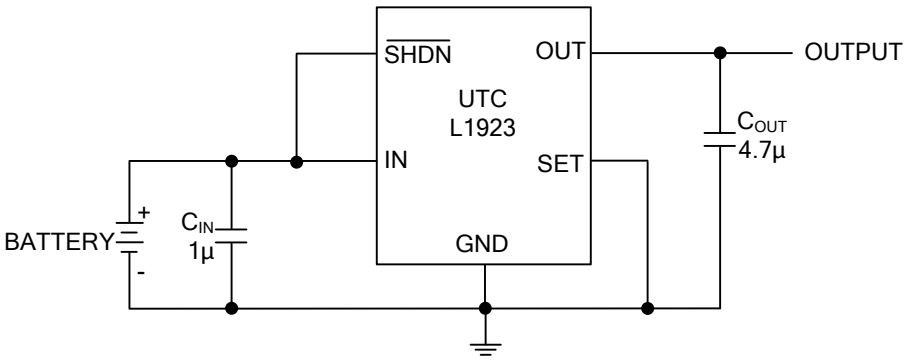
The UTC **L1923** is particularly designed to deliver low dropout voltages and low quiescent currents in battery-powered systems. Power-supply rejection is 42dB at low frequencies. As the frequency increases above 20kHz, the output capacitor is the major contributor to the rejection of power-supply noise.

When operating from sources other than batteries, improve supply-noise rejection and transient response by increasing the values of the input and output capacitors, and using passive filtering techniques.

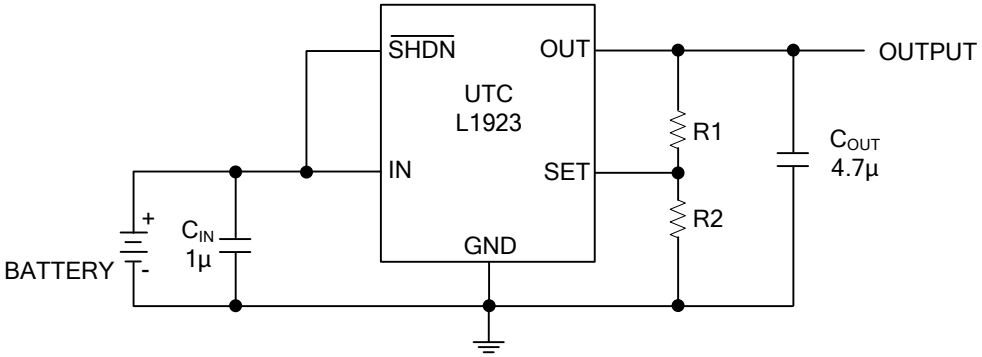
Input-Output (Dropout) Voltage

The minimum input-output voltage differential (or dropout voltage) of a regulator determines the lowest usable supply voltage. In battery-powered system applications, this will determine the useful end-of-life battery voltage. Because the UTC **L1923** use a P-channel MOSFET pass transistor, their dropout voltage is a function of $R_{DS(ON)}$ multiplied by the load current.

■ TYPICAL APPLICATION CIRCUIT



Fixed Mode



Adjustable Mode