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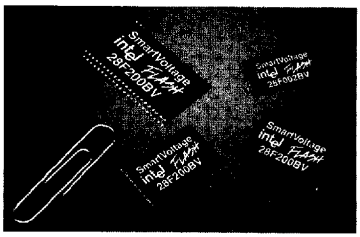
PRODUCT PREVIEW

2-MBIT (128K x 16, 256K x 8) SmartVoltage BOOT BLOCK FLASH MEMORY FAMILY

28F200BV-T/B, 28F002BV-T/B, 28F200CV-T/B

- **Intel SmartVoltage Technology**
  - 5V or 12V Program/Erase
  - 3.3V or 5V Read Operation
  - 60% Faster Typical Programming at 12V V_{PP}
- **Very High Performance Read**
  - 5V: 60/80/120 ns Max. Access Time, 30/40 ns Max. Output Enable
  - 3V: 110/150 /180 ns Max. Access Time 65/90 ns Max. Output Enable
- **Low Power Consumption**
  - Maximum 60 mA Read Current at 5V
  - Maximum 30 mA Read Current at 3V
- **x8/x16-Selectable Input/Output Bus**
  - 28F200 for High Performance 16- or 32-bit CPUs
- **x8-Only Input/Output Architecture**
  - 28F002 for Space-Constrained 8-bit Applications
- **Optimized Array Blocking Architecture**
  - One 16-KB Protected Boot Block
  - Two 8-KB Parameter Blocks
  - One 96-KB Main Block
  - One 128-KB Main Blocks
  - Top or Bottom Boot Locations
- **Absolute Hardware-Protection for Boot Block**
- **Software EEPROM Emulation with Parameter Blocks**
- **Extended Temperature Operation**
  - −40°C to +85°C
- **Extended Cycling Capability**
  - 100,000 Block Erase Cycles (Commercial Temperature)
  - 10,000 Block Erase Cycles (Extended Temperature)
- **Automated Word/Byte Write and Block Erase**
  - Industry Standard Command User Interface
  - Status Registers
  - Erase Suspend Capability
- **SRAM-Compatible Write Interface**
- **Automatic Power Savings Feature**
  - 1 mA Typical I_{CC} Active Current in Static Operation
- **Reset/Deep Power-Down Input**
  - 0.2 μA I_{CC} Typical
  - Provides Reset for Boot Operations
- **Hardware Data Protection Feature**
  - Erase/Write Lockout during Power Transitions
- **Industry-Standard Surface Mount Packaging**
  - 40-Lead TSOP
  - 44-Lead PSOP: JEDEC ROM Compatible
  - 48-Lead TSOP
  - 56-Lead TSOP
- **Footprint Upgradable to 4 or 8 Mbit**
- **ETOX™ IV Flash Technology**



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2-MBIT (128K x 16, 256K x 8) SmartVoltage BOOT BLOCK FLASH MEMORY FAMILY

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1.0 PRODUCT FAMILY OVERVIEW

This datasheet comprises the specifications for the SmartVoltage products in the 2-Mbit boot block flash memory family. Throughout this datasheet, the 28F200 refers to all x8/x16 2-Mbit products, while 28F002 refers to all x8 2-Mbit products. Section 1 provides an overview of the flash memory family including applications, pinouts and pin descriptions. Sections 2 and 3 describe, in detail, the specific memory organizations and principles of operation for these products. Finally, Sections 4 and 5 describe the family's operating specifications. Tables 1 and 2 provide a quick reference to each product's voltage supply capability.

1.1 New Features in the SmartVoltage Products

The new SmartVoltage boot block flash memory family offers identical operation as the current BX/BL 12V program products, except for the differences listed below. All other functions are equivalent to current products, including signatures, write commands, and pinouts.

- WP# pin has replaced a DU pin. See Table 3 and Table 10 for details.
- 5V Program/Erase operation has been added that uses proven program and erase techniques with 5V ± 10% applied to V_{PP}.
- Enhanced circuits optimize performance at 3.3V V_{CC}.

If you are designing with existing BX/BL 12V V_{PP} boot block products today, you should provide the capability in your board design to upgrade to these new SmartVoltage products.

Follow these guidelines to ensure compatibilty:

1. Connect WP# (DU on existing products) to control signal or to V_{CC} or GND.
2. If adding a switch on V_{PP} for write protection, switch to GND for complete write protection.
3. Allow for connecting 5V to V_{PP} and disconnect 12V from V_{PP} line, if desired.

1.2 Main Features

Intel's SmartVoltage technology provides the most flexible voltage solution in the industry. SmartVoltage provides two discrete voltage supply pins, V_{CC} for read operation, and V_{PP} for program and erase operation. Discrete supply pins allow system designers to use the optimal voltage levels for their design. The 28F200/002BV provides read capability at 3.3V or 5V, and program/erase capability at 5V or 12V. Since many designs read from the flash memory a large percentage of the time, 3.3V V_{CC} operation can provide great power savings. If read performance is an issue, however, 5V V_{CC} provides faster read access times. For program and erase operations, 5V V_{PP} operation eliminates the need for in system voltage converters, while 12V V_{PP} operation provides faster program and erase for situations where 12V is available, such as manufacturing or designs where 12V is in-system.

The 28F200/28F002 boot block flash memory family is a very high-performance, 2-Mbit (2,097,152 bit) flash memory family organized as either 256 Kwords (131,072 words) of 16 bits each or 512 Kbytes (262,144 bytes) of 8 bits each.

Separately erasable blocks, including a hardware-lockable boot block (16,384 bytes), two parameter blocks (8,192 bytes each) and main blocks (one block of 98,304 bytes and three blocks of 131,072 bytes) define the boot block flash family architecture. See Figure 7 and 8 for memory maps. Each block can be independently erased and programmed 100,000 times at commercial temperature or 10,000 times at extended temperature.

Table 1. x8/x16 Boot Block Product Family

Product Name	V_{PP}		V_{CC}	
	12V	5V	5V	3V
28F200BV-T/B	✓	✓	✓	✓

Table 2. x8-only Boot Block Product Family

Product Name	V_{PP}		V_{CC}	
	12V	5V	5V	3V
28F002BV-T/B	✓	✓	✓	✓

The boot block is located at either the top (denoted by **-T** suffix) or the bottom (**-B** suffix) of the address map in order to accommodate different microprocessor protocols for boot code location. The hardware-lockable boot block provides complete code security for the kernel code required for system initialization. Locking and unlocking of the boot block is controlled by WP# and/or RP# (see Section 3.4 for details).

The Command User Interface (CUI) serves as the interface between the microprocessor or microcontroller and the internal operation of the boot block flash memory products. The internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for program and erase operations, including verifications, thereby unburdening the microprocessor or microcontroller of these tasks. The Status Register (SR) indicates the status of the WSM and whether it successfully completed the desired program or erase operation.

Program and Erase Automation allows program and erase operations to be executed using an industry-standard two-write command sequence to the CUI. Data writes are performed in word (28F200 family) or byte (28F200 or 28F002 families) increments. Each byte or word in the Flash memory can be programmed independently of other memory locations, unlike erases, which erase all locations within a block simultaneously.

The 2-Mbit SmartVoltage boot block flash memory family is also designed with an Automatic Power Savings (APS) feature which minimizes system battery current drain, allowing for very low power designs. To provide even greater power savings, the boot block family includes a deep power-down mode which minimizes power consumption by turning most of the Flash memory's circuitry off. This mode is controlled by the RP# pin and its usage is discussed in Section 3.5, along with other power consumption issues.

Additionally, the RP# pin provides protection against unwanted command writes due to invalid system bus conditions that may occur during system reset and power-up/down sequences. Also, when the Flash memory powers-up, it automatically defaults to the read array mode, but during a warm system reset, where power continues uninterrupted to the system components, the flash memory could remain in a non-read mode, such as erase. Consequently, the system Reset pin should be tied to RP# to reset the memory to normal read mode upon activation of the Reset pin.

For the 28F200, byte-wide or word-wide input/output is controlled by the BYTE# pin. Please see Table 3 for a detailed description of BYTE# operations, especially the usage of the DQ_{15}/A_{-1} pin.

The 28F200 products are available in a ROM/EPROM-compatible pinout and housed in the 44-Lead PSOP (Plastic Small Outline) package, the 48-Lead TSOP (Thin Small Outline, 1.2 mm thick) package and the 56-Lead TSOP as shown in Figure 4, 5 and 6, respectively. The 28F002 products are available in the 40-Lead TSOP package as shown in Figure 3.

Refer to the DC Characteristics Table, Section 4.2 (commercial temperature) and Section 5.2 (extended temperature), for complete current and voltage specifications. Refer to the AC Characteristics Table, Section 4.3 (commercial temperature) and Section 5.3 (extended temperature), for read, write and erase performance specifications.

1.3 Applications

The 2-Mbit boot block flash memory family combines high-density, low-power, high-performance, cost-effective flash memories with blocking and hardware protection capabilities. Their flexibility and versatility reduce costs throughout the product life cycle. Flash memory is ideal for Just-In-Time production flow, reducing system inventory and costs, and eliminating component handling during the production phase.

When your product is in the end-user's hands, and updates or feature enhancements become necessary, flash memory reduces the update costs by allowing user-performed code changes instead of costly product returns or technician calls.

The 2-Mbit boot block flash memory family provides full-function, blocked flash memories suitable for a wide range of applications. These applications include extended PC BIOS and ROM-able applications storage, digital cellular phone program and data storage, telecommunication boot/firmware, printer firmware/font storage and various other embedded applications where program and data storage are required.

Reprogrammable systems such as personal computers, are ideal applications for the 2-Mbit flash memory products. Increasing software sophistication greatens the probability that a code update will be required after the PC is shipped. For example, the emerging of "Plug and Play" standard in desktop and portable PCs enables auto-configuration of ISA and PCI add-in cards. However, since the "Plug and Play" specification continues to evolve, a flash BIOS provides a cost-effective capability to update existing PCs. In addition, the parameter blocks are ideal for storing the required auto-configuration parameters, allowing you to integrate the BIOS PROM and parameter storage EEPROM into a single component, reducing parts costs while increasing functionality.

The 2-Mbit flash memory products are also excellent design solutions for digital cellular phone and telecommunication switching applications requiring very low power consumption, high-performance, high-density storage capability, modular software designs, and a small form factor package. The 2-Mbit's blocking scheme allows for easy segmentation of the embedded code with 16 Kbytes of hardware-protected boot code, two main blocks of program code and two parameter blocks of 8 Kbytes each for frequently updated data storage and diagnostic messages (e.g., phone numbers, authorization codes).

Intel's boot block architecture provides a flexible voltage solution for the different design needs of various applications. The asymmetrically blocked memory map allows the integration of several memory components into a single Flash device. The boot block provides a secure boot PROM; the parameter blocks can emulate EEPROM functionality for parameter store with proper software techniques; and the main blocks provide code and data storage with access times fast enough to execute code in place, decreasing RAM requirements.

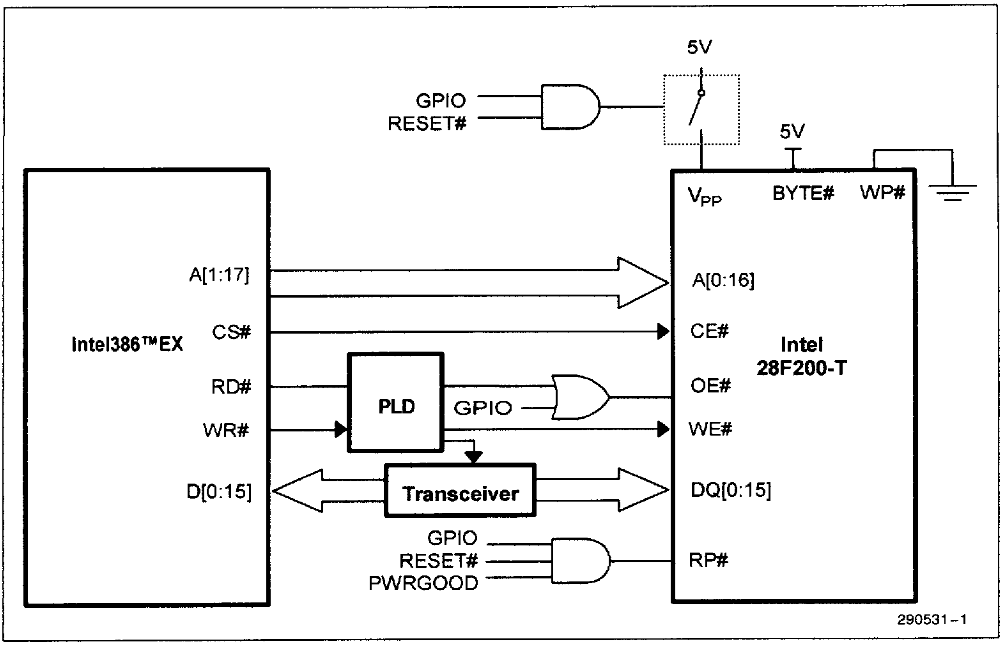


Figure 1. 28F200 Interface to Intel386EX™ Microprocessor

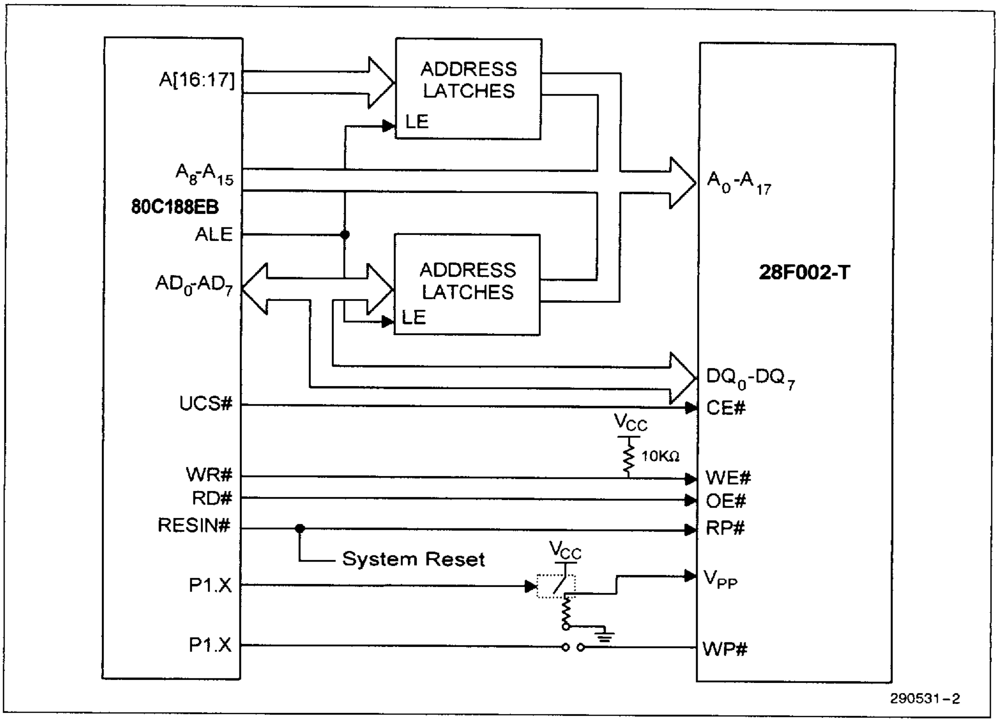
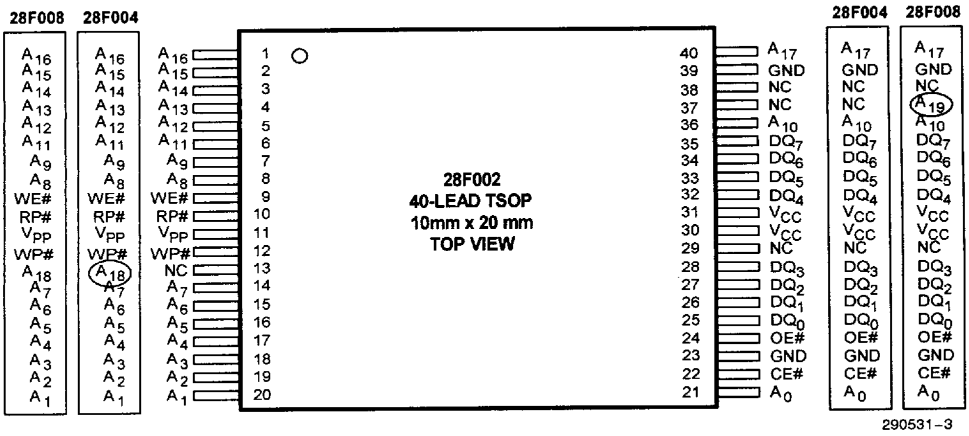


Figure 2. 28F002 Interface to Intel80C188EB 8-Bit Embedded Microprocessor

1.4 Pinouts

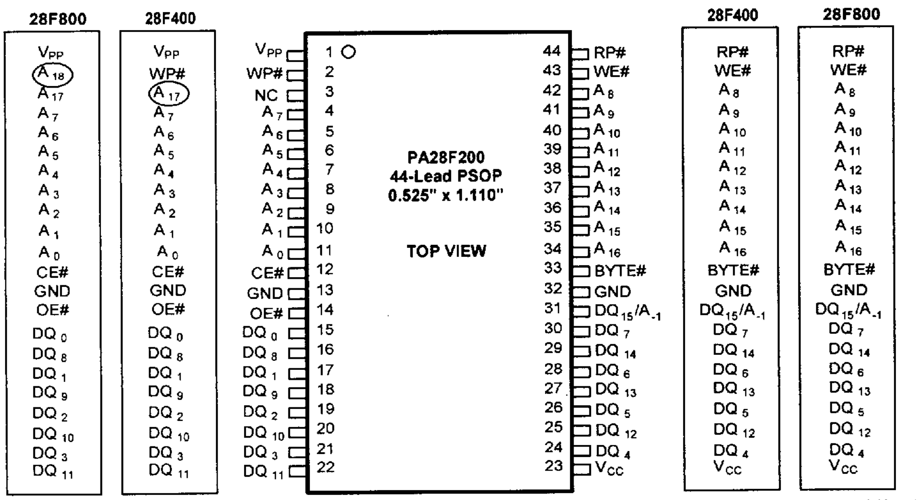
Intel's SmartVoltage Boot Block architecture provides upgrade paths in every package pinout to the 8-Mbit density. The 28F002 40-Lead TSOP pinout for space-constrained designs is shown in Figure 3. The 28F200 44-Lead PSOP pinout follows the industry standard ROM/EPROM pinout as shown in Figure 4. For designs that require x16 operation but have space concerns, refer to the 48-Lead pinout in Figure 5. Furthermore, the 28F200 56-Lead TSOP pinout shown in Figure 6 provides density upgrades to future higher density boot block memories.

Pinouts for the corresponding 4-Mbit and 8-Mbit components are also provided for convenient reference. 2-Mbit pinouts are given on the chip illustration in the center, with 4-Mbit and 8-Mbit pinouts going outward from the center.



NOTE:
Pin 12 is DU for BX/BL 12V V_{PP} Versions.

Figure 3. The 40-Lead TSOP Offers the Smallest Form Factor for Space-Constrained Applications



NOTE:
Pin 2 is DU for BX/BL 12V V_{PP} Versions, but for the 8-Mbit device, pin 2 has been changed to A_{18} (WP# on 2/4 Mbit). Designs planning on upgrading to the 8-Mbit density from the 2/4-Mbit density in this package should design pin 2 to control WP# functionality at the 2/4-Mbit level and allow for pin 2 to control A_{18} after upgrading to the 8-Mbit density.

Figure 4. The 44-Lead PSOP Offers a Convenient Upgrade from JEDEC ROM Standards

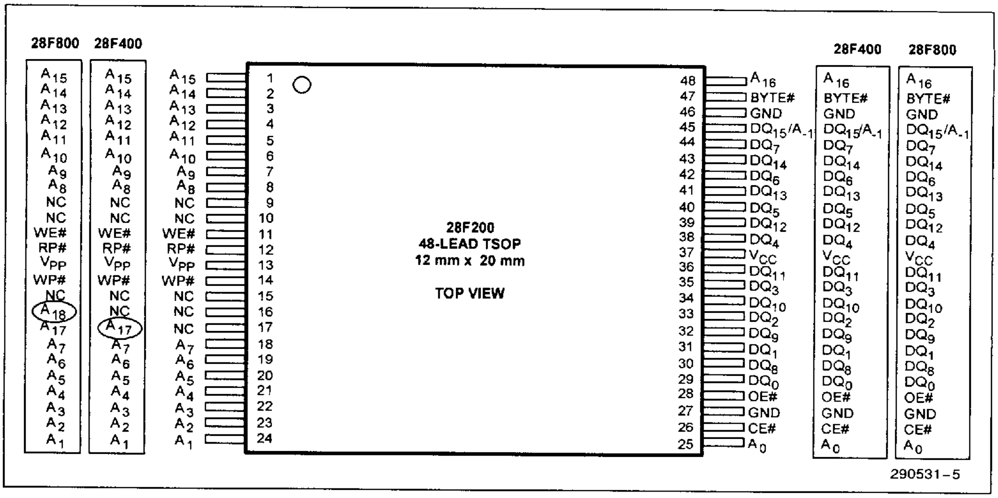
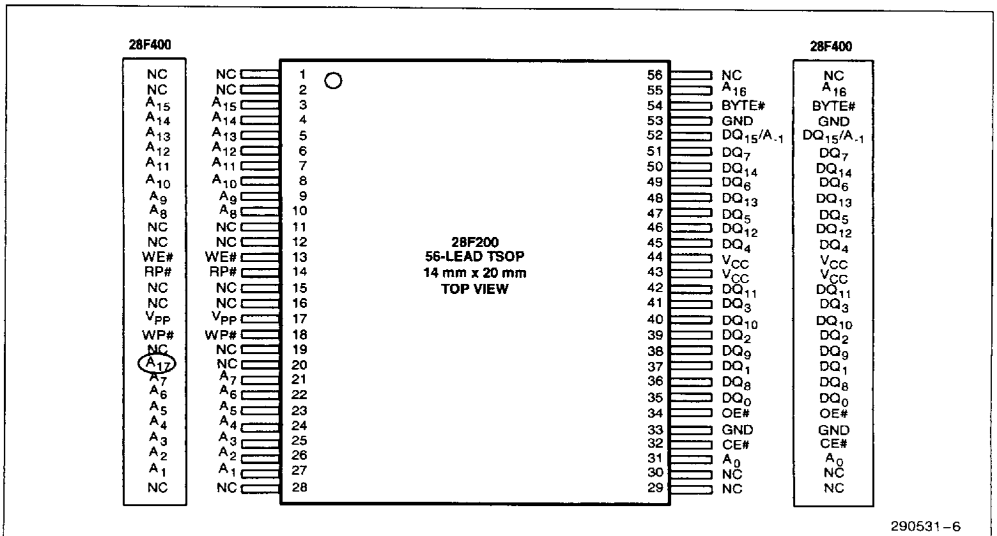


Figure 5. The 48-Lead TSOP Offers the Smallest Form Factor for x16 Operation



NOTE:
Pin 18 is DU for BX/BL 12V V_{PP} Versions.

Figure 6. The 56-Lead TSOP Offers Compatibility between 2 Mbits and 4 Mbits

1.5 Pin Descriptions

Table 3. 28F200/002 Pin Descriptions

Symbol	Type	Name and Function
A_0–A_{17}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle. **The 28F200 only has A_0–A_{16} pins, while the 28F002 has A_0–A_{17}.**
A_9	INPUT	**ADDRESS INPUT:** When A_9 is at V_{HH} the signature mode is accessed. During this mode, A_0 decodes between the manufacturer and device IDs. When BYTE# is at a logic low, only the lower byte of the signatures are read. DQ_{15}/A_{-1} is a don't care in the signature mode when BYTE# is low.
DQ_0–DQ_7	INPUT/ OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs array data on the second CE# and WE# cycle during a Program command. Inputs commands to the Command User Interface when CE# and WE# are active. Data is internally latched during the Write cycle. Outputs array, Intelligent Identifier and Status Register data. The data pins float to tri-state when the chip is de-selected or the outputs are disabled.
DQ_8–DQ_{15}	INPUT/ OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs array data on the second CE# and WE# cycle during a Program command. Data is internally latched during the Write cycle. Outputs array data. The data pins float to tri-state when the chip is de-selected or the outputs are disabled as in the byte-wide mode (BYTE# = "0"). In the byte-wide mode DQ_{15}/A_{-1} becomes the lowest order address for data output on DQ_0–DQ_7. **The 28F002 does not include these DQ_8–DQ_{15} pins.**
CE#	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. CE# is active low. CE# high de-selects the memory device and reduces power consumption to standby levels. If CE# and RP# are high, but not at a CMOS high level, the standby current will increase due to current flow through the CE# and RP# input stages.
OE#	INPUT	**OUTPUT ENABLE:** Enables the device's outputs through the data buffers during a read cycle. OE# is active low.
WE#	INPUT	**WRITE ENABLE:** Controls writes to the Command Register and array blocks. WE# is active low. Addresses and data are latched on the rising edge of the WE# pulse.
RP#	INPUT	**RESET/DEEP POWER-DOWN:** Uses three voltage levels (V_{IL}, V_{IH}, and V_{HH}) to control two different functions: reset/deep power-down mode and boot block unlocking. It is backwards-compatible with the 28F200BX/BL. **When RP# is at logic low, the device is in reset/deep powerdown mode,** which puts the outputs at High-Z, resets the Write State Machine, and draws minimum current. **When RP# is at logic high, the device is in standard operation.** When RP# transitions from logic-low to logic-high, the device defaults to the read array mode. **When RP# is at V_{HH}, the boot block is unlocked** and can be programmed or erased. This overides any control from the WP# input.

Table 3. 28F200/002 Pin Descriptions (Continued)

Symbol	Type	Name and Function
WP#	INPUT	**WRITE PROTECT:** Provides a method for unlocking the boot block in a system without a 12V supply. WP# must be driven to logic high or low, not left floating. **When WP# is at logic low, the boot block is locked,** preventing Program and Erase operations to the boot block. If a Program or Erase operation is attempted on the boot block when WP# is low, the corresponding status bit (bit 4 for Program, bit 5 for Erase) will be set in the Status Register to indicate the operation failed. **When WP# is at logic high, the boot block is unlocked** and can be programmed or erased. **NOTE:** This feature is overridden and the boot block unlocked when RP# is at V_{HH}. See Section 3.4 for details on write protection.
BYTE#	INPUT	**BYTE# ENABLE: Not available on 28F002.** Controls whether the device operates in the byte-wide mode (x8) or the word-wide mode (x16). BYTE# pin must be controlled at CMOS levels to meet the CMOS current specification in the standby mode. **When BYTE# is at logic low, the byte-wide mode is enabled,** where data is read and programmed on DQ_0–DQ_7 and DQ_{15}/A_{-1} becomes the lowest order address that decodes between the upper and lower byte. DQ_8–DQ_{14} are tri-stated during the byte-wide mode. **When BYTE# is at logic high, the word-wide mode is enabled,** where data is read and programmed on DQ_0–DQ_{15}.
V_{CC}		**DEVICE POWER SUPPLY:** 5.0V ± 10%, 3.3V ± 0.3V
V_{PP}		**PROGRAM/ERASE POWER SUPPLY:** For erasing memory array blocks or programming data in each block, a voltage either of 5V ± 10% or 12V ± 5% must be applied to this pin. When $V_{PP} < V_{PPLK}$ all blocks are locked and protected against Program and Erase commands.
GND		**GROUND:** For all internal circuitry.
NC		**NO CONNECT:** Pin may be driven or left floating.

2.0 PRODUCT DESCRIPTION

2.1 Memory Organization

2.1.1 BLOCKING

This product family features an asymmetrically blocked architecture providing system memory integration. Each erase block can be erased independently of the others up to 100,000 times at commercial temperature or up to 10,000 times at extended temperature. The block sizes have been chosen to optimize their functionality for common applications of nonvolatile storage. For the address locations of the blocks, see the memory maps in Figures 7 and 8.

2.1.1.1 Boot Block—1 x 16 KB

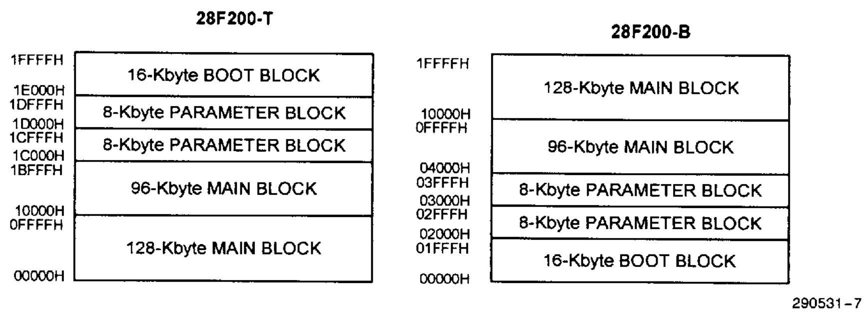
The boot block is intended to replace a dedicated boot PROM in a microprocessor or microcontroller-based system. The 16-Kbyte (16,384 bytes) boot block is located at either the top (denoted by -T suffix) or the bottom (-B suffix) of the address map to accommodate different microprocessor protocols for boot code location. This boot block features hardware controllable write-protection to protect the crucial microprocessor boot code from accidental erasure. The protection of the boot block is controlled using a combination of the V_{PP}, RP#, and WP# pins, as is detailed in Section 3.4.

2.1.1.2 Parameter Blocks—2 x 8 KB

The boot block architecture includes parameter blocks to facilitate storage of frequently updated small parameters that would normally require an EEPROM. By using software techniques, the byte-rewrite functionality of EEPROMs can be emulated. These techniques are detailed in Intel's AP-604, "Using Intel's Boot Block Flash Memory Parameter Blocks to Replace EEPROM." Each boot block component contains two parameter blocks of eight Kbytes (8,192 bytes) each. The parameter blocks are not write-protectable.

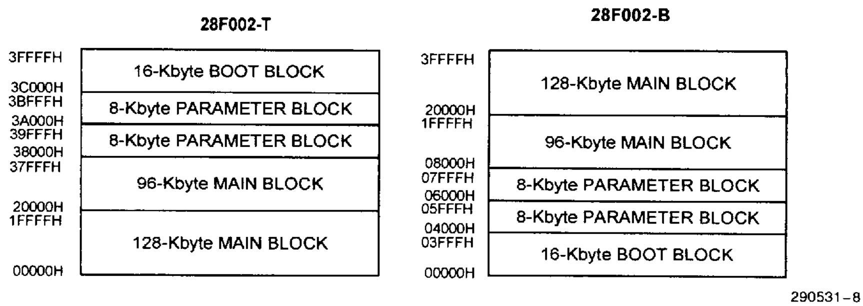
2.1.1.3 Main Blocks—1 x 96 KB + 1 x 128 KB

After the allocation of address space to the boot and parameter blocks, the remainder is divided into main blocks for data or code storage. Each 2-Mbit device contains one 96-Kbyte (98,304 byte) block and one 128-Kbyte (131,072 byte) blocks. See the memory maps for each device for more information.



NOTE:
Address = A[17:0]. In x8 operation, the least significant system address should be connected to A_{-1}. Memory maps are shown for x16 operation.

Figure 7. 28F200-T/B Memory Maps



NOTE:
Address = A[18:0].

Figure 8. 28F002-T/B Memory Maps

3.0 PRODUCT FAMILY PRINCIPLES OF OPERATION

Flash memory augments EPROM functionality with in-circuit electrical write and erase. The boot block flash family utilizes a Command User Interface (CUI) and automated algorithms to simplify write and erase operations. The CUI allows for 100% TTL-level control inputs, fixed power supplies during erasure and programming, and maximum EPROM compatibility.

When $V_{PP} < V_{PPLK}$, the device will only successfully execute the following commands: Read Array, Read Status Register, Clear Status Register and intelligent identifier mode. The device provides standard EPROM Read, Standby and Output Disable operations. Manufacturer Identification and Device Identification data can be accessed through the CUI or through the standard EPROM A_9 high voltage access (V_{ID}) for PROM programming equipment.

The same EPROM Read, Standby and Output Disable functions are available when 5V or 12V is applied to the V_{PP} pin. In addition, 5V or 12V on V_{PP} allows write and erase of the device. All functions associated with altering memory contents: Write and Erase, Intelligent Identifier Read, and Read Status are accessed via the CUI.

The purpose of the Write State Machine (WSM) is to completely automate the write and erasure of the device. The WSM will begin operation upon receipt of a signal from the CUI and will report status back through a Status Register. The CUI will handle the WE# interface to the data and address latches, as well as system software requests for status while the WSM is in operation.

3.1 Bus Operations

Flash memory reads, erases and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles. These bus operations are summarized in Tables 4 and 5.

3.2 Read Operations

3.2.1 READ ARRAY

When RP# transitions from V_{IL} (reset) to V_{IH}, the device will be in the read array mode and will respond to the read control inputs (CE#, address inputs) and OE#) without any commands being written to the CUI.

When the device is in the read array mode, five control signals must be controlled to obtain data at the outputs.

- WE# must be logic high (V_{IH})
- CE# must be logic low (V_{IL})
- OE must be logic low (V_{IL})
- RP# must be logic high (V_{IH})
- BYTE# must be logic high or logic low.

In addition, the address of the desired location must be applied to the address pins. Refer to Figure 18 and 19 for the exact sequence and timing of these signals.

If the device is not in read array mode, as would be the case after a program or erase operation, the Read Mode command (FFH) must be written to the CUI before reads can take place.

Table 4. Bus Operations for Word-Wide Mode (BYTE# = V_{IH})

Mode	Notes	RP#	CE#	OE#	WE#	A_9	A_0	V_{PP}	DQ_{0-15}
Read	1,2,3	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	X	D_{OUT}
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	X	High Z
Standby		V_{IH}	V_{IH}	X	X	X	X	X	High Z
Deep Power-Down	9	V_{IL}	X	X	X	X	X	X	High Z
Intelligent Identifier (Mfr)	4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IL}	X	0089 H
Intelligent Identifier (Device)	4,5	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IH}	X	See Table 6
Write	6,7,8	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	X	D_{IN}

Table 5. Bus Operations for Byte-Wide Mode (BYTE# = V_{IL})

Mode	Notes	RP#	CE#	OE#	WE#	A_9	A_0	A_{-1}	V_{PP}	DQ_{0-7}	DQ_{8-14}
Read	1,2,3	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	X	X	D_{OUT}	High Z
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	X	X	High Z	High Z
Standby		V_{IH}	V_{IH}	X	X	X	X	X	X	High Z	High Z
Deep Power-Down	9	V_{IL}	X	X	X	X	X	X	X	High Z	High Z
Intelligent Identifier (Mfr)	4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IL}	X	X	89H	High Z
Intelligent Identifier (Device)	4,5	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IH}	X	X	See Table 6	High Z
Write	6,7,8	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	X	X	D_{IN}	High Z

NOTES:
1. Refer to DC Characteristics.
2. X can be V_{IL}, V_{IH} for control pins and addresses, V_{PPLK} or V_{PPH} for V_{PP}.
3. See DC Characteristics for V_{PPLK}, $V_{PPH}1$, $V_{PPH}2$, V_{HH}, V_{ID} voltages.
4. Manufacturer and Device codes may also be accessed via a CUI write sequence, A_1-A_{16} = X, A_1-A_{17} = X.
5. See Table 6 of Device IDs.
6. Refer to Table 7 for valid D_{IN} during a Write operation.
7. Command writes for Block Erase or Word/Byte Write are only executed when V_{PP} = $V_{PPH}1$ or $V_{PPH}2$.
8. To Write or Erase the boot block, hold RP# at V_{HH} or WP# at V_{IH}.
9. RP# must be at GND ± 0.2V to meet the maximum deep power-down current specified.

3.2.2 INTELLIGENT IDENTIFIERS

The intelligent identifiers of the SmartVoltage boot block components are identical to the boot block products that operate only at 12V V_{PP}. The manufacturer and device codes are read via the CUI or by taking the A_9 pin to V_{ID}. Writing 90H to the CUI places the device into intelligent identifier read mode. In this mode, $A_0 = 0$ outputs the manufacturer's identification code and $A_0 = 1$ outputs the device code. When BYTE# is at a logic low, only the lower byte of the above signatures is read and DQ_{15}/A_{-1} is a "don't care" during intelligent identifier mode. For x8 only products only the lower byte is read. See the Table 6 below for product signatures. A Read Array command must be written to the memory to return to the read array mode.

Table 6. Intelligent Identifier Table

Product	Mfr. ID	Device ID	
		-T (Top Boot)	-B (Bottom Boot)
28F200	0089 H	2274 H	2275 H
28F002	89 H	7C H	7D H

3.3 Write Operations

3.3.1 COMMAND USER INTERFACE (CUI)

The Command User Interface (CUI) serves as the interface between the microprocessor and the internal chip controller. Commands are written to the CUI using standard microprocessor write timings. The available commands are Read Array, Read Intelligent Identifier, Read Status Register, Clear Status Register, Erase and Program (summarized in Tables 7 and 8). For Read commands, the CUI points the read path at either the array, the intelligent identifier, or the Status Register depending on the command received. For Program or Erase commands, the CUI informs the Write State Machine (WSM) that a write or erase has been requested. During the execution of a Program command, the WSM will control the programming sequences and the CUI will only respond to status reads. During an erase cycle, the CUI will respond to status reads and erase suspend. After the WSM has completed its task, it will set the WSM Status bit to a "1," which will also allow the CUI to respond to its full command set. Note that after the WSM has returned control to the CUI, the CUI will stay in the current command state until it receives another command.

Table 7. Command Set Codes and Corresponding Device Mode

Command Codes	Device Mode
00	Invalid Reserved
10	Alternate Program Set-Up
20	Erase Set-Up
40	Program Set-Up
50	Clear Status Register
70	Read Status Register
90	Intelligent Identifier
B0	Erase Suspend
D0	Erase Resume/Erase Confirm
FF	Read Array

Table 8. Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array	8	Write	X	FFH			
Intelligent Identifier	1	Write	X	90H	Read	IA	IID
Read Status Register	2,4	Write	X	70H	Read	X	SRD
Clear Status Register	3	Write	X	50H			
Word/Byte Write		Write	WA	40H	Write	WA	WD
Alternate Word/Byte Write	6,7	Write	WA	10H	Write	WA	WD
Block Erase/Confirm	6,7	Write	BA	20H	Write	BA	D0H
Erase Suspend/Resume	5	Write	X	B0H	Write	X	D0H

ADDRESS
BA = Block Address
IA = Identifier Address
WA = Write Address
X = Don't Care

DATA
SRD = Status Register Data
IID = Identifier Data
WD = Write Data

NOTES:
1. Bus operations are defined in Tables 4 and 5.
2. IA = Identifier Address: A0 = 0 for manufacturer code, A0 = 1 for device code.
3. SRD—Data read from Status Register.
4. IID = Intelligent Identifier Data. Following the Intelligent Identifier command, two Read operations access manufacturer and device codes.
5. BA = Address within the block being erased.
6. WA = Address to be written. WD = Data to be written at location WD.
7. Either 40H or 10H commands is valid.
8. When writing commands to the device, the upper data bus [DQ_8–DQ_{15}] = X (28F200 only) which is either V_{IL} or V_{IH}, to minimize current draw.

3.3.1.1 Command Function Description

Device operations are selected by writing specific commands into the CUI. Tables 7 and 8 define the available commands.

Invalid/Reserved

These are unassigned commands and should not be used. Intel reserves the right to redefine these codes for future functions.

Read Array (FFH)

This single write cycle command points the read path at the array. If the host CPU performs a CE#/OE#-controlled Read immediately following a two-write sequence that started the WSM, then the device will output Status Register contents. If the Read Array command is given after the Erase Setup command, the device will reset to read the array. A two Read Array command sequence (FFH) is required to reset to Read Array after the Program Setup command.

Intelligent Identifier (90H)

After this command is executed, the CUI points the output path to the intelligent identifier circuits. Only intelligent identifier values at addresses 0 and 1 can be read (only address A_0 is used in this mode, all other address inputs are ignored).

Read Status Register (70H)

This is one of the two commands that is executable while the WSM is operating. After this command is written, a read of the device will output the contents of the Status Register, regardless of the address presented to the device.

The device automatically enters this mode after program or erase has completed.

Clear Status Register (50H)

The WSM can only set the Program Status and Erase Status bits in the Status Register to "1," it cannot clear them to "0."

Two reasons exist for operating the Status Register in this fashion. The first is synchronization. Since the WSM does not know when the host CPU has read the Status Register, it would not know when to clear the status bits. Secondly, if the CPU is programming a string of bytes, it may be more efficient to query the Status Register after programming the string. Thus, if any errors exist while programming the string, the Status Register will return the accumulated error status.

Program Setup (40H or 10H)

This command simply sets the CUI into a state such that the next write will load the Address and Data registers. After this command is executed, the outputs default to the Status Register. A two Read Array command sequence (FFH) is required to reset to Read Array after the Program Setup command.

Program

The second write after the Program Setup command, will latch addresses and data. Also, the CUI initiates the WSM to begin execution of the program algorithm. The device outputs Status Register data when OE# is enabled. A Read Array command is required after programming, to read array data.

Erase Setup (20H)

Prepares the CUI for the Erase Confirm command. No other action is taken. If the next command is not an Erase Confirm command, then the CUI will set both the Program Status and Erase Status bits of the Status Register to a "1," place the device into the Read Status Register state, and wait for another command.

Erase Confirm (D0H)

If the previous command was an Erase Setup command, then the CUI will enable the WSM to erase, at the same time closing the address and data latches, and respond only to the Read Status Register and Erase Suspend commands. While the WSM is executing, the device will output Status Register data when OE# is toggled low. Status Register data can only be updated by toggling either OE# or CE# low.

Erase Suspend (B0H)

This command is only valid while the WSM is executing an Erase operation, and therefore will only be responded to during an Erase operation. After this command has been executed, the CUI will set an output that directs the WSM to suspend Erase operations, and then respond only to Read Status Register or to the Erase Resume commands. Once the WSM has reached the Suspend state, it will set an output into the CUI which allows the CUI to respond to the Read Array, Read Status Register, and Erase Resume commands. In this mode, the CUI will not respond to any other commands. The WSM will also set the WSM Status bit to a "1." The WSM will continue to run, idling in the SUSPEND state, regardless of the state of all input control pins except RP#, which will immediately shut down the WSM and the remainder of the chip, if it is made active. During a Suspend operation, the data and address latches will remain closed, but the address pads are able to drive the address into the read path.

Erase Resume (D0H)

This command will cause the CUI to clear the Suspend state and clear the WSM Status Bit to a "0," but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect under any other conditions.

3.3.2 STATUS REGISTER

The device contains a Status Register which may be read to determine when a Program or Erase operation is complete, and whether that operation completed successfully. The Status Register may be read at any time by writing the Read Status command to the CUI. After writing this command, all subsequent Read operations output data from the Status Register until another command is written to the CUI. A Read Array command must be written to the CUI to return to the read array mode.

The Status Register bits are output on DQ[0:7], whether the device is in the byte-wide (x8) or word-wide (x16) mode. In the word-wide mode the upper byte, DQ[8:15], is set to 00H during a Read Status command. In the byte-wide mode, DQ[8:14] are tri-stated and DQ_{15}/A_{-1} retains the low order address function.

Important: *The contents of the Status Register are latched on the falling edge of OE# or CE#, whichever occurs last in the read cycle.* This prevents possible bus errors which might occur if the contents of the Status Register change while reading the Status Register. CE# or OE# must be toggled with each subsequent status read, or the completion of a Program or Erase operation will not be evident from the Status Register.

When the WSM is active, this register will indicate the status of the WSM, and will also hold the bits indicating whether or not the WSM was successful in performing the desired operation.

3.3.2.1 Clearing the Status Register

The WSM sets status bits "3" through "7" to "1," and clears bits "6" and "7" to "0," but cannot clear status bits "3" through "5" to "0." Bits 3 through 5 can only be cleared by the controlling CPU through the use of the Clear Status Register command. These bits can indicate various error conditions. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several bytes or erasing multiple blocks in sequence). The Status Register may then be read to determine if an error occurred during that programming or erasure series. This adds flexibility to the way the device may be programmed or erased. To clear the Status Register, the Clear Status Register command is written to the CUI. Then, any other command may be issued to the CUI. Note, again, that before a read cycle can be initiated, a Read Array command must be written to the CUI to specify whether the read data is to come from the Memory Array, Status Register, or Intelligent Identifier.

Table 9. Status Register Bit Definition

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Write State Machine bit must first be checked to determine Byte/Word program or Block Erase completion, before the Program or Erase Status bits are checked for success.
SR.6 = ERASE-SUSPEND STATUS (ESS) 1 = Erase Suspended 0 = Erase in Progress/Completed	When Erase Suspend is issued, WSM halts execution and sets both WSMS and ESS bits to "1." ESS bit remains set to "1" until an Erase Resume command is issued.
SR.5 = ERASE STATUS 1 = Error in Block Erasure 0 = Successful Block Erase	When this bit is set to "1," WSM has applied the maximum number of erase pulses to the block and is still unable to successfully verify block erasure.
SR.4 = PROGRAM STATUS 1 = Error in Byte/Word Program 0 = Successful Byte/Word Program	When this bit is set to "1," WSM has attempted but failed to program a byte or word.
SR.3 = V_{PP} STATUS 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK	The V_{PP} Status bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP} level only after the Byte Write or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. V_{PP} Status bit is not guaranteed to report accurate feedback between V_{PPLK} and V_{PPH}.
SR.2–SR.0 = RESERVED FOR FUTURE ENHANCEMENTS	These bits are reserved for future use and should be masked out when polling the Status Register.

3.3.3 PROGRAM MODE

Programming is executed using a two-write sequence. The Program Setup command is written to the CUI followed by a second write which specifies the address and data to be programmed. The WSM will execute a sequence of internally timed events to:

1. Program the desired bits of the addressed memory word or byte.
2. Verify that the desired bits are sufficiently programmed.

Programming of the memory results in specific bits within a byte or word being changed to a "0."

If the user attempts to program "1"s, there will be no change of the memory cell content and no error occurs.

Similar to erasure, the Status Register indicates whether programming is complete. While the program sequence is executing, bit 7 of the Status Register is a "0." The Status Register can be polled by toggling either CE# or OE# to determine when the program sequence is complete. Only the Read Status Register command is valid while programming is active.

When programming is complete, the status bits, which indicate whether the Program operation was successful, should be checked. If the programming operation was unsuccessful, bit 4 of the Status

Register is set to a "1" to indicate a Program Failure. If bit 3 is set to a "1," then V_{PP} was not within acceptable limits, and the WSM did not execute the programming sequence. If the program operation fails, bit 4 of the Status Register will be set within 1.5 ms as determined by the timeout of the WSM.

The Status Register should be cleared before attempting the next operation. Any CUI instruction can follow after programming is completed; however, reads from the Memory Array, Status Register, or Intelligent Identifier cannot be accomplished until the CUI is given the Read Array command.

3.3.4 ERASE MODE

Erasure of a single block is initiated by writing the Erase Setup and Erase Confirm commands to the CUI, along with the addresses identifying the block to be erased. These addresses are latched internally when the Erase Confirm command is issued. Block erasure results in all bits within the block being set to "1."

The WSM will execute a sequence of internally timed events to:

1. Program all bits within the block to "0."
2. Verify that all bits within the block are sufficiently programmed to "0."
3. Erase all bits within the block.
4. Verify that all bits within the block are sufficiently erased.

While the erase sequence is executing, bit 7 of the Status Register is a "0."

When the Status Register indicates that erasure is complete, the status bits, which indicate whether the Erase operation was successful, should be checked. If the Erase operation was unsuccessful, bit 5 of the Status Register will be set to a "1", indicating an Erase Failure. If V_{PP} was not within acceptable limits after the Erase Confirm command is issued, the WSM will not execute an erase sequence; instead, bit 5 of the Status Register is set to a "1" to indicate an Erase Failure, and bit 3 is set to a "1" to identify that V_{PP} supply voltage was not within acceptable limits. If the erase operation fails, bit 5 of the Status Register will be set within 1.5 ms as determined by the timeout of the WSM.

The Status Register should be cleared before attempting the next operation. Any CUI instruction can follow after erasure is completed; however, reads from the Memory Array, Status Register, or Intelligent Identifier cannot be accomplished until the CUI is given the Read Array command.

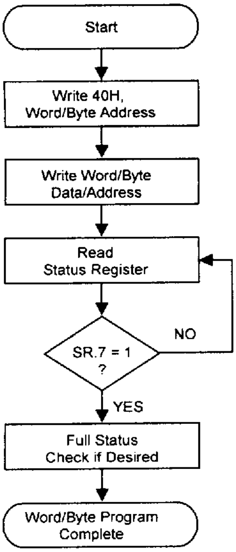
3.3.4.1 Suspending and Resuming Erase

Since an erase operation requires on the order of seconds to complete, an Erase Suspend command is provided to allow erase-sequence interruption in order to read data from another block of the memory. Once the erase sequence is started, writing the Erase Suspend command to the CUI requests that the WSM pause the erase sequence at a predetermined point in the erase algorithm. The Status Register must then be read to determine if the erase operation has been suspended.

At this point, a Read Array command can be written to the CUI in order to read data from blocks other than that which is being suspended. The only other valid command at this time is the Erase Resume command or Read Status Register command.

During erase suspend mode, the chip can go into a pseudo-standby mode by taking CE# to V_{IH}, which reduces active current draw.

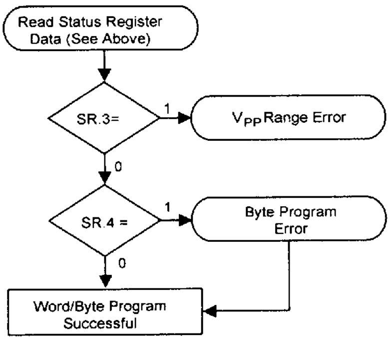
To resume the erase operation, the chip must be enabled by taking CE# to V_{IL}, then issuing the Erase Resume command. When the Erase Resume command is given, the WSM will continue with the erase sequence and complete erasing the block. As with the end of a standard erase operation, the Status Register must be read, cleared, and the next instruction issued in order to continue.



Bus Operation	Command	Comments
Write	Setup Program	Data = 40H Addr = Word/Byte to Program
Write	Program	Data = Data to Program Addr = Location to Program
Read		Status Register Data Toggle CE# or OE# to Update SRD.
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent Word/Byte Writes.
SR Full Status Check can be done after each Word/Byte Write, or after a sequence of Word/Byte Writes.
Write FFH after the last write operation to reset device to read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4 1 = V_{PP} Byte Program Error

SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine.

SR.4 is only clear by the Clear Status Register Command, in cases where multiple bytes are programmed before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

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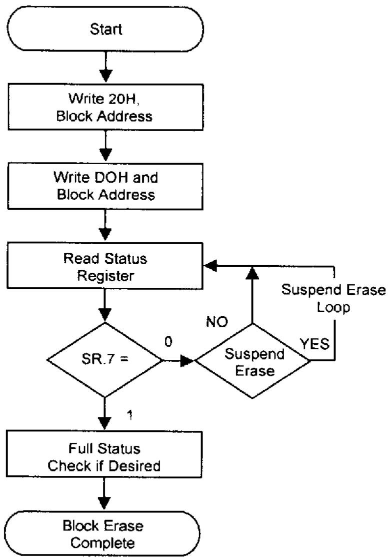
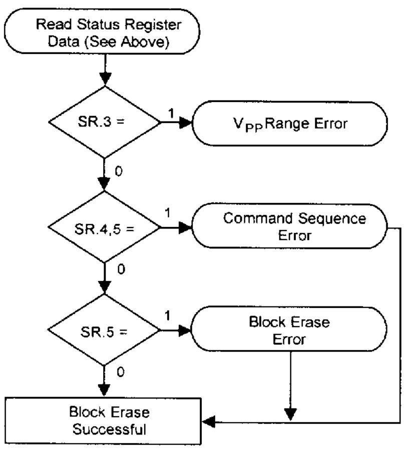
Figure 9. Automated Word/Byte Programming Flowchart



Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Addr = Within Block to be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to be Erased
Read		Status Register Data Toggle CE# or OE# to Update Status Register
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent block erasures.
Full Status Check can be done after each block erase, or after a sequence of block erasures.
Write FFH after the last operation to reset device to Read Array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

SR.3 MUST be cleared, if set during an erase attempt, before further attempts are allowed by the Write State Machine

SR.5 is only clear by the Clear Status Register Command, in cases where multiple blocks are erase before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

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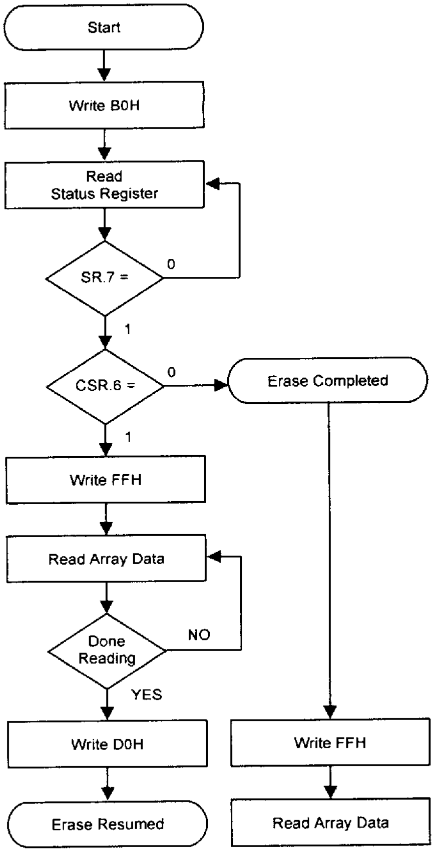
Figure 10. Automated Block Erase Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Read		Status Register Data Toggle CE# or OE# to Update SRD. Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Erase Suspended 0 = Erase Completed
Write	Read Array	Data = FFH Addr = X
Read		Read Array Data from Block Other Than the One Being Erased
Write	Erase Resume	Data = D0H Addr = X

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Figure 11. Erase Suspend/Resume Flowchart

3.4 Boot Block Locking

The boot block family architecture features a hardware-lockable boot block so that the kernel code for the system can be kept secure while the parameter and main blocks are programmed and erased independently as necessary. Only the boot block can be locked independently from the other blocks.

3.4.1 $V_{PP} = V_{IL}$ FOR COMPLETE PROTECTION

For complete write protection of all blocks in the flash device, the V_{PP} programming voltage can be held low. When V_{PP} is below V_{PPLK}, any program or erase operation will result in a error in the Status Register.

3.4.2 WP# = V_{IL} FOR BOOT BLOCK LOCKING

When WP# = V_{IL}, the boot block is locked and any program or erase operation to the boot block will result in an error in the Status Register. All other blocks remain unlocked in this condition and can be programmed or erased normally. Note that this feature is overridden and the boot block unlocked when RP# = V_{HH}.

3.4.3 RP# = V_{HH} OR WP# = V_{IH} FOR BOOT BLOCK UNLOCKING

Two methods can be used to unlock the boot block:

1. WP# = V_{IH}
2. RP# = V_{HH}

If both or either of these two conditions are met, the boot block will be unlocked and can be programmed or erased. The truth table, Table 10, clearly defines the write protection methods.

3.5 Power Consumption

3.5.1 ACTIVE POWER

With CE# at a logic-low level and RP# at a logic-high level, the device is placed in the active mode. Refer to the DC Characteristics table for I_{CC} current values.

Table 10. Write Protection Truth Table for SmartVoltage Boot Block Family

V_{PP}	RP#	WP#	Write Protection Provided
V_{IL}	X	X	All Blocks Locked
$\geq V_{PPLK}$	V_{IL}	X	All Blocks Locked (Reset)
$\geq V_{PPLK}$	V_{HH}	X	All Blocks Unlocked
$\geq V_{PPLK}$	V_{IH}	V_{IL}	Boot Block Locked
$\geq V_{PPLK}$	V_{IH}	V_{IH}	All Blocks Unlocked

3.5.2 AUTOMATIC POWER SAVINGS (APS)

Automatic Power Savings (APS) is a low-power feature during active mode of operation. The boot block flash memory family incorporates Power Reduction Control (PRC) circuitry which allows the device to put itself into a low current state when it is not being accessed. After data is read from the memory array, PRC logic controls the device's power consumption by entering the APS mode where typical I_{CC} current is less than 1 mA. The device stays in this static state with outputs valid until a new location is read.

3.5.3 STANDBY POWER

With CE# at a logic-high level (V_{IH}), and the CUI in read mode, the memory is placed in standby mode. The standby operation disables much of the device's circuitry and substantially reduces device power consumption. The outputs (DQ[0:15] or DQ[0:7]) are placed in a high-impedance state independent of the status of the OE# signal. When CE# is at logic-high level during erase or program functions, the devices will continue to perform the erase or program function and consume erase or program active power until erase or program is completed.

3.5.4 DEEP POWER-DOWN MODE

The SmartVoltage boot block family supports a low typical I_{CC} in deep power-down mode, which turns off all circuits to save power. This mode is activated by the RP# pin when it is at a logic-low (GND $\pm$0.2V.) (Note: BYTE# pin must be at CMOS levels to meet the I_{CCD} specification.)

During read modes, the RP# pin going low deselects the memory and places the output drivers in a high impedance state. Recovery from the deep power-down state, requires a minimum access time of t_{PHQV}. (See AC Characteristics table)

During erase or program modes, RP# low will abort either erase or program operations, but the memory contents are no longer valid as the data has been corrupted by the RP# function. As in the read mode above, all internal circuitry is turned off to achieve the power savings.

RP# transitions to V_{IL}, or turning power off to the device will clear the Status Register.

3.6 Power-Up/Down Operation

The device offers protection against accidental block erasure or programming during power transitions. Power supply sequencing is not required, since the device is indifferent as to which power supply, V_{PP} or V_{CC}, powers-up first. The CUI is reset to the read mode after power-up, but the system must drop CE# low or present a new address to ensure valid data at the outputs.

A system designer must guard against spurious writes when V_{CC} voltages are above V_{LKO} and V_{PP} is active. Since both WE# and CE# must be low for a command write, driving either signal to V_{IH} will inhibit writes to the device. The CUI architecture provides an additional protection since alteration of memory contents can only occur after successful completion of the two-step command sequences. The device is also disabled until RP# is brought to V_{IH}, regardless of the state of its control inputs. By holding the device in reset (RP# connected to system PowerGood) during power up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

3.6.1 RP# CONNECTED TO SYSTEM RESET

The use of RP# during system reset is important with automated write/erase devices because the system expects to read from the flash memory when it comes out of reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization would not occur because the flash memory may be providing status information instead of array data. Intel's flash memories allow proper CPU initialization following a system reset by connecting the RP# pin to the same RESET# signal that resets the system CPU.

3.6.2 V_{CC}, V_{PP} AND RP# TRANSITIONS

The CUI latches commands as issued by system software and is not altered by V_{PP} or CE# transitions or WSM actions. Its default state upon power-up, after exit from deep power-down mode, or after V_{CC} transitions above V_{LKO} (Lockout voltage), is read array mode.

After any Word/Byte Write or Block Erase operation is complete and even after V_{PP} transitions down to V_{PPLK}, the CUI must be reset to read array mode via the Read Array command if accesses to the flash memory are desired.

3.7 Power Supply Decoupling

Flash memory's power switching characteristics require careful device decoupling methods. System designers should consider three supply current issues:

1. Standby current levels (I_{CCS})
2. Active current levels (I_{CCR})
3. Transient peaks produced by falling and rising edges of CE#.

Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1 µF ceramic capacitor connected between each V_{CC} and GND, and between its V_{PP} and GND. These high frequency, inherently low inductance capacitors should be placed as close as possible to the package leads.

3.7.1 V_{PP} TRACE ON PRINTED CIRCUIT BOARDS

Designing for in-system writes to the flash memory requires special consideration of the V_{PP} power supply trace by the printed circuit board designer. The V_{PP} pin supplies the flash memory cells current for programming and erasing. One should use similar trace widths and layout considerations given to the V_{CC} power supply trace. Adequate V_{PP} supply traces, and decoupling capacitors placed adjacent to the component, will decrease spikes and overshoots.

Guide to Subsequent Tables

NOTE:

In the following tables, the topmost heading lists the line items to which the specifications in that column apply. For space considerations, the line items have been abbreviated as shown in the following table. See Section 7.1 for more information on product naming and line items.

Abbreviation	Applicable Product Names
BV-60	E28F200BV-T60, E28F200BV-B60, E28F002BV-T60, E28F002BV-B60, E28F200CV-T60, E28F200CV-B60, PA28F200BV-T60, PA28F200BV-B60
BV-80	E28F200BV-T80, E28F200BV-B80, E28F002BV-T80, E28F002BV-B80, E28F200CV-T80, E28F200CV-B80, PA28F200BV-T80, PA28F200BV-B80
BV-120	E28F002BV-T120, E28F002BV-B120, PA28F200BV-T120, PA28F200BV-B120
TBV-80	TE28F200BV-T80, TE28F200BV-B80, TE28F002BV-T80, TE28F002BV-B80, TE28F200CV-T80, TE28F200CV-B80, TB28F200BV-T80, TB28F200BV-B80

4.0 ABSOLUTE MAXIMUM RATINGS*

Commercial Operating Temperature

During Read .... 0°C to +70°C

During Block Erase and Word/Byte Write .... 0°C to +70°C

Temperature Bias .... −10°C to 80°C

Extended Operating Temperature

During Read .... −40°C to +85°C

During Block Erase and Word/Byte Write .... −40°C to +85°C

Temperature Under Bias .... −40°C to +85°C

Storage Temperature .... −65°C to +125°C

Voltage on Any Pin (except V_{CC}, V_{PP}, A_9 and RP#) with Respect to GND .... −2.0V to +7.0V(2)

Voltage on Pin RP# or Pin A_9 with Respect to GND ...... −2.0V to +13.5V(2,3)

V_{PP} Program Voltage with Respect to GND during Block Erase and Word/Byte Write ..... −2.0V to +14.0V(2,3)

V_{CC} Supply Voltage with Respect to GND .... −2.0V to +7.0V(2)

Output Short Circuit Current .... 100 mA(4)

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

***WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
3. Maximum DC voltage on V_{PP} may overshoot to +14.0V for periods <20 ns. Maximum DC voltage on RP# or A_9 may overshoot to 13.5V for periods <20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. 10% V_{CC} specifications reference the 28F200/002BV-60 in their standard test configurations, and 28F200/002BV-80/120.
6. 5% V_{CC} specifications reference the 28F200/002BV-60 in their high speed test configuration.

5.0 COMMERCIAL OPERATING CONDITIONS

Table 11. Commercial Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Notes	Min	Max	Units
T_A	Operating Temperature		0	70	°C
V_{CC}	3.3V V_{CC} Supply Voltage (±0.3V)		3.0	3.6	Volts
	5V V_{CC} Supply Voltage (10%)	1	4.50	5.50	Volts
	5V V_{CC} Supply Voltage (5%)	2	4.75	5.25	Volts

NOTES:
1. 10% V_{CC} specifications apply to the 60, 80 and 120 ns product versions in their standard test configuration.
2. 5% V_{CC} specifications apply to the 60 ns versions in their high speed test configuration.

5.1 Switching V_{CC} Voltages

Table 12. V_{CC} Supply Switching Timing

Symbol	Parameter	Notes	Min	Max	Unit
T_{5VPH}	V_{CC} at 4.5V (minimum) to RP# High	1	2		μs
T_{3VPH}	V_{CC} at 3.0V (minimum) to RP# High	1	2		μs

NOTES:
1. The T_{5VPH} and/or T_{3VPH} times must be strictly followed to guarantee all other read and write specifications.
2. To switch between 3.3V and 5.0V operation, the system should first transition V_{CC} from the existing voltage to GND, and then to the new voltage. The V_{CC} supply voltage should not be switched when the WSM is busy.

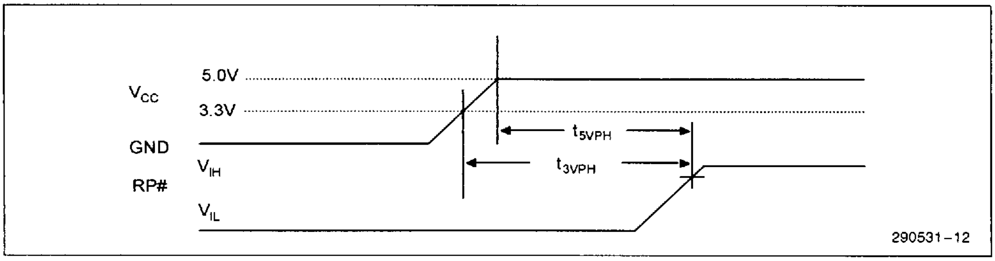


Figure 12. V_{CC} Supply Switching Waveform

5.2 DC Characteristics

Table 13. DC Characteristics (Commercial)

Symbol	Parameter	Notes	BV-60 BV-80 BV-120 V_{CC} = 3.3 ± 0.3V Min	Typ	Max	BV-60 BV-80 BV-120 V_{CC} = 5V ± 10% Min	Typ	Max	Units	Test Conditions
I_{IL}	Input Load Current	1			±1.0			± 1.0	µA	$V_{CC} = V_{CC}$ MAX $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1			±10			± 10	µA	$V_{CC} = V_{CC}$ MAX $V_{IN} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1,3		0.4	1.5		0.8	2.0	mA	$V_{CC} = V_{CC}$ MAX CE# = RP# = BYTE# = WP# = V_{IH}
				60	110		50	130	µA	$V_{CC} = V_{CC}$ MAX CE# = RP# = V_{CC} ± 0.2V
I_{CCD}	V_{CC} Deep Power-Down Current	1		0.2	8		0.2	8	µA	$V_{CC} = V_{CC}$ MAX $V_{IN} = V_{CC}$ or GND RP# = GND ± 0.2V
I_{CCR}	V_{CC} Read Current for Word or Byte	1,5,6		15	30		50	60	mA	**CMOS INPUTS** $V_{CC} = V_{CC}$ MAX CE# = GND OE# = V_{CC} f = 10 MHz (5V), 5 MHz (3.3V) I_{OUT} = 0 mA Inputs = GND ± 0.2V or V_{CC} ± 0.2V
				15	30		55	65	mA	**TTL INPUTS** $V_{CC} = V_{CC}$ MAX CE# = V_{IL} OE# = V_{IH} f = 10 MHz (5V), 5 MHz (3.3V) I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH}
I_{CCW}	V_{CC} Write Current for Word or Byte	1,4		13	30		30	50	mA	Word Write in Progress $V_{PP} = V_{PPH}1$ (at 5V)
				10	25		30	45	mA	Word Write in Progress $V_{PP} = V_{PPH}2$ (at 12V)

Table 13. DC Characteristics (Commercial) (Continued)

Symbol	Parameter	Notes	BV-60 BV-80 BV-120 V_{CC} = 3.3±0.3V Min	Typ	Max	BV-60 BV-80 BV-120 V_{CC} = 5V±10% Min	Typ	Max	Units	Test Conditions
I_{CCE}	V_{CC} Erase Current	1,4		13	30		18	35	mA	Block Erase in Progress $V_{PP} = V_{PPH}1$ (at 5V)
				10	25		18	30	mA	Block Erase in Progress $V_{PP} = V_{PPH}2$ (at 12V)
I_{CCES}	V_{CC} Erase Suspend Current	1,2		3	8.0		5	10	mA	CE# = V_{IH} Block Erase Suspend
I_{PPS}	V_{PP} Standby Current	1		±5	±15		± 5	± 10	μA	$V_{PP} \leq V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1		0.2	10		0.2	5.0	μA	RP# = GND ± 0.2V
I_{PPR}	V_{PP} Read Current	1		50	200		30	200	μA	$V_{PP} > V_{CC}$
I_{PPW}	V_{PP} Word/Byte Write Current	1,4		13	30		13	25	mA	$V_{PP} = V_{PPH}1$ (at 5V) Word Write in Progress
				8	25		8	20		$V_{PP} = V_{PPH}2$ (at 12V) Word Write in Progress
I_{PPE}	V_{PP} Erase Current	1,4		13	30		10	20	mA	$V_{PP} = V_{PPH}1$ (at 5V) Block Erase in Progress
				8	25		5	15		$V_{PP} = V_{PPH}2$ (at 12V) Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1		50	200		30	200	μA	$V_{PP} = V_{PPH}$ Block Erase Suspend in Progress
$I_{RP\#}$	RP# Boot Block Unlock Current	1,4			500			500	μA	RP# = V_{HH}
I_{ID}	A_9 Intelligent Identifier Current	1,4			500			500	μA	$A_9 = V_{ID}$

Table 13. DC Characteristics (Commercial) (Continued)

Symbol	Parameter	Notes	BV-60 BV-80 BV-120 V_{CC} = 3.3 ± 0.3V Min	Typ	Max	BV-60 BV-80 BV-120 V_{CC} = 5V ± 10% Min	Typ	Max	Units	Test Conditions
V_{ID}	A_9 Intelligent Identifier Voltage		11.4		12.6	11.4		12.6	V	
V_{IL}	Input Low Voltage		−0.5		0.8	−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} +0.5V	2.0		V_{CC} +0.5V	V	
V_{OL}	Output Low Voltage				0.45			0.45	V	$V_{CC} = V_{CC}$ MIN I_{OL} = 5.8 mA
$V_{OH}1$	Output High Voltage (TTL)		2.4			2.4			V	$V_{CC} = V_{CC}$ MIN I_{OH} = −2.5 mA
$V_{OH}2$	Output High Voltage (CMOS)		0.85 V_{CC}			0.85 V_{CC}			V	$V_{CC} = V_{CC}$ MIN I_{OH} = −2.5 mA
			V_{CC} −0.4V			V_{CC} −0.4V				$V_{CC} = V_{CC}$ MIN I_{OH} = −100 µA
V_{PPLK}	V_{PP} Lock-Out Voltage	3	0.0		1.5	0.0		1.5	V	Complete Write Protection
$V_{PPH}1$	V_{PP} (Program/Erase Operations)		4.5		5.5	4.5		5.5	V	V_{PP} at 5V
$V_{PPH}2$	V_{PP} (Program/Erase Operations)		11.4		12.6	11.4		12.6	V	V_{PP} at 12V
V_{LKO}	V_{CC} Erase/Write Lock Voltage	8	2.0			2.0			V	
V_{HH}	RP# Unlock Voltage		11.4		12.6	11.4		12.6	V	Boot Block Write/Erase

NOTES:
1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, T = 25°C. These currents are valid for all product versions (packages and speeds).
2. I_{CCES} is specified with the device deselected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Block erases and word/byte writes are inhibited when $V_{PP} = V_{PPLK}$, and not guaranteed in the range between $V_{PPH}1$ and V_{PPLK}.
4. Sampled, not 100% tested.
5. Automatic Power Savings (APS) reduces I_{CCR} to less than 1 mA typical, in static operation.
6. CMOS Inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL Inputs are either V_{IL} or V_{IH}.
7. For the 28F002, address pin A_{10} follows the C_{OUT} capacitance numbers.
8. For all BV parts, V_{LKO} = 2.0V for both 3.3V and 5V operations.

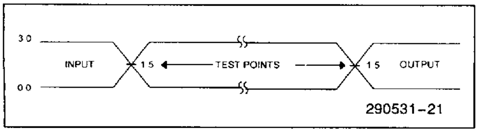
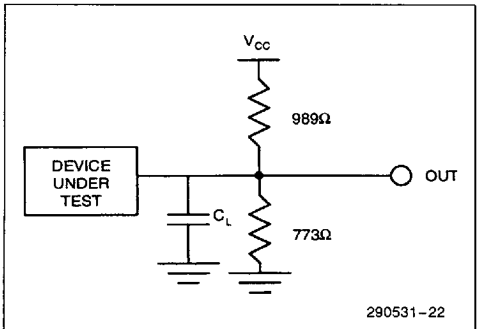


Figure 13. 3.3V Inputs and Measurement Points



NOTE:
C_L = 50 pF, includes Jig Capacitance

Figure 14. 3.3V Standard Test Configuration

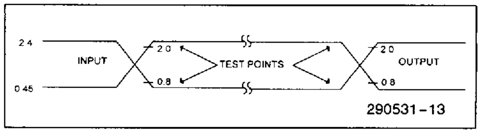
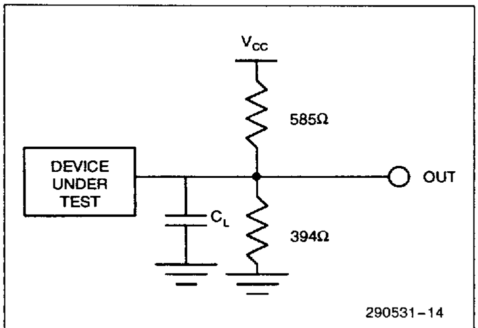
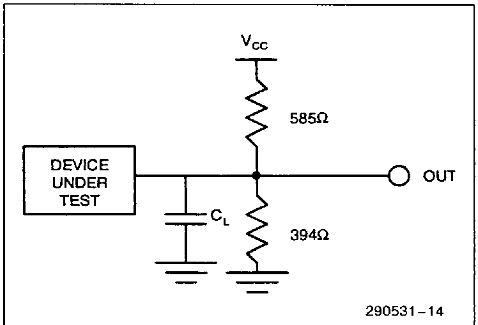


Figure 15. 5V Inputs and Measurement Points



NOTE:
C_L = 100 pF, includes Jig Capacitance

Figure 16. 5V Standard Test Configuration



NOTE:
C_L = 30 pF, includes Jig Capacitance

Figure 17. 5V High Speed Test Configuration

5.3 AC Characteristics

Table 14. AC Characteristics: Read Only Operations (Commercial)

			BV-60						
		V_{CC}	5V ± 5%		5V ± 10%		3.3 ± 0.3V		
		Load	30 pF		100 pF		50 pF		
Symbol	Parameter	Note	Min	Max	Min	Max	Min	Max	Units
t_{AVAV}	Read Cycle Time		60		70		110		ns
t_{AVQV}	Address to Output Delay			60		70		110	ns
t_{ELQV}	CE# to Output Delay	2		60		70		110	ns
t_{PHQV}	RP# to Output Delay			450		450		800	ns
t_{GLQV}	OE# to Output Delay	2		30		35		65	ns
t_{ELQX}	CE# to Output in Low Z	3	0		0		0		ns
t_{EHQZ}	CE# to Output in High Z	3		20		25		55	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		0		ns
t_{GHQZ}	OE# to Output in High Z	3		20		25		45	ns
t_{OH}	Output Hold from Address CE#, or OE# change whichever occurs first	3	0		0		0		ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE# High or Low	3		5		5		7	ns
t_{AVFL}	Address to BYTE# High or Low	3		5		5		7	ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3,4		60		70		110	ns
t_{FLQZ}	BYTE# Low to Output in High Z	3		20		25		45	ns

5.3 AC Characteristics

Table 14. AC Characteristics: Read Only Operations (Commercial) (Continued)

			BV-80				BV-120				
		V_{CC}	5V ± 10%		3.3 ± 0.3V		5V ± 10%		3.3 ± 0.3V		
		Load	100 pF		50 pF		100 pF		50 pF		
Symbol	**Parameter**	**Note**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{AVAV}	Read Cycle Time		80		150		120		180		ns
t_{AVQV}	Address to Output Delay			80		150		120		180	ns
t_{ELQV}	CE# to Output Delay	2		80		150		120		180	ns
t_{PHQV}	RP# to Output Delay			450		800		450		800	ns
t_{GLQV}	OE# to Output Delay	2		40		90		40		90	ns
t_{ELQX}	CE# to Output in Low Z	3	0		0		0		0		ns
t_{EHQZ}	CE# to Output in High Z	3		30		80		30		80	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		0		0		ns
t_{GHQZ}	OE# to Output in High Z	3		30		60		30		60	ns
t_{OH}	Output Hold from Address CE#, or OE# change whichever occurs first	3	0		0		0		0		ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE# High or Low	3		5		10		5		10	ns
t_{AVFL}	Address to BYTE# High or Low	3		5		10		5		10	ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3,4		80		150		120		180	ns
t_{FLQZ}	BYTE# Low to Output in High Z	3		30		60		30		60	ns

NOTES:
1. See AC Input/Output Reference Waveform for timing measurements.
2. OE# may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of CE# without impact on t_{CE}.
3. Sampled, but not 100% tested.
4. t_{FLQV}, BYTE# switching low to valid output delay will be equal to t_{AVQV}, measured from the time DQ_{15}/A_{-1} becomes valid.
5. See 5V High Speed Test Configuration.
6. See 5V Standard Test Configuration.
7. See 3.3V Test Configuration

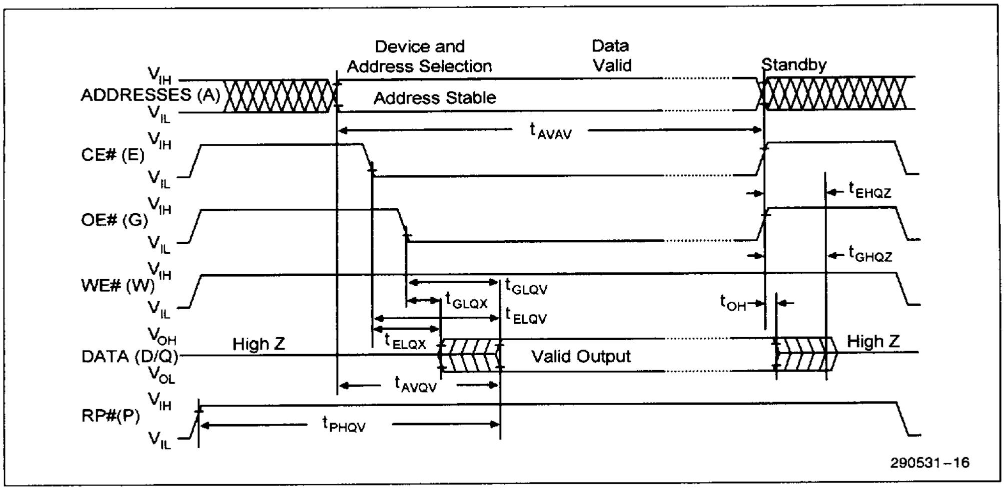


Figure 18. AC Waveforms for Read Operations

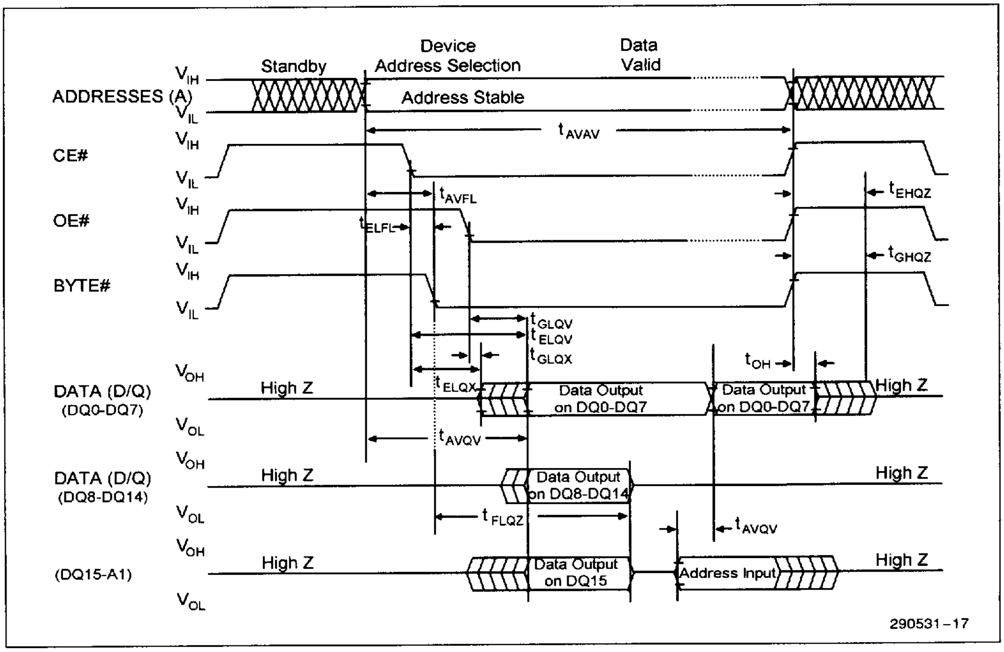


Figure 19. BYTE# Timing Diagram for Both Read and Write Operations with V_{CC} at 5.0V

Table 15. AC Characteristics: WE#—Controlled Write Operations(1) (Commercial)

		V_{CC}	BV-60						
			5V ± 5%		5V ± 10%		3.3 ± 0.3V		
		Load	30 pF		100 pF		50 pF		
Symbol	Parameter	Note	Min	Max	Min	Max	Min	Max	Units
t_{AVAV}	Write Cycle Time		60		70		110		ns
t_{PHWL}	RP# Setup to WE# Going Low		450		450		800		ns
t_{ELWL}	CE# Setup to WE# Going Low		0		0		0		ns
t_{PHHWH}	Boot Block Lock Setup to WE# Going High	6,8	100		100		200		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	5,8	100		100		200		ns
t_{AVWH}	Address Setup to WE# Going High	3	50		50		90		ns
t_{DVWH}	Data Setup to WE# Going High	4	50		50		90		ns
t_{WLWH}	WE# Pulse Width		50		50		90		ns
t_{WHDX}	Data Hold Time from WE# High	4	0		0		0		ns
t_{WHAX}	Address Hold Time from WE# High	3	10		10		10		ns
t_{WHEH}	CE# Hold Time from WE# High		0		0		0		ns
t_{WHWL}	WE# Pulse Width High		10		20		20		ns
t_{WHQV1}	Duration of Word/Byte Programming Operation	2,5	6		6		6		μs
t_{WHQV2}	Duration of Erase Operation (Boot)	2,5,6	0.3		0.3		0.3		s
t_{WHQV3}	Duration of Erase Operation (Parameter)	2,5	0.3		0.3		0.3		s
t_{WHQV4}	Duration of Erase Operation (Main)	2,5	0.6		0.6		0.6		s
t_{QWL}	V_{PP} Hold from Valid SRD	5,8	0		0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD	6,8	0		0		0		ns
t_{PHBR}	Boot-Block Relock Delay	7,8		100		100		200	ns

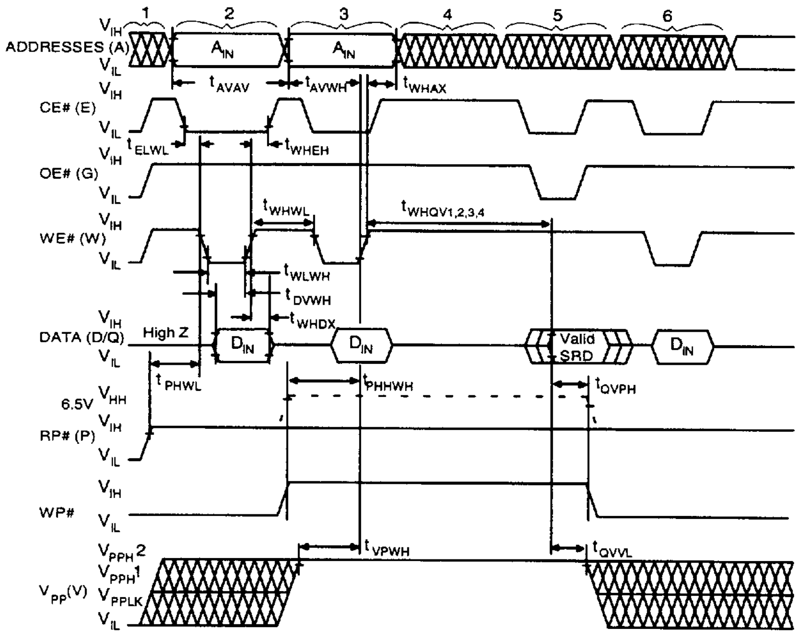
Table 15. AC Characteristics: WE#—Controlled Write Operations(1) (Commercial) (Continued)

			BV-80				BV-120				
		V_{CC}	5V ± 10%		3.3 ± 0.3V		5V ± 10%		3.3 ± 0.3V		
		Load	100 pF		50 pF		100 pF		50 pF		
Symbol	**Parameter**	**Note**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{AVAV}	Write Cycle Time		80		150		120		180		ns
t_{PHWL}	RP# Setup to WE# Going Low		450		1000		450		1000		ns
t_{ELWL}	CE# Setup to WE# Going Low		0		0		0		0		ns
t_{PHHWH}	Boot Block Lock Setup to WE# Going High	6,8	100		200		100		200		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	5,8	100		200		100		200		ns
t_{AVWH}	Address Setup to WE# Going High	3	50		120		50		150		ns
t_{DVWH}	Data Setup to WE# Going High	4	50		120		50		150		ns
t_{WLWH}	WE# Pulse Width		50		120		50		150		ns
t_{WHDX}	Data Hold Time from WE# High	4	0		0		0		0		ns
t_{WHAX}	Address Hold Time from WE# High	3	10		10		10		10		ns
t_{WHEH}	CE# Hold Time from WE# High		0		0		0		0		ns
t_{WHWL}	WE# Pulse Width High		30		30		30		30		ns
t_{WHQV1}	Duration of Word/Byte Programming Operation	2,5	6		6		6		6		µs
t_{WHQV2}	Duration of Erase Operation (Boot)	2,5,6	0.3		0.3		0.3		0.3		s
t_{WHQV3}	Duration of Erase Operation (Parameter)	2,5	0.3		0.3		0.3		0.3		s
t_{WHQV4}	Duration of Erase Operation (Main)	2,5	0.6		0.6		0.6		0.6		s
t_{QWL}	V_{PP} Hold from Valid SRD	5,8	0		0		0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD	6,8	0		0		0		0		ns
t_{PHBR}	Boot-Block Relock Delay	7,8		100		200		100		200	ns

4826175 0157734 630

NOTES:

1. Read timing characteristics during write and erase operations are the same as during read-only operations. Refer to AC characteristics during read mode.
2. The on-chip WSM completely automates Program/Erase operations; Program/Erase algorithms are now controlled internally which includes verify and margining operations.
3. Refer to command definition table for valid A_{IN}.
4. Refer to command definition table for valid D_{IN}.
5. Program/Erase durations are measured to valid SRD data (successful operation, SR.7 = 1).
6. For boot block program/erase, RP# should be held at V_{HH} or WP# should be held at V_{IH} until operation completes successfully.
7. Time t_{PHBR} is required for successful relocking of the boot block.
8. Sampled, but not 100% tested.
9. V_{PP} at 5.0V.
10. V_{PP} at 12.0V.
11. See 5V High Speed Test Configuration.
12. See 5V Standard Test Configuration.
13. See 3.3V Test Configuration.



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NOTES:

1. V_{CC} Power-Up and Standby.
2. Write program or Erase Setup Command.
3. Write Valid Address and Data (Program) or Erase Confirm Command.
4. Automated Program or Erase Delay.
5. Read Status Register Data.
6. Write Read Array Command.

Figure 20. AC Waveforms for Write and Erase Operations (WE#-Controlled Writes)

Table 16. AC Characteristics: CE#-Controlled Write Operations(1,13) (Commercial)

			BV-60						
		V_{CC}	5V ± 5%		5V ± 10%		3.3 ± 0.3V		
		Load	30 pF		100 pF		50 pF		
Symbol	Parameter	Note	Min	Max	Min	Max	Min	Max	Units
t_{AVAV}	Write Cycle Time		60		70		110		ns
t_{PHEL}	RP# High Recovery to CE# Going Low		450		450		1000		ns
t_{WLEL}	WE# Setup to CE# Going Low		0		0		0		ns
t_{PHHEH}	Boot Block Lock Setup to CE# Going High	6,8	100		100		200		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	5,8	100		100		200		ns
t_{AVEH}	Address Setup to CE# Going High	3	50		50		90		ns
t_{DVEH}	Data Setup to CE# Going High	4	50		50		90		ns
t_{ELEH}	CE# Pulse Width		50		50		90		ns
t_{EHDX}	Data Hold Time from CE# High	4	0		0		0		ns
t_{EHAX}	Address Hold Time from CE# High	3	10		10		10		ns
t_{EHWH}	WE # Hold Time from CE# High		0		0		0		ns
t_{EHEL}	CE# Pulse Width High		10		20		20		ns
t_{EHQV1}	Duration of Word/Byte Programming Operation	2,5	6		6		6		μs
t_{EHQV2}	Duration of Erase Operation (Boot)	2,5,6	0.3		0.3		0.3		s
t_{EHQV3}	Duration of Erase Operation (Parameter)	2,5	0.3		0.3		0.3		s
t_{EHQV4}	Duration of Erase Operation (Main)	2,5	0.6		0.6		0.6		s
t_{QWL}	V_{PP} Hold from Valid SRD	5,8	0		0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD	6,8	0		0		0		ns
t_{PHBR}	Boot-Block Relock Delay	7,8		100		100		200	ns

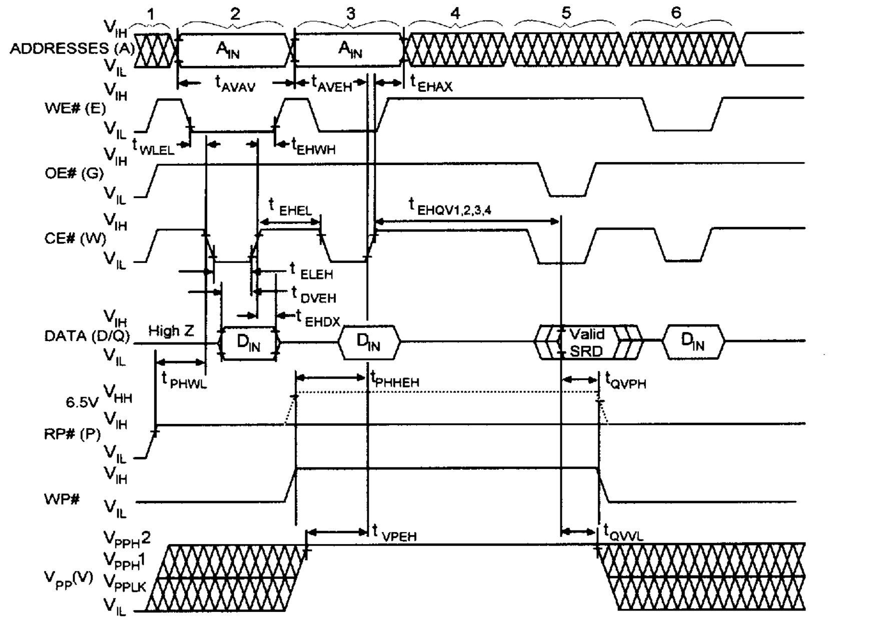
Table 16. AC Characteristics: CE#-Controlled Write Operations(1,13) (Commercial) (Continued)

			BV-80				BV-120				
		V_{CC}	5V ± 10%		3.3V ± 0.3V		5V ± 10%		3.3V ± 0.3V		
		Load	100 pF		50 pF		100 pF		50 pF		
Symbol	**Parameter**	**Note**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{AVAV}	Write Cycle Time		80		150		120		180		ns
t_{PHEL}	RP# High Recovery to CE# Going Low		450		1000		450		1000		ns
t_{WLEL}	WE# Setup to CE# Going Low		0		0		0		0		ns
t_{PHHEH}	Boot Block Lock Setup to CE# Going High	6,8	100		200		100		200		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	5,8	100		200		100		200		ns
t_{AVEH}	Address Setup to CE# Going High	3	50		120		50		150		ns
t_{DVEH}	Data Setup to CE# Going High	4	50		120		50		150		ns
t_{ELEH}	CE# Pulse Width		50		120		50		150		ns
t_{EHDX}	Data Hold Time from CE# High	4	0		0		0		0		ns
t_{EHAX}	Address Hold Time from CE# High	3	10		10		10		10		ns
t_{EHWH}	WE # Hold Time from CE# High		0		0		0		0		ns
t_{EHEL}	CE# Pulse Width High		30		30		30		30		ns
t_{EHQV1}	Duration of Word/ Byte Programming Operation	2,5	6		6		6		6		μs
t_{EHQV2}	Duration of Erase Operation (Boot)	2,5,6	0.3		0.3		0.3		0.3		s
t_{EHQV3}	Duration of Erase Operation (Parameter)	2,5	0.3		0.3		0.3		0.3		s
t_{EHQV4}	Duration of Erase Operation (Main)	2,5	0.6		0.6		0.6		0.6		s
t_{QWL}	V_{PP} Hold from Valid SRD	5,8	0		0		0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD	6,8	0		0		0		0		ns
t_{PHBR}	Boot-Block Relock Delay	7,8		100		200		100		200	ns

NOTES:

See WE# Controlled Write Operations for notes 1 through 12.

13. Chip-Enable controlled writes: Write operations are driven by the valid combination of CE# and WE# in systems where CE# defines the write pulse-width (within a longer WE# timing waveform), all set-up, hold and inactive WE# times should be measured relative to the CE# waveform.



NOTES:
1. V_{CC} Power-Up and Standby.
2. Write program or Erase Setup Command.
3. Write Valid Address and Data (Program) or Erase Confirm Command.
4. Automated Program or Erase Delay.
5. Read Status Register Data.
6. Write Read Array Command.

Figure 21. Alternate AC Waveforms for Write and Erase Operations (CE#—Controlled Writes)

Table 17. Erase and Program Timings (Commercial T_A = 0°C to +70°C)

Parameter	V_{PP} = 5V ±10%		V_{PP} = 12V ±5%		Units
	V_{CC} = 3.3 ±0.3V	V_{CC} = 5V ±10%	V_{CC} = 3.3V ±0.3V	V_{CC} = 5V ±10%	
	Typ	Typ	Typ	Typ	
Boot/Parameter Block Erase Time	0.84	0.8	0.44	0.34	s
Main Block Erase Time	2.4	1.9	1.3	1.1	s
Main Block Write Time (Byte Mode)	1.7	1.8	1.6	1.2	s
Main Block Write Time (Word Mode)	1.1	0.9	0.8	0.6	s
Byte Write Time	10	10	8	8	µs
Word Write Time	13	13	8	8	µs

NOTES:
1. All numbers are sampled, not 100% tested.
2. Contact your Intel representative for information regarding maximum Byte/Word Write specifications.

6.0 EXTENDED OPERATING CONDITIONS

Table 18. Extended Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Notes	Min	Max	Units
T_A	Operating Temperature		−40	85	°C
V_{CC}	3.3V V_{CC} Supply Voltage (±0.3V)	1	3.0	3.6	Volts
	5V V_{CC} Supply Voltage (10%)	2	4.50	5.50	Volts

NOTES:
1. AC specifications are valid at both voltage ranges. See DC Characteristics tables for voltage range-specific specifications.
2. 10% V_{CC} specifications apply to 110 ns and 80 ns versions in their standard test configuration.

6.1 Applying V_{CC} Voltages

Table 19. V_{CC} Supply Switching Timing

Symbol	Parameter	Notes	Min	Max	Units
T_{5VPH}	V_{CC} at 4.5V (minimum) to RP# High	1	2		μs
T_{3VPH}	V_{CC} at 3.0V (minimum) to RP# High	1	2		μs

NOTES:
1. The T_{5VPH} and/or T_{3VPH} times must be strictly followed to guarantee all other read and write specifications.
2. To switch between 3.3V and 5.0V operation, the system should first transition V_{CC} from the existing voltage to GND, and then to the new voltage. The V_{CC} supply voltage should not be switched when the WSM is busy.

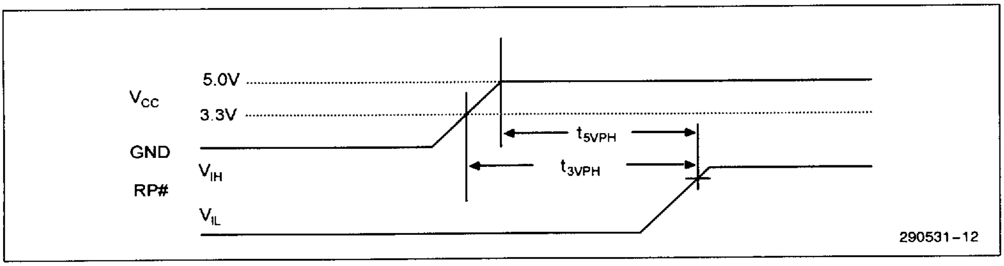


Figure 22. V_{CC} Supply Switching Waveform

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6.2 DC Characteristics

Table 20. DC Characteristics: Extended Temperature Operation

Symbol	Parameter	Notes	TBV-80 $V_{CC} = 3.3 \pm 0.3V$			TBV-80 $V_{CC} = 5V \pm 10\%$			Units	Test Conditions
			Min	Typ	Max	Min	Typ	Max		
I_{IL}	Input Load Current	1			± 1.0			± 1.0	μA	$V_{CC} = V_{CC}MAX$ $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1			± 10			± 10	μA	$V_{CC} = V_{CC}$ MAX $V_{IN} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1,3		0.4	1.5		0.8	2.5	mA	$V_{CC} = V_{CC}MAX$ CE# = RP# = BYTE# = V_{IH}
				60	110		70	150	μA	$V_{CC} = V_{CC}MAX$ CE# = RP# = WP# = $V_{CC} \pm 0.2V$
I_{CCD}	V_{CC} Deep Power-Down Current	1		0.2	8		0.2	8	μA	$V_{CC} = V_{CC}MAX$ $V_{IN} = V_{CC}$ or GND RP# = GND ± 0.2V
I_{CCR}	V_{CC} Read Current for Word or Byte	1,5,6		15	30		50	65	mA	**CMOS INPUTS** $V_{CC} = V_{CC}MAX$ CE# = GND OE# = V_{CC} f = 10 MHz (5V), 5 MHz (3.3V) I_{OUT} = 0 mA Inputs = GND ± 0.2V or $V_{CC} \pm 0.2V$
				15	30		55	70	mA	**TTL INPUTS** $V_{CC} = V_{CC}MAX$ CE# = V_{IL} OE# = V_{IH} f = 10 MHz (5V), 5 MHz (3.3V) I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH}
I_{CCW}	V_{CC} Write Current for Word or Byte	1,4		13	30		30	50	mA	Word/Byte Program in Progress $V_{PP} = V_{PPH}1$ (at 5V)
				10	25		30	45	mA	Word/Byte Program in Progress $V_{PP} = V_{PPH}2$ (at 12V)

Table 20. DC Characteristics: Extended Temperature Operation (Continued)

Symbol	Parameter	Notes	TBV-80 $V_{CC} = 3.3 \pm 0.3V$ Min	Typ	Max	TBV-80 $V_{CC} = 5V \pm 10\%$ Min	Typ	Max	Units	Test Conditions
I_{CCE}	V_{CC} Erase Current	1,4		13	30		22	45	mA	Block Erase in Progress $V_{PP} = V_{PPH}1$ (at 5V)
				10	25		18	40	mA	Block Erase in Progress $V_{PP} = V_{PPH}2$ (at 12V)
I_{CCES}	V_{CC} Erase Suspend Current	1,2		3	8.0		5	12.0	mA	CE# = V_{IH} Block Erase Suspend $V_{PP} = V_{PPH}1$ (at 5V)
I_{PPS}	V_{PP} Standby Current	1		± 5	± 15		± 5	± 15	μA	$V_{PP} \leq V_{CC}$
I_{PPD}	V_{PP} Deep Power-down Current	1		0.2	10		0.2	10	μA	RP# = GND ± 0.2V
I_{PPR}	V_{PP} Read Current	1		50	200		50	200	μA	$V_{PP} > V_{CC}$
I_{PPW}	V_{PP} Write Current for Word/Byte	1,4		13	30		13	30	mA	$V_{PP} = V_{PPH}$ Word Write in Progress $V_{PP} = V_{PPH}1$ (at 5V)
				8	25		8	25	mA	$V_{PP} = V_{PPH}$ Word Write in Progress $V_{PP} = V_{PPH}2$ (at 12V)
I_{PPE}	V_{PP} Erase Current	1,4		13	30		15	25	mA	$V_{PP} = V_{PPH}$ Block Erase in Progress $V_{PP} = V_{PPH}1$ (at 5V)
				8	25		10	20	mA	$V_{PP} = V_{PPH}$ Block Erase in Progress $V_{PP} = V_{PPH}2$ (at 12V)
I_{PPES}	V_{PP} Erase Suspend Current	1		50	200		50	200	μA	$V_{PP} = V_{PPH}$ Block Erase Suspend in Progress

Table 20. DC Characteristics: Extended Temperature Operation (Continued)

Symbol	Parameter	Notes	TBV-80 $V_{CC} = 3.3 \pm 0.3V$ Min	Typ	Max	TBV-80 $V_{CC} = 5V \pm 10\%$ Min	Typ	Max	Units	Test Conditions
$I_{RP\#}$	RP# Boot Block Unlock Current	1,4			500			500	µA	RP# = V_{HH} V_{PP} = 12V
I_{ID}	A_9 Intelligent Identifier Current	1,4			500			500	µA	A_9 = V_{ID}
V_{ID}	A_9 Intelligent Identifier Voltage		11.4		12.6	11.4		12.6	V	
V_{IL}	Input Low Voltage		−0.5		0.8	−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} ± 0.5V	2.0		V_{CC} ± 0.5V	V	
V_{OL}	Output Low Voltage				0.45			0.45	V	V_{CC} = V_{CC}MIN I_{OL} = 5.8 mA (5V) 2 mA (3.3V) V_{PP} = 12V
$V_{OH}1$	Output High Voltage (TTL)		2.4			2.4			V	V_{CC} = V_{CC}MIN I_{OH} = −2.5 mA
$V_{OH}2$	Output High Voltage (CMOS)		0.85 × V_{CC}			0.85 × V_{CC}			V	V_{CC} = V_{CC}MIN I_{OH} = −2.5 mA
			V_{CC} − 0.4V			V_{CC} − 0.4V				V_{CC} = V_{CC}MIN I_{OH} = −100 µA
V_{PPLK}	V_{PP} Lock-Out Voltage	3	0.0		1.5	0.0		1.5	V	Complete Write Protection
$V_{PPH}1$	V_{PP} (Program/ Erase Operations)		4.5		5.5	4.5		5.5	V	V_{PP} at 5V
$V_{PPH}2$	V_{PP} (Program/ Erase Operations)		11.4		12.6	11.4		12.6	V	V_{PP} at 12V

Table 20. DC Characteristics: Extended Temperature Operation (Continued)

Symbol	Parameter	Notes	TBV-80 V_{CC} = 3.3 ± 0.3V			TBV-80 V_{CC} = 5V ± 10%			Units	Test Conditions
			Min	Typ	Max	Min	Typ	Max		
V_{LKO}	V_{CC} Erase/Write Lock Voltage	10	2.0			2.0			V	V_{PP} = 12V
V_{HH}	RP# Unlock Voltage		11.4		12.6	11.4		12.6	V	Boot Block Write/Erase V_{PP} = 12V

NOTES:
1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, T = 25°C. These currents are valid for all product versions (packages and speeds).
2. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Block erases and word/byte writes are inhibited when V_{PP} = V_{PPLK}, and not guaranteed in the range between $V_{PPH}1$ and V_{PPLK}.
4. Sampled, not 100% tested.
5. Automatic Power Savings (APS) reduces I_{CCR} to less than 1 mA typical, in static operation.
6. CMOS Inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL Inputs are either V_{IL} or V_{IH}.
7. For the 28F002 address pin A_{10} follows the C_{OUT} capacitance numbers.
8. For all BV parts, V_{LKO} = 2.0V for both 3.3V and 5.0V operations.

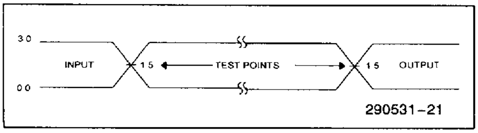


Figure 23. 3.3V Inputs and Measurement Points

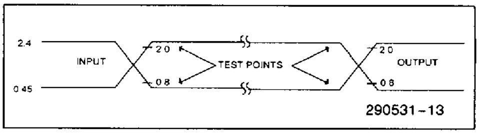
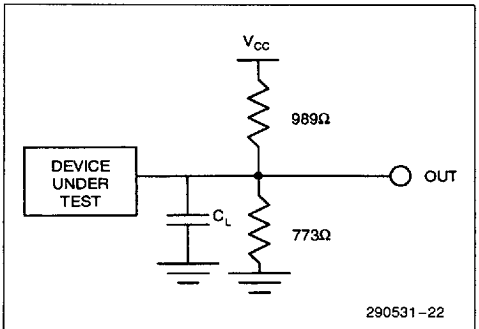
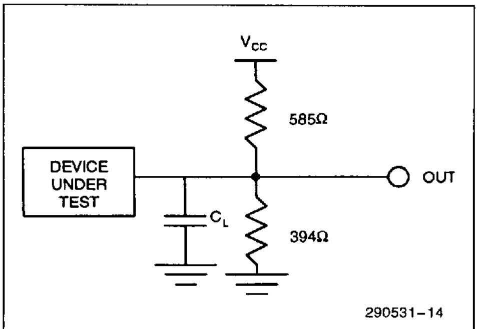


Figure 25. 5V Inputs and Measurement Points



NOTE:
C_L = 50 pF, includes Jig Capacitance

Figure 24. 3.3V Standard Test Configuration



NOTE:
C_L = 100 pF, includes Jig Capacitance

Figure 26. 5V Standard Test Configuration

6.3 AC Characteristics

Table 21. AC Characteristics: Read Only Operations(1) (Extended Temperature)

Symbol	Parameter	Note	TBV-80 $V_{CC} = 3.3 \pm 0.3V^{(6)}$		TBV-80 $V_{CC} = 5V \pm 10\%^{(5)}$		Units
			Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time		110		80		ns
t_{AVQV}	Address to Output Delay			110		80	ns
t_{ELQV}	CE# to Output Delay	2		110		80	ns
t_{PHQV}	RP# to Output Delay			800		450	ns
t_{GLQV}	OE# to Output Delay	2		65		40	ns
t_{ELQX}	CE# to Output in Low Z	3	0		0		ns
t_{EHQZ}	CE# to Output in High Z	3		55		30	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		ns
t_{GHQZ}	OE# to Output in High Z	3		45		30	ns
t_{OH}	Output Hold from Address CE#, or OE# change whichever occurs first	3	0		0		ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE# High or Low	3		7		5	ns
t_{AVFL}	Address to BYTE# High or Low	3		7		5	ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3,4		110		80	ns
t_{FLQZ}	BYTE# Low to Output in High Z	3		45		30	ns

NOTES:
1. See AC Input/Output Reference Waveform for timing measurements.
2. OE# may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of CE# without impact on t_{CE}.
3. Sampled, but not 100% tested.
4. t_{FLQV}, BYTE# switching low to valid output delay will be equal to t_{AVQV}, measured from the time DQ_{15}/A_{-1} becomes valid.
5. See 5V Standard Test Configuration.
6. See 3.3V Standard Test Configuration.

Table 22. AC Characteristics: WE#-Controlled Write Operations(1) (Extended Temperature)

Symbol	Parameter	Notes	TBV-80		TBV-80		Units
			V_{CC} = 3.3 ± 0.3V(11)		V_{CC} = 5V ± 10%(12)		
			Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time		110		80		ns
t_{PHWL}	RP# High Recovery to WE# Going Low		800		450		ns
t_{ELWL}	CE# Setup to WE# Going Low		0		0		ns
t_{PHHWH}	Boot Block Lock Setup to WE# Going High	6,8	200		100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	5,8	200		100		ns
t_{AVWH}	Address Setup to WE# Going High	3	90		60		ns
t_{DVWH}	Data Setup to WE# Going High	4	90		60		ns
t_{WLWH}	WE# Pulse Width		90		60		ns
t_{WHDX}	Data Hold Time from WE# High	4	0		0		ns
t_{WHAX}	Address Hold Time from WE# High	3	10		10		ns
t_{WHEH}	CE# Hold Time from WE# High		0		0		ns
t_{WHWL}	WE# Pulse Width High		20		20		ns
t_{WHQV1}	Duration of Word/Byte Write Operation	2,5	6		7		µs
t_{WHQV2}	Duration of Erase Operation (Boot)	2,5,6	0.3		0.4		s
t_{WHQV3}	Duration of Erase Operation (Parameter)	2,5	0.3		0.4		s
t_{WHQV4}	Duration of Erase Operation (Main)	2,5	0.6		0.7		s

Table 22. AC Characteristics: WE#-Controlled Write Operations[1] (Extended Temperature) (Continued)

Symbol	Parameter	Notes	TBV-80		TBV-80		Units
			$V_{CC} = 3.3 \pm 0.3V$[11]		$V_{CC} = 5V \pm 10\%$[12]		
			Min	Max	Min	Max	
t_{QWL}	V_{PP} Hold from Valid SRD	5,8	0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD	6,8	0		0		ns
t_{PHBR}	Boot-Block Relock Delay	7,8		200		100	ns

NOTES:
1. Read timing characteristics during write and erase operations are the same as during read-only operations. Refer to AC Characteristics during read mode.
2. The on-chip WSM completely automates program/erase operations; program/erase algorithms are now controlled internally which includes verify and margining operations.
3. Refer to command definition table for valid A_{IN}.
4. Refer to command definition table for valid D_{IN}.
5. Program/Erase durations are measured to valid SRD data (successful operation, SR.7 = 1)
6. For boot block program/erase, RP# should be held at V_{HH} or WP# should be held at V_{IH} until operation completes successfully.
7. Time t_{PHBR} is required for successful relocking of the boot block.
8. Sampled, but not 100% tested.
9. V_{PP} at 5.0V.
10. V_{PP} at 12.0V.
11. See 3.3V Standard Test Configuration.
12. See 5V Standard Test Configuration.

Table 23. AC Characteristics: CE#-Controlled Write Operations(1,13)

Symbol	Parameter	Notes	TBV-80 V_{CC} = 3.3 ± 0.3V(11)		TBV-80 V_{CC} = 5V ± 10%(12)		Units
			Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time		110		80		ns
t_{PHEL}	RP# High Recovery to CE# Going Low		800		450		ns
t_{WLEL}	WE# Setup to CE# Going Low		0		0		ns
t_{PHHEH}	Boot Block Lock Setup to CE# Going High	6,8	200		100		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	5,8	200		100		ns
t_{AVEH}	Address Setup to CE# Going High		90		60		ns
t_{DVEH}	Data Setup to CE# Going High	3	90		60		ns
t_{ELEH}	CE# Pulse Width	4	90		60		ns
t_{EHDX}	Data Hold Time from CE# High		0		0		ns
t_{EHAX}	Address Hold Time from CE# High	4	10		10		ns
t_{EHWH}	WE# Hold Time from CE# High	3	0		0		ns
t_{EHEL}	CE# Pulse Width High		20		20		ns
t_{EHQV1}	Duration of Word/Byte Write Operation	2,5	6		7		µs
t_{EHQV2}	Duration of Erase Operation (Boot)	2,5,6	0.3		0.4		s
t_{EHQV3}	Duration of Erase Operation (Parameter)	2,5	0.3		0.4		s
t_{EHQV4}	Duration of Erase Operation (Main)	2,5	0.6		0.7		s
t_{QWL}	V_{PP} Hold from Valid SRD	5,8	0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD	6,8	0		0		ns
t_{PHBR}	Boot-Block Relock Delay	7,8		200		100	ns

NOTES:

See WE# Controlled Write Operations for notes 1 through 12.

13. Chip-Enable controlled writes: Write operations are driven by the valid combination of CE# and WE# in systems where CE# defines the write pulse-width (within a longer WE# timing waveform), all set-up, hold and inactive WE# times should be measured relative to the CE# waveform.

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Table 24. Extended Temperature Operations—Erase and Program Timings

Parameter	V_{PP} = 5V ± 10%		V_{PP} = 12V ± 5%		Units
	V_{CC} = 3.3 ± 0.3V	V_{CC} = 5V ± 10%	V_{CC} = 3.3 ± 0.3V	V_{CC} = 5V ± 10%	
	Typ	Typ	Typ	Typ	
Boot/Parameter Block Erase Time	0.84	0.8	0.44	0.34	s
Main Block Erase Time	2.4	1.9	1.3	1.1	s
Main Block Write Time (Byte Mode)	1.7	1.4	1.6	1.2	s
Main Block Write Time (Word Mode)	1.1	0.9	0.8	0.6	s
Byte Write Time	10	10	8	8	µs
Word Write Time	13	13	8	8	µs

NOTES:
1. All numbers are sampled, not 100% tested.
2. Contact your Intel representative for information regarding maximum Byte/Word Write specifications.

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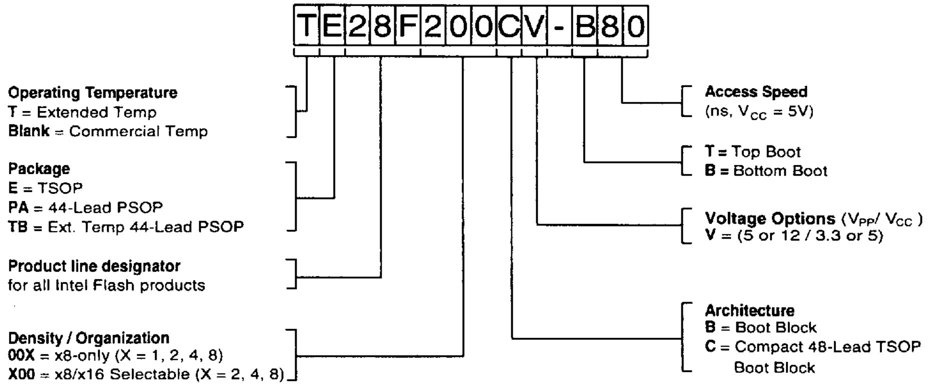
7.0 ADDITIONAL INFORMATION

7.1 Ordering Information



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VALID COMBINATIONS:

	40-Lead TSOP	44-Lead PSOP	48-Lead TSOP	56-Lead TSOP
Commercial	E28F002BVT60	PA28F200BVT60	E28F200CVT60	E28F200BVT60
	E28F002BVB60	PA28F200BVB60	E28F200CVB60	E28F200BVB60
	E28F002BVT80	PA28F200BVT80	E28F200CVT80	E28F200BVT80
	E28F002BVB80	PA28F200BVB80	E28F200CVB80	E28F200BVB80
	E28F002BVT120	PA28F200BVT120		
	E28F002BVB120	PA28F200BVB120		
Extended	TE28F002BVT80	TB28F200BVT80	TE28F200CVT80	TE28F200BVT80
	TE28F002BVB80	TB28F200BVB80	TE28F200CVB80	TE28F200BVB80

Table 25. Summary of Line Items

Name	V_{CC}		V_{PP}		40-Lead TSOP	44-Lead PSOP	48-Lead TSOP	56-Lead TSOP	0°–+70°C	−40°–+85°C
	3.3V	5V	5V	12V						
28F200BV	✓	✓	✓	✓		✓	✓	✓	✓	✓
28F002BV	✓	✓	✓	✓	✓				✓	✓

7.2 References

Order Number	Document
292130	AB-57 "Boot Block Architecture for Safe Firmware Updates"
292154	AB-60 "2/4/8-Mbit SmartVoltage Boot Block Flash Memory Family"
292098	AP-363 "Extended Flash BIOS Concepts for Portable Computers"
292148	AP-604 "Using Intel's Boot Block Flash Memory Parameter Blocks to Replace EEPROM"
290448	28F002/200BX-T/B 2-Mbit Boot Block Flash Memory Datasheet
290449	28F002/200BL-T/B 2-Mbit Low Power Boot Block Flash Memory Datasheet
290450	28F004/400BL-T/B 4-Mbit Low Power Boot Block Flash Memory Datasheet
290451	28F004/400BX-T/B 4-Mbit Boot Block Flash Memory Datasheet
290530	2-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet
290539	8-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet

7.3 Revision History

-001	Initial release of datasheet

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