2.7 V to 5.5 V, <100 µA, 8/10/12 Bit D/A with I2C Compatible Interface, tiny SC70 Package

Preliminary Technical Data

AD5602/12/22

FEATURES

Single 8/10/12-bit DAC, 2 LSB INL
6-lead SC70 package
Micropower operation: max 100 µA @ 5 V
Power-down to <100 nA @ 3 V
2.7 V to 5.5 V power supply
Guaranteed monotonic by design
Power-on-reset to 0 V with brownout detection
3 power-down functions
I²C® Compatible Serial Interface supports:
Standard (100KHz), Fast (400KHz) and High-Speed (3.4MHz) Modes
On-chip output buffer amplifier, rail-to-rail operation

APPLICATIONS

Process control
Data acquisition systems
Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources
Programmable attenuators

FUNCTIONAL BLOCK DIAGRAM

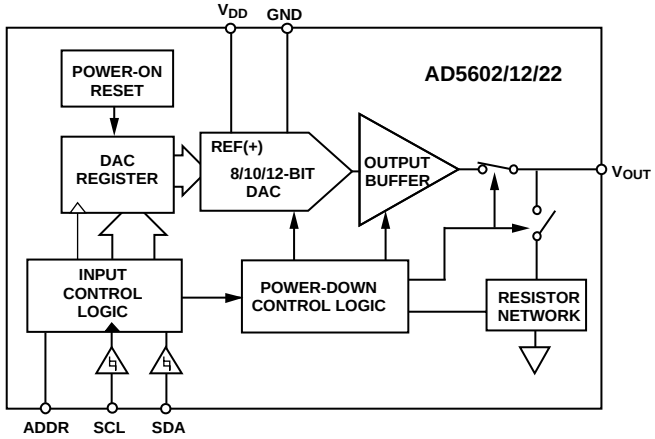

Figure 1

RELATED DEVICES

Part No.	Description
AD5601/11/21	2.7V to 5.5 V, <100µA, 8/10/12 Bit *nano*DAC™ D/A with SPI Interface in a tiny SC70 package

GENERAL DESCRIPTION

The AD5602/12/22, a member of the *nano*DAC™ D/A family is a single, 8/10/12-bit buffered voltage out DAC that operates from a single +2.7 V to +5.5 V supply consuming <100 µA at 5 V, and comes in a tiny SC70 package. Its on-chip precision output amplifier allows rail-to-rail output swing to be achieved. The AD5602/12/22 utilizes a 2-wire I²C compatible serial interface that operates in Standard (100 KHz), Fast (400 KHz) and High-Speed (3.4 MHz) Modes.

The reference for AD5602/12/22 is derived from the power supply inputs and thus gives the widest dynamic output range. The part incorporates a power-on-reset circuit that ensures the DAC output powers up to 0 V and remains there until a valid write takes place to the device. The part contains a power-down feature that reduces the current consumption of the device to <100 nA at 3 V and provides software selectable output loads while in power-down mode. The part is put into power-down mode over the serial interface. The low power consumption of this part in normal operation makes it ideally suited to portable battery operated equipment. The power consumption is 0.5 mW at 5 V.

PRODUCT HIGHLIGHTS

1. Available in 6-lead SC70.
2. Max 100µA power consumption, single-supply operation. This part operates from a single 2.7 V to 5.5 V supply and typically consumes 0.2 mW at 3 V and 0.5 mW at 5 V, making it ideal for battery-powered applications.
3. The on-chip output buffer amplifier allows the output of the DAC to swing rail-to-rail with a typical slew rate of 0.5 V/µs.
4. Reference derived from the power supply.
5. Standard, Fast and High-Speed Mode I²C interface.
6. Designed for very low power consumption.
7. Power-down capability. When powered down, the DAC typically consumes <100 nA at 3 V.
8. Brown out detection on power-on-reset.

Rev. PrB **18-Feb-05**

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REVISION HISTORY

Revision PrB 18-Feb-05 : Preliminary Version

AD5602/12/22—SPECIFICATIONS

Table 1. V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX} unless otherwise noted

	A,B,W,Y Version[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
STATIC PERFORMANCE					
Resolution				Bits	
AD5602	8				
AD5612	10				
AD5622	12				
Relative Accuracy[2]					
AD5602			±1	LSB	B,Y Versions
AD5612			±0.5	LSB	B,Y Versions
			±4	LSB	A Version
AD5622			±2	LSB	B,Y Versions
			±6	LSB	A,W versions
Differential Nonlinearity[2]			±1	LSB	Guaranteed Monotonic by Design.
Zero Code Error			TBD	LSB	All 0s Loaded to DAC Register.
Full-Scale Error			TBD	LSB	All 1s Loaded to DAC Register.
Gain Error			TBD	% of FSR	
Zero Code Error Drift		TBD		µV/°C	
Gain Temperature Coefficient		TBD		ppm of FSR/°C	
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0		V_{DD}	V	
Output Voltage Settling Time		8	18	µs	Code ¼ to ¾
Slew Rate		0.5		V/µs	
Capacitive Load Stability		470		pF	$R_L = \infty$
		1000		pF	RL = 2 kΩ
Output Noise Spectral Density		120		nV/Hz	DAC code=TBD , 10 kHz
Noise		TBD			DAC code=TBD 0.1-10Hz Bandwidth
Digital-to-Analog Glitch Impulse		10		nV-s	1 LSB Change Around Major Carry.
Digital Feedthrough		0.5		nV-s	
DC Output Impedance		1		Ω	
Short Circuit Current		20		mA	V_{DD} = +3V/+5 V
LOGIC INPUTS (SDA, SCL)					
I_{IN}, Input Current			±1	µA	
V_{INL}, Input Low Voltage			0.3(V_{DD})	V	
V_{INH}, Input High Voltage	0.7(V_{DD})			V	
C_{IN}, Pin Capacitance		3		pF	
V_{HYST}, Input Hysteresis	0.1(V_{DD})			V	
LOGIC OUTPUTS (OPEN DRAIN)					
V_{OL}, Output Low Voltage			0.4	V	I_{SINK} = 3 mA
			0.6	V	I_{SINK} = 6 mA
Floating-State Leakage Current			±1	µA	
Floating-State Output Capacitance			TBD	pF	
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
I_{DD} (Normal Mode)					DAC Active and Excluding Load Current
V_{DD} = +4.5 V to +5.5 V			100	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = +2.7 V to +3.6 V			70	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND

[1] Temperature ranges are as follows: A,B Version: –40°C to +125°C, typical at 25°C.
[2] Linearity calculated using a reduced code range 120-16179.
[3] Guaranteed by design and characterization, not production tested.

	A,B,W,Y Version[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
I_{DD} (All Power-Down Modes)					
V_{DD} = +4.5 V to +5.5 V		0.2	1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = +2.7 V to +3.6 V		0.05	1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
POWER EFFICIENCY					
I_{OUT}/I_{DD}		TBD		%	I_{LOAD} = 2 mA. V_{DD} = +5 V

I²C TIMING SPECIFICATIONS[4]

Table 2. V_{DD} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, f_{SCL} = 3.4 MHz unless otherwise noted. See Figure 2.

Parameter	Conditions	Limit at T_{MIN}, T_{MAX}		Unit	Description
		MIN	MAX		
f_{SCL}[5]	Standard Mode		100	KHz	Serial Clock Frequency
	Fast Mode		400	KHz	
	High-Speed Mode, C_B = 100pF		3.4	MHz	
	High-Speed Mode, C_B = 400pF		1.7	MHz	
t_1	Standard Mode	4		µS	t_{HIGH}, SCL High Time
	Fast Mode	0.6		µS	
	High-Speed Mode, C_B = 100pF	60		µS	
	High-Speed Mode, C_B = 400pF	120		µS	
t_2	Standard Mode	4.7		µS	t_{LOW}, SCL Low Time
	Fast Mode	1.3		µS	
	High-Speed Mode, C_B = 100pF	160		nS	
	High-Speed Mode, C_B = 400pF	320		nS	
t_3	Standard Mode	250		nS	$t_{SU;DAT}$, Data Setup Time
	Fast Mode	100		nS	
	High-Speed Mode	10		nS	
t_4	Standard Mode	0	3.45	µS	$t_{HD;DAT}$, Data Hold Time
	Fast Mode	0	0.9	µS	
	High-Speed Mode, C_B = 100pF	0	70	nS	
	High-Speed Mode, C_B = 400pF	0	150	nS	
t_5	Standard Mode	4.7		µS	$t_{SU;STA}$, Set-up Time for a repeated START Condition
	Fast Mode	0.6		µS	
	High-Speed Mode	160		nS	
t_6	Standard Mode	4		µS	$t_{HD;STA}$, Hold Time (repeated) START Condition
	Fast Mode	0.6		µS	
	High-Speed Mode	160		nS	
t_7	Standard Mode	4.7		µS	t_{BUF}, Bus Free Time Between a STOP and a START Condition
	Fast Mode	1.3		µS	
t_8	Standard Mode	4		µS	$t_{SU;STO}$, Set-up Time for a STOP Condition
	Fast Mode	0.6		µS	
	High-Speed Mode	160		nS	
t_9	Standard Mode	-	1000	nS	t_{RDA}, Rise Time of SDA Signal
	Fast Mode	20+0.1C_B	300	nS	
	High-Speed Mode, C_B = 100pF	10	80	nS	
	High-Speed Mode, C_B = 400pF	20	160	nS	
t_{10}	Standard Mode	-	300	nS	t_{FDA}, Fall Time of SDA Signal
	Fast Mode	20+0.1C_B	300	nS	
	High-Speed Mode, C_B = 100pF	10	80	nS	
	High-Speed Mode, C_B = 400pF	20	160	nS	
t_{11}	Standard Mode	-	1000	nS	t_{RCL}, Rise Time of SCL Signal
	Fast Mode	20+0.1C_B	300	nS	
	High-Speed Mode, C_B = 100pF	10	40	nS	
	High-Speed Mode, C_B = 400pF	20	80	nS	

[4] See Figure 2. HS-Mode timing specification applies to the AD5602/12/22-1 only. Standard and Fast-mode timing specifications apply to both the AD5602/12/22-1 and AD5602/12/22-2. C_B refers to the capacitance load on the bus line.

[5] The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate but has a negative effect on EMC behavior of the part.

Parameter	Conditions	Limit at Tmin, Tmax		Unit	Description
		MIN	MAX		
t_{11A}	Standard Mode	-	1000	nS	t_{RCL1}, Rise Time of SCL signal after a repeated START Condition and after an Acknowledge bit
	Fast Mode	20+0.1C_B	300	nS	
	High-Speed Mode, C_B = 100pF	10	80	nS	
	High-Speed Mode, C_B = 400pF	20	160	nS	
t_{12}	Standard Mode	-	300	nS	t_{FCL}, Fall Time of SCL Signal
	Fast Mode	20+0.1C_B	300	nS	
	High-Speed Mode, C_B = 100pF	10	40	nS	
	High-Speed Mode, C_B = 400pF	20	80	nS	
t_{SP}[6]	Fast Mode	0	50	nS	Pulsewidth of Spike Suppressed
	High-Speed Mode	0	10	nS	

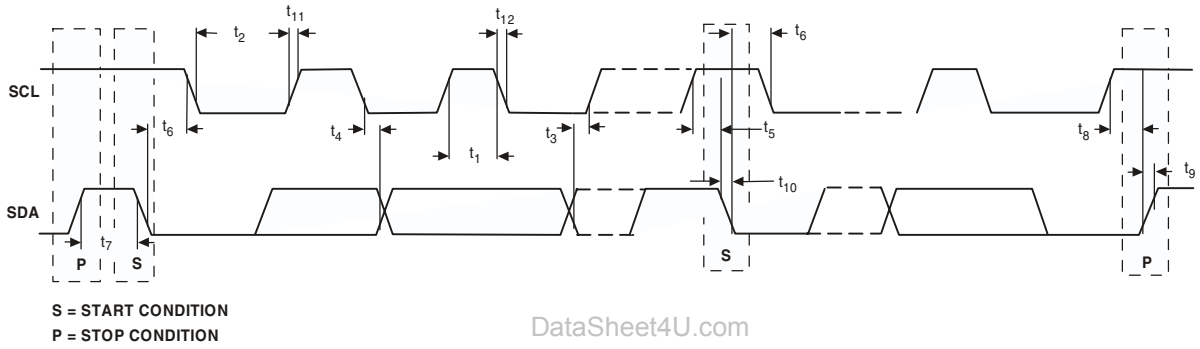

Figure 2. Two-Wire Serial Interface Timing Diagram

[6] Input filtering on both the SCL and SDA inputs suppress noise spikes that are less than 50nS or 10nS for Fast Mode or High-Speed Mode respectively

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Table 3. T_A = 25°C, unless otherwise noted

Parameter	Rating
V_{DD} to GND	–0.3 V to + 7.0 V
Digital Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	–0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Extended Automotive (W,Y Version)	–40°C to +125°C
Extended industrial (A,B Version)	-40°C to + 85°C
Storage Temperature Range	–65°C to +160°C
Maximum Junction Temperature	150°C
SC70 Package	
θ_{JA} Thermal Impedance	332°C/W
θ_{JC} Thermal Impedance	120°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	2.0 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	INL	I²C Interface Modes Supported	Temperature Range	Power Supply Range	Package Option	Package Description	Branding
AD5602YKSZ-1	± 1 LSB Max	Standard , Fast and High Speed Modes	-40°C to 125°C	2.7 V to 5.5V	KS-6	6-Lead SC-70	D5W
AD5602BKSZ-2	± 1 LSB Max	Standard, Fast Modes	-40°C to 85°C	2.7 V to 5.5V	KS-6	6-Lead SC-70	D5X
AD5602YKSZ-2	± 1 LSB Max	Standard , Fast Modes	-40°C to 125°C	2.7 V to 5.5V	KS-6	6-Lead SC-70	D5Y
AD5612YKSZ-1	± 0.5 LSB Max	Standard , Fast and High Speed Modes	-40°C to 125°C	2.7 V to 5.5V	KS-6	6-Lead SC-70	D5T
AD5612BKSZ-2	± 0.5 LSB Max	Standard, Fast Modes	-40°C to 85°C	2.7 V to 5.5V	KS-6	6-Lead SC-70	D5U
AD5612AKSZ-2	± 4 LSB Max	Standard , Fast Modes	-40°C to 85°C	2.7 V to 5.5V	KS-6	6-Lead SC-70	D5V
AD5612YKSZ-2	± 0.5 LSB Max	Standard, Fast Modes	-40°C to 125°C	2.7 V to 5.5V	KS-6	6-Lead SC-70	D5S
AD5622YKSZ-1	± 2 LSB Max	Standard , Fast and High Speed Modes	-40°C to 125°C	2.7 V to 5.5V	KS-6	6-Lead SC-70	D5M
AD5622BKSZ-2	± 2 LSB Max	Standard, Fast Modes	-40°C to 85°C	2.7 V to 5.5V	KS-6	6-Lead SC-70	D5N
AD5622YKSZ-2	± 2 LSB Max	Standard , Fast Modes	-40°C to 125°C	2.7 V to 5.5V	KS-6	6-Lead SC-70	D5P
AD5622WKSZ-1	± 6 LSB Max	Standard , Fast and High Speed Modes	-40°C to 125°C	2.7 V to 5.5V	KS-6	6-Lead SC-70	D5Q
AD5622AKSZ-2	± 6 LSB Max	Standard, Fast Modes	-40°C to 85°C	2.7 V to 5.5V	KS-6	6-Lead SC-70	D5R

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

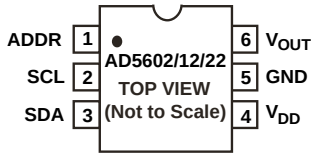

Figure 3. AD5602/12/22 SC70 (Top View)

Table 4. Pin Function Descriptions

Mnemonic	Function
V_{DD}	Power Supply Input. These parts can be operated from 2.7 V to 5.5 V, and V_{DD} should be decoupled to GND.
V_{OUT}	Analog Output Voltage from the DAC. The output amplifier has rail-to-rail operation.
ADDR	Tri-State Address input. Sets the two least significant bits (A1,A0) of the 7-bit slave address. See Table 5.
SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into or out of the 16-bit input register.
SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into or out of the 16-bit input register. It is a bidirectional open-drain data line that should be pulled to the supply with an external pull-up resistor.
GND	Ground Reference Point for all circuitry on the part.

TERMINOLOGY

Relative Accuracy

For the DAC, relative accuracy or Integral Nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 2.

Differential Nonlinearity

Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 7.

Zero-Code Error

Zero-code error is a measure of the output error when zero code (0000Hex) is loaded to the DAC register. Ideally the output should be 0 V. The zero-code error is always positive in the AD5602/12/22 because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in mV. A plot of zero-code error vs. temperature can be seen in Figure 6.

Full-Scale Error

Full-scale error is a measure of the output error when full-scale code (FFFF Hex) is loaded to the DAC register. Ideally the output should be VDD – 1 LSB. Full-scale error is expressed in percent of full-scale range. A plot of full-scale error vs. temperature can be seen in Figure 6.

Gain Error

This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percent of the full-scale range.

Total Unadjusted Error

Total Unadjusted Error (TUE) is a measure of the output error taking all the various errors into account. A typical TUE vs. code plot can be seen in Figure 5.

Zero-Code Error Drift

This is a measure of the change in zero-code error with a change in temperature. It is expressed in µV/°C.

Gain Error Drift

This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV secs and is measured when the digital input code is changed by 1 LSB at the major carry transition (7FFF Hex to 8000 Hex). See Figure 19.

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV secs and measured with a full-scale code change on the data bus, i.e., from all 0s to all 1s and vice versa.

TYPICAL PERFORMANCE CHARACTERISTICS

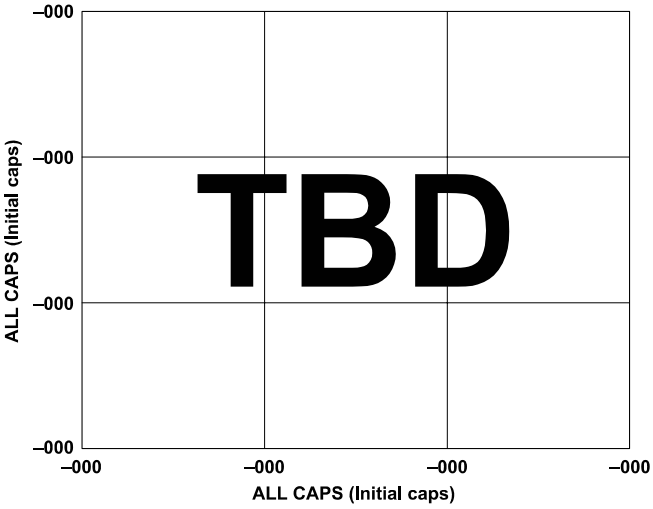

Figure 4. Typical INL Plot

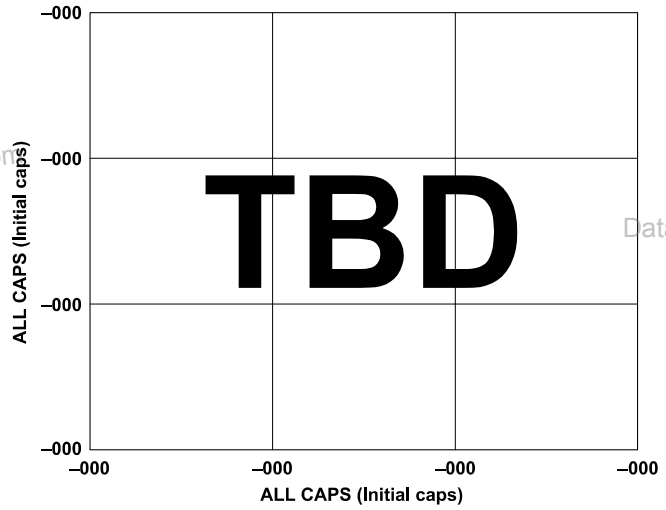

Figure 5. Total Unadjusted Error Plot..

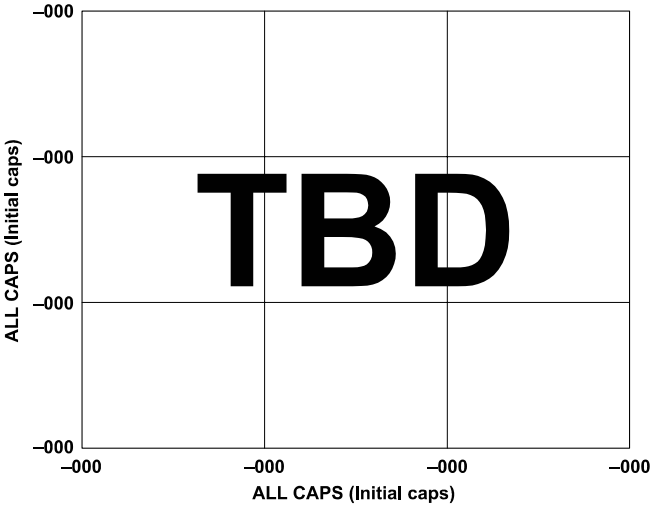

Figure 6. Zero Scale Error and Full Scale Error vs. Temperature

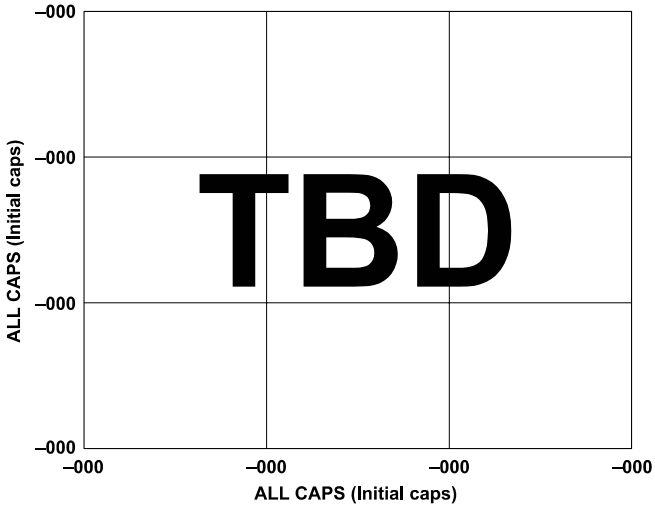

Figure 7. Typical DNL Plot

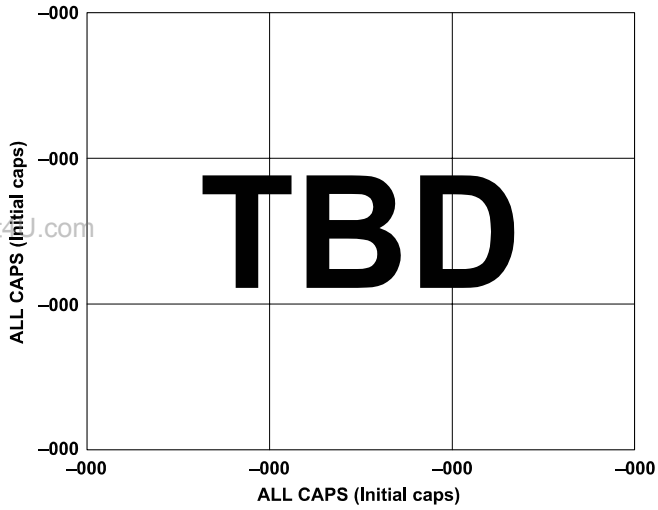

Figure 8. INL and DNL vs Supply

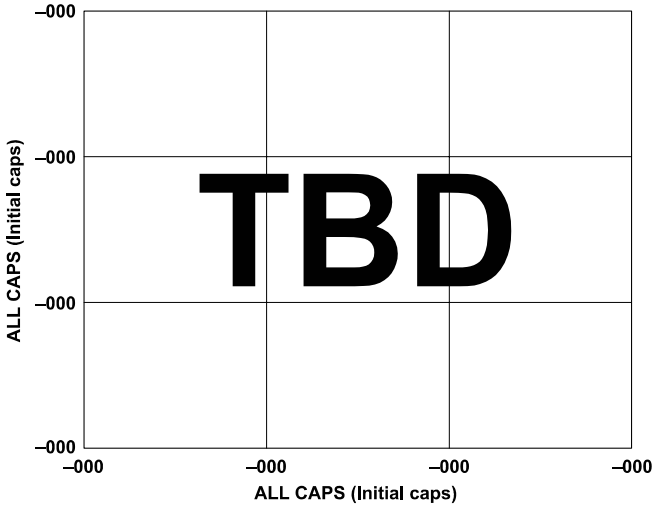

Figure 9. I_{DD} Histogram @ V_{DD} = 3 V/5 V

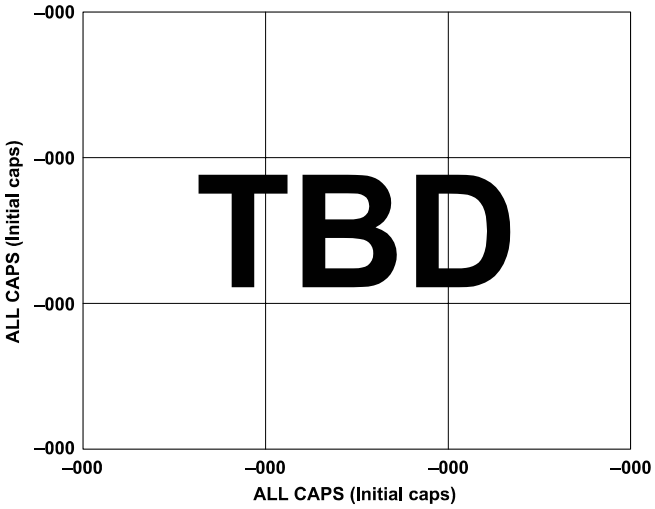

Figure 10. Source and Sink Current Capability

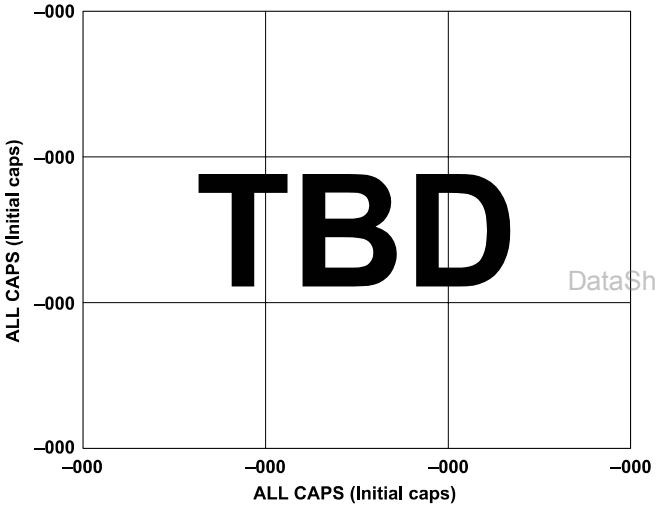

Figure 11. Supply Current vs. Temperature

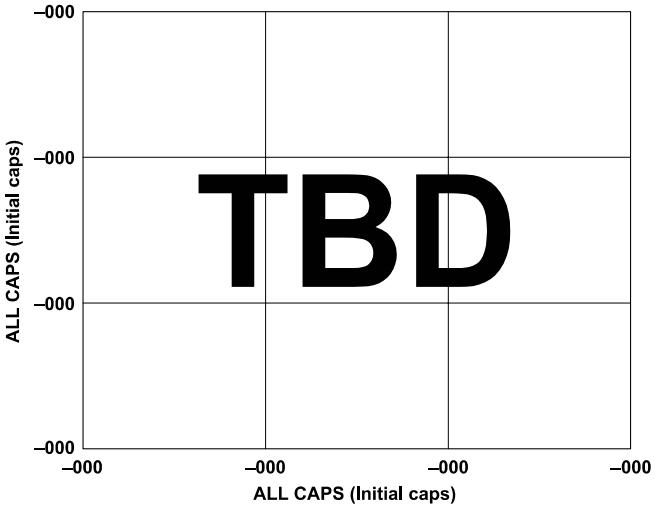

Figure 12. Full Scale Settling Time

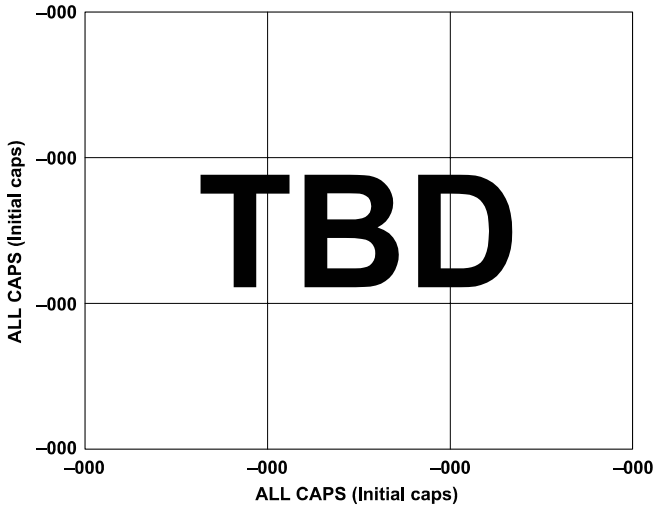

Figure 13. Supply Current vs Code.

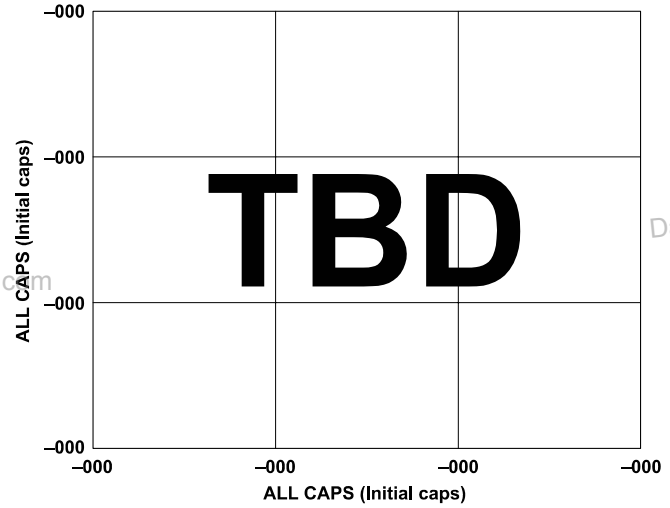

Figure 14. Supply Current vs. Supply Voltage

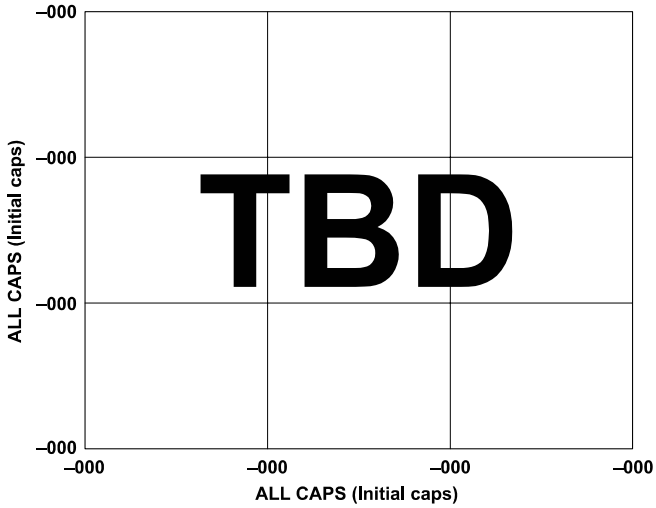

Figure 15. Half Scale Settling Time

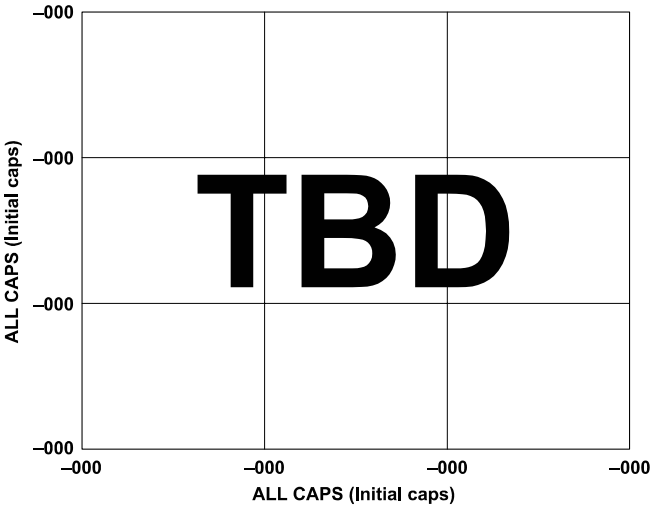

Figure 16. Power on Reset to 0 V

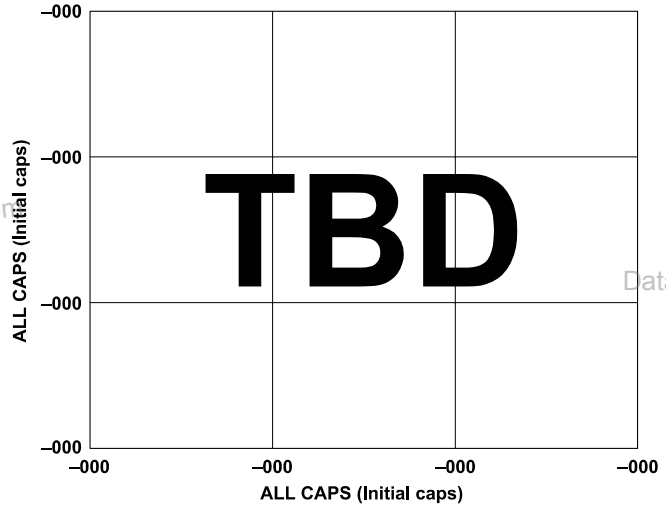

Figure 17. Digital to Analog Glitch Impulse

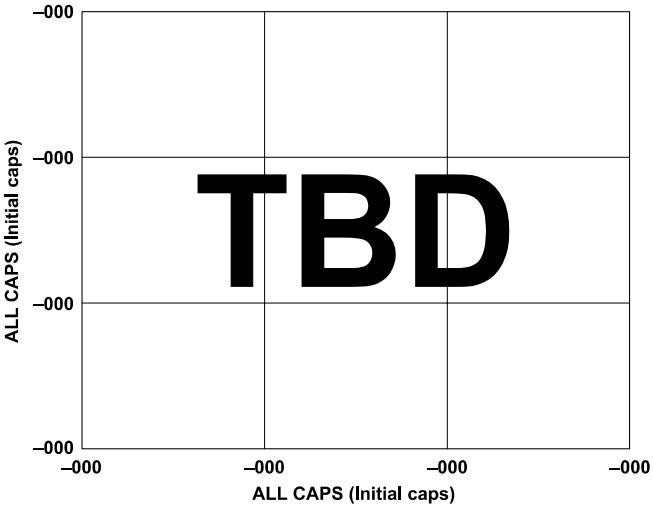

Figure 18. Output Spectral Density 100k Bandwidth

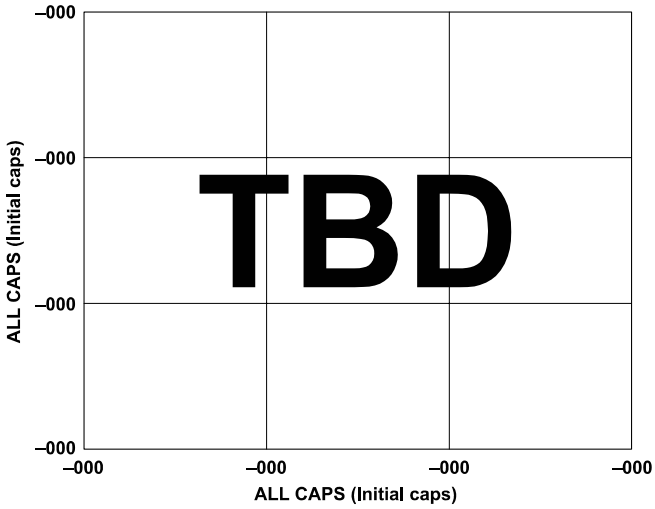

Figure 19. Exiting Power-Down

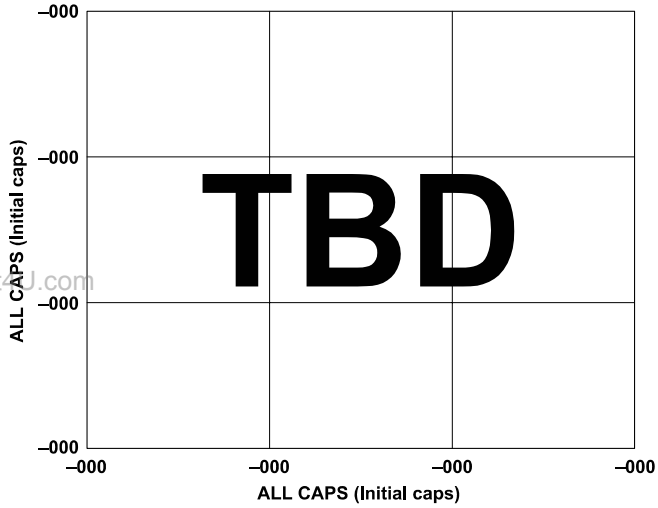

Figure 20.

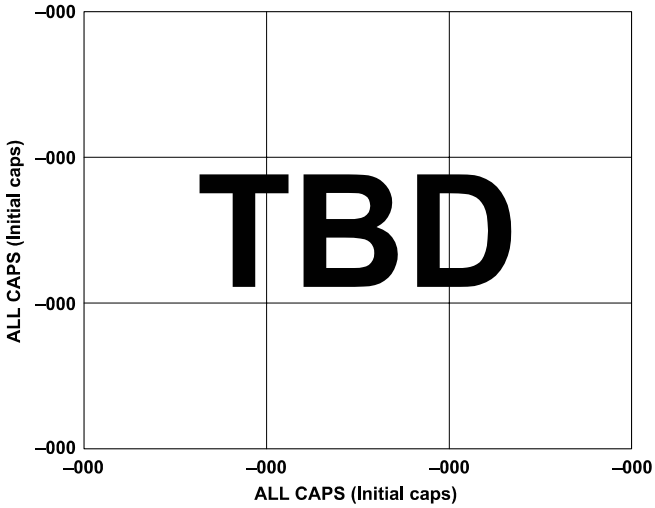

Figure 21. 0.1 Hz to 10 Hz Noise Plot

GENERAL DESCRIPTION

D/A SECTION

The AD5602/12/22 DAC is fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Figure 22 shows a block diagram of the DAC architecture.

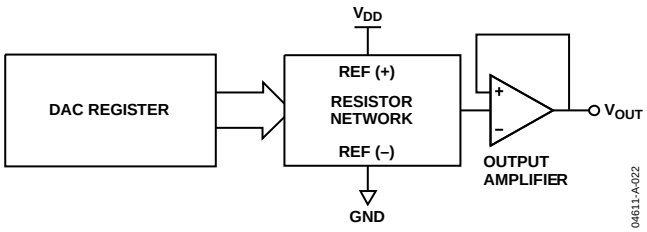

Figure 22. DAC Architecture

Since the input coding to the DAC is straight binary, the ideal output voltage is given by;

$$V_{OUT} = V_{DD} \times \left(\frac{D}{2^n} \right)$$

where;

D = Decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 255 (AD5602), 0 to 1023 (AD5612) or 0 to 4095 (AD5622).

And;

n = Bit resolution of the DAC.

RESISTOR STRING

The resistor string section is shown in Figure 23. It is simply a string of resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

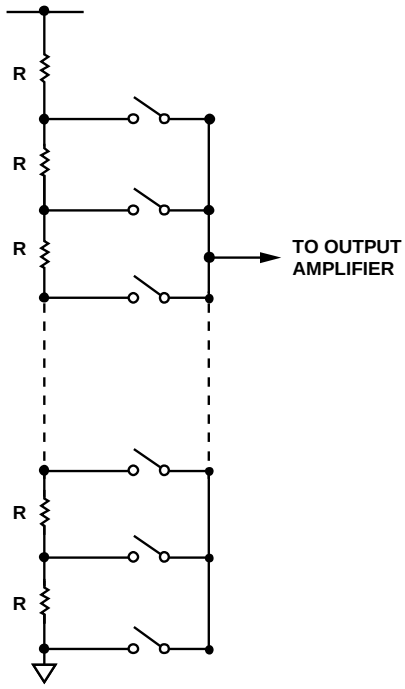

Figure 23 Resistor String Structure

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0 V to V_{DD}. It is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 10. The slew rate is 0.5 V/μs with a half-scale settling time of 8 μs with the output unloaded.

SERIAL INTERFACE

The AD5602/12/22 has a two-wire I²C compatible serial interface (Refer to I²C-Bus specification, Version 2.1, January 2000, available from Philips Semiconductor). The AD5602/12/22 can be connected to an I²C bus as a slave device, under the control of a master device. See Figure 2 for a timing diagram of a typical write sequence. The AD5602/12/22 supports Standard (100kHz), Fast (400 kHz) and High Speed (3.4 MHz) data transfer modes. Support is not provided for ten bit addressing and general call address.

The AD5602/12/22 have a 7-bit slave address. The 5 MSBs are 00011 and the two LSBs are determined by the state of the ADDR pin. The facility to make hardwired changes to ADDR allows the user to use up to three of these devices on one bus as outlined in Table 5.

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address. The slave whose address corresponds to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its shift register.

2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.

3. When all data bits have been read or written, a STOP condition is established. In write mode, the master will pull the SDA line high during the 10th clock pulse to establish a STOP condition. In read mode, the master will issue a No Acknowledge for the ninth clock pulse (i.e., the SDA line remains high). The master will then bring the SDA line low before the 10th clock pulse and then high during the 10th clock pulse to establish a STOP condition.

Table. 5 Device Address selection

ADDR	A1	A0
GND	1	1
V_{DD}	0	0
NC	1	0

INPUT REGISTER

The input register is 16 bits wide. Figure 23 illustrates the contents of the input register for each part. Data is loaded into the device as a 16 bit word under the control of a serial clock input, SCL. The timing diagram for this operation is shown in Figure 2. The 16 bit word consists of four control bits followed by 8, 10 or 12 bits of data depending on the device type. MSB (DB15) is loaded first. The first two bits are reserved bits that must be set to zero, the next two are control bits that control the mode of operation of the device (normal mode or any one of three power-down modes). See Power Down Modes section for a complete description.The remaining bits are left-justified DAC data bits, starting with the MSB and ending with the LSB.

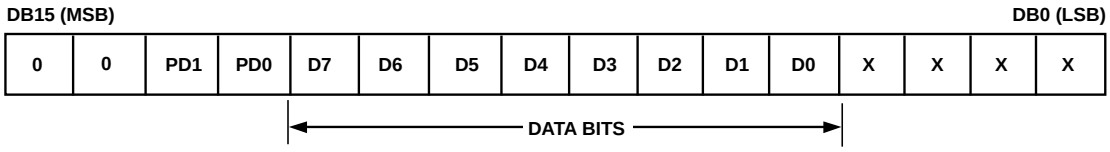

Figure 24a. AD5602 Input Register Contents

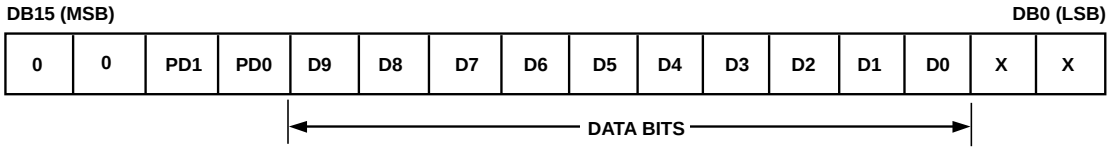

Figure 24b AD5612 Input Register Contents

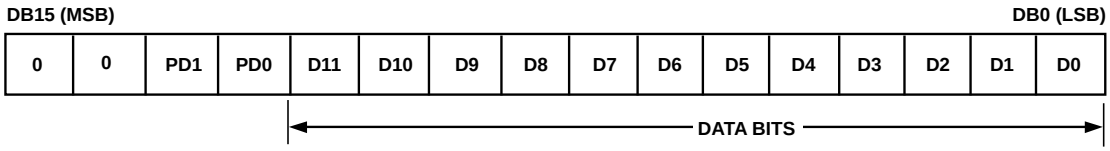

Figure 24c AD5622 Input Register Contents

POWER-ON-RESET

The AD5602/12/22 contains a power-on-reset circuit that controls the output voltage during power-up. The DAC register is filled with zeros and the output voltage is 0 V. It remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

POWER-DOWN MODES

The AD5602/12/22 contains four separate modes of operation. These modes are software-programmable by setting two bits (PD1 and PD0) in the control register. Table 6 shows how the state of the bits corresponds to the mode of operation of the device.

Table 6. Modes of Operation for the AD5602/12/22

PD1	PD0	Operating Mode
0	0	Normal Operation
0	1	Power-Down (1 kΩ Load to GND)
1	0	Power-Down (100 kΩ Load to GND)
1	1	Power-Down (Three-State Output)

When both bits are set to 0, the part works normally with its normal power consumption of 100 µA max at 5 V. However, for the three power-down modes, the supply current falls to <100 nA (at 3 V). Not only does the supply current fall but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND through a 1 kΩ resistor or a 100 kΩ resistor, or is left open-circuited (three-state). Figure 25 shows the output stage.

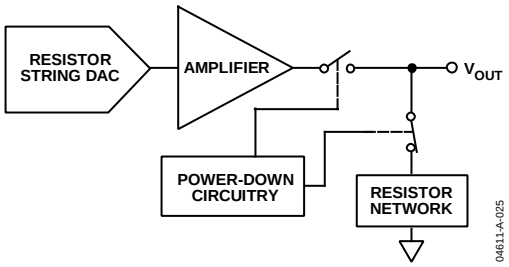

Figure 25 Output Stage During Power-Down

The bias generator, the output amplifier, the resistor string and other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 14 µs for V_{DD} = 5 V and 17 µs for V_{DD} = 3 V. See Figure 19 for a plot.

WRITE OPERATION

When writing to the AD5602/12/22, the user must begin with a START command followed by an address byte (R/W = 0), after which the DAC will acknowledge that it is prepared to receive data by pulling SDA low. Two bytes of data are then written to the DAC, the most significant byte followed by the least significant byte as shown in Figure 25, both data bytes will be acknowledged by the AD5602/12/22. A STOP condition then follows. The write operations for the three DACs is shown in Figure 25.

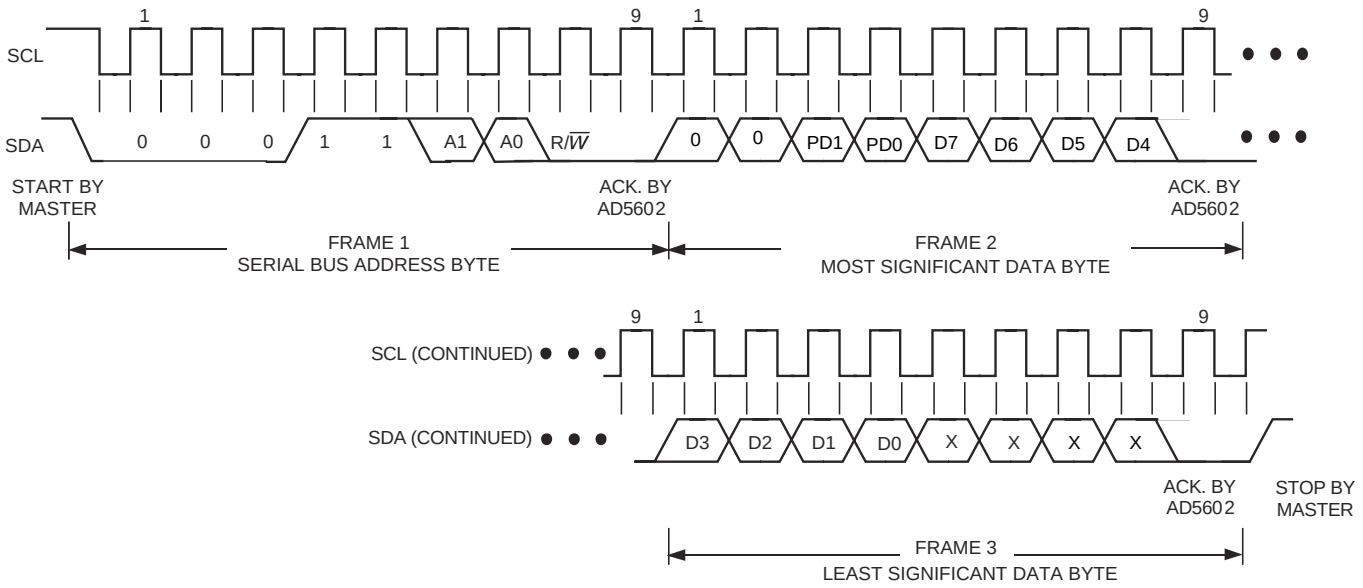

Figure 26a AD5602 Write Sequence

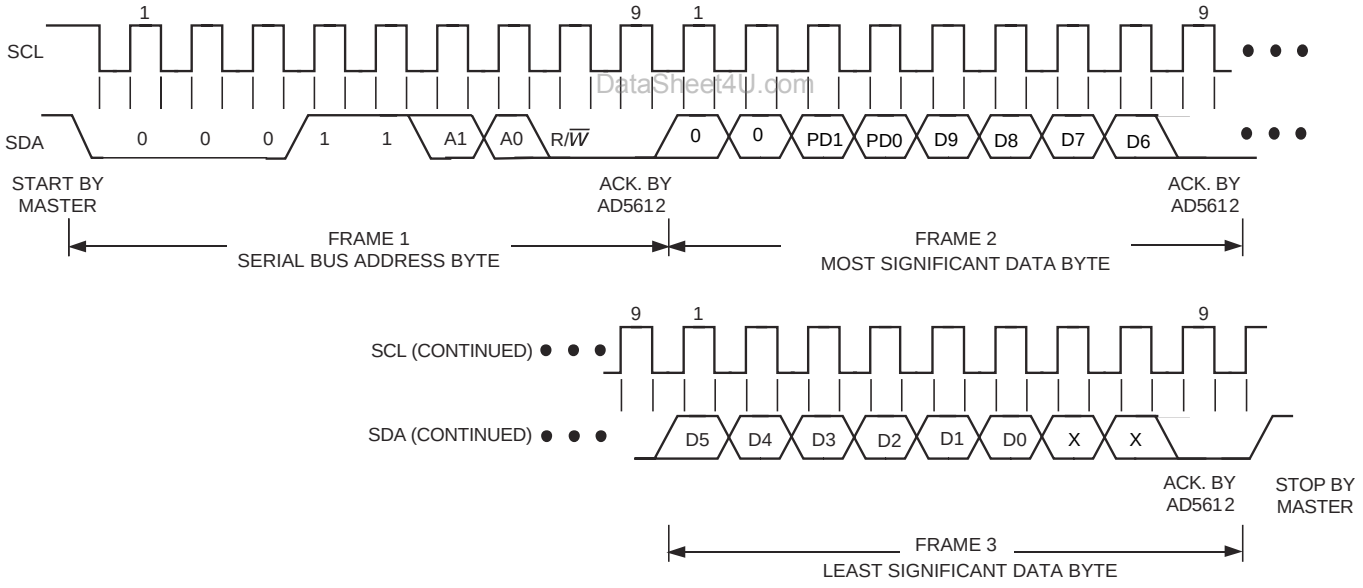

Figure 26b AD5612 Write Sequence

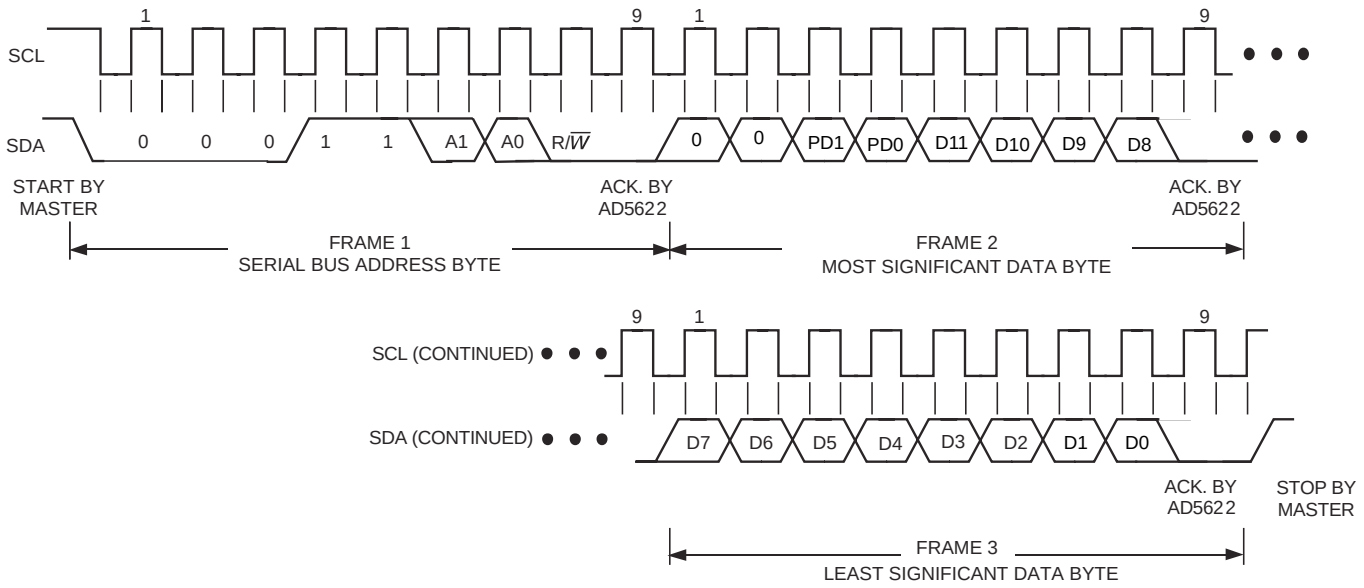

Figure 26c AD5622 Write Sequence

READ OPERATION

When reading data back from the AD5602/12/22, the user begins with a START command followed by an address byte (R/W = 1), after which the DAC will acknowledge that it is prepared to transmit data by pulling SDA low. Two bytes of data are then read from the DAC which are both acknowledged by the master as shown in Figure 26. A STOP condition follows.

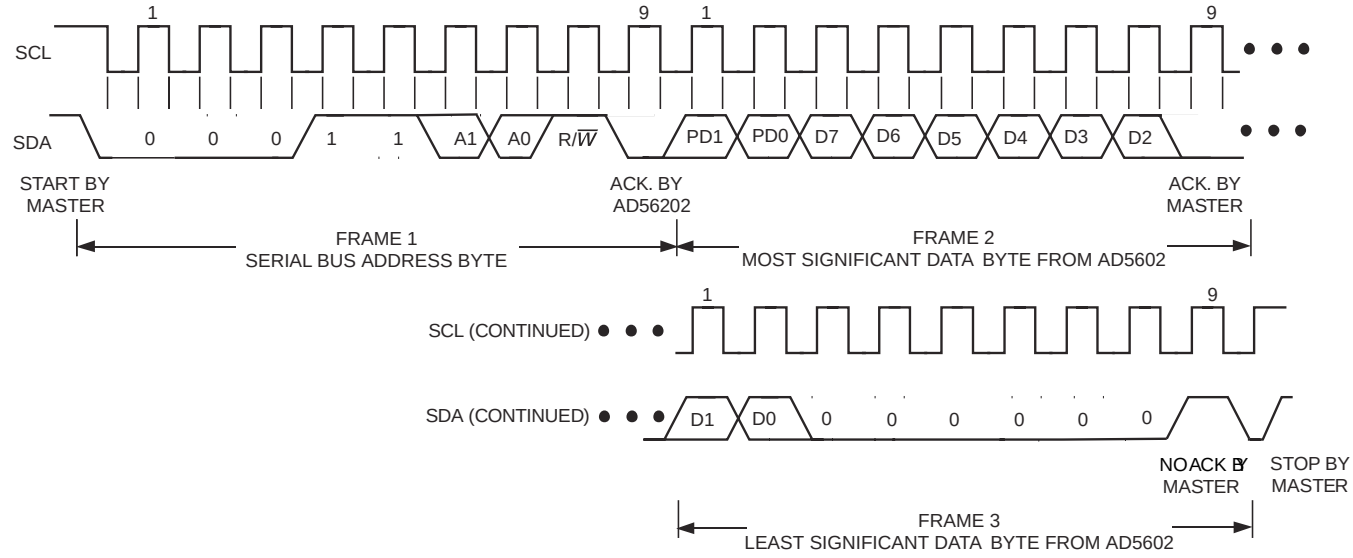

Figure 27a AD5602 Read Sequence

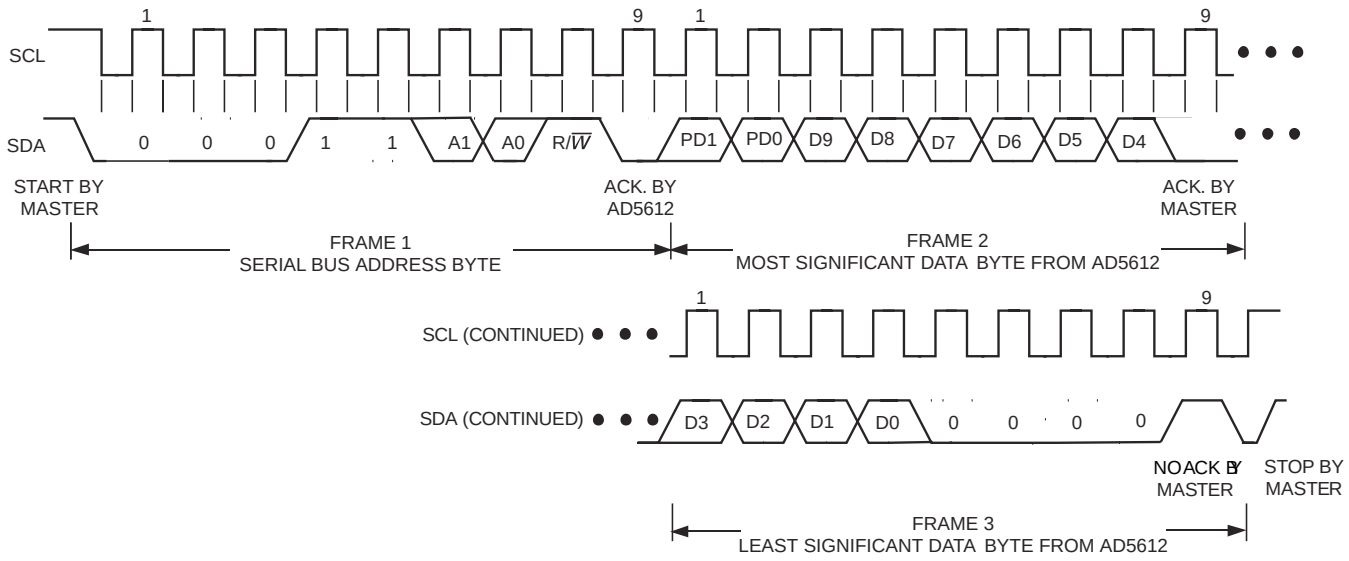

Figure 27b AD5612 Read Sequence

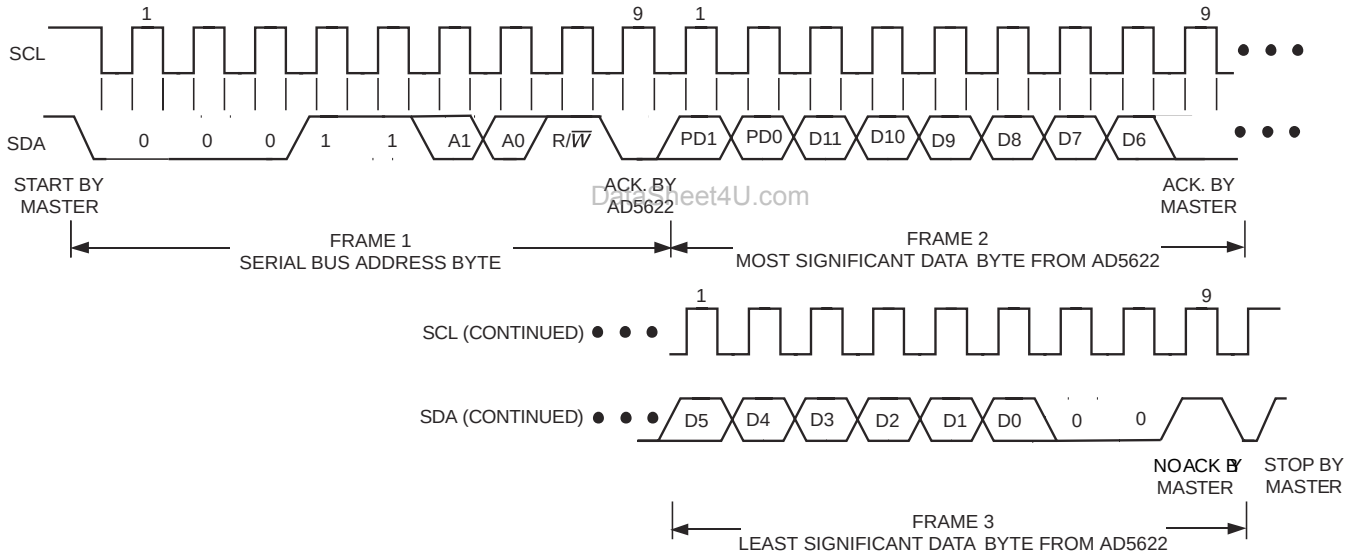

Figure 27c AD5622 Read Sequence

PLACING THE AD5602/12/22 -1 INTO HIGH-SPEED MODE

Hs-Mode communication commences after the master addresses all devices connected to the bus with the Master code, 00001XXX, to indicate that a High-Speed Mode transfer is to begin. No device connected to the bus is permitted to acknowledge the High-Speed Master code, therefore the code is followed by a not-Acknowledge. The master must then issue a repeated start followed by the device address. The selected device will then acknowledge its address. All devices continue to operate in Hs-Mode until such time as the master issues a STOP condition. When the STOP condition is issued the devices all return to F/S Mode.

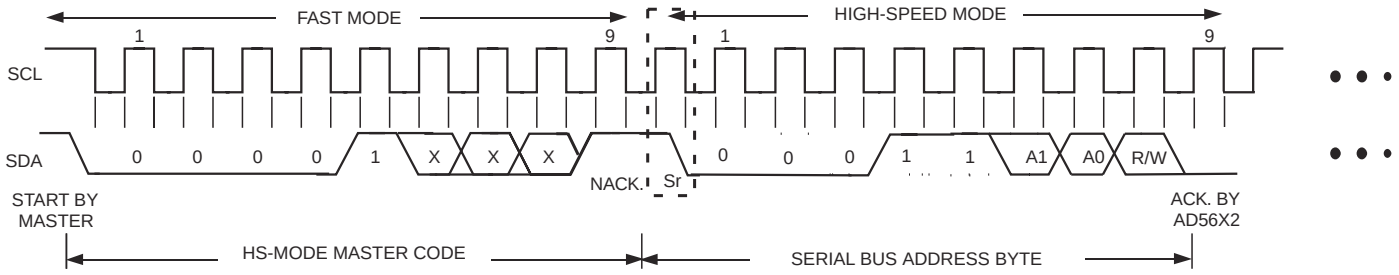

Figure 28 Placing the AD5602/12/22 into High Speed Mode

APPLICATIONS

CHOOSING A REFERENCE AS POWER SUPPLY FOR AD5602/12/22

The AD5602/12/22 comes in a tiny SC70 package with less than 100 µA supply current. Because of this, the choice of reference depends on the application requirement. For space saving applications, the ADR425 is available in an SC70 package and has excellent drift at 3ppm/°C. It also provides very good noise performance at 3.4 µV p-p in the 0.1 Hz to 10 Hz range.

Because the supply current required by the AD5602/12/22 is extremely low, it is ideal for low supply applications. The ADR293 voltage reference is recommended in this case. This requires 15 µA of quiescent current and can therefore drive multiple DACs in the one system if required.

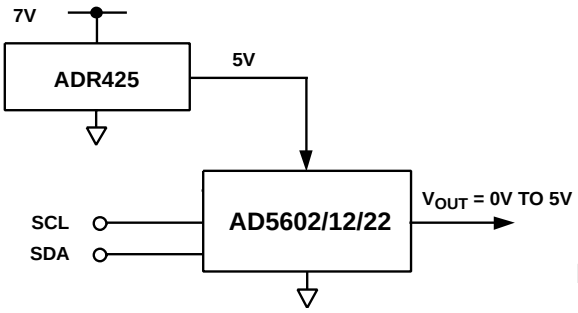

Figure 29. ADR425 as Power Supply to AD5602/12/22

Examples of some recommended precision references for use as supply to the AD5602/12/22 are shown in Table 7.

Table 7. Precision References for Use with AD5602/12/22

Part No.	Initial Accuracy (mV max)	Temperature Drift (ppm/°C max)	0.1–10 Hz Noise (µV p-p typ)
ADR435	±6	3	3.4
ADR425	±6	3	3.4
ADR02	±5	3	15
ADR395	±6	25	5

BIPOLAR OPERATION USING THE AD5602/12/22

The AD5602/12/22 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 30. The circuit in Figure 30 will give an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{DD} \times \left(\frac{D}{2^n} \right) \times \left(\frac{R1 + R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0–16384) and n represents the bit resolution of the DAC.
With V_{DD} = 5 V, $R1 = R2$ = 10 kΩ:

$$V_O = \left(\frac{10 \times D}{2^n} \right) - 5\text{V}$$

This is an output voltage range of ±5 V with 000 Hex corresponding to a –5 V output and FFF Hex corresponding to a +5 V output.

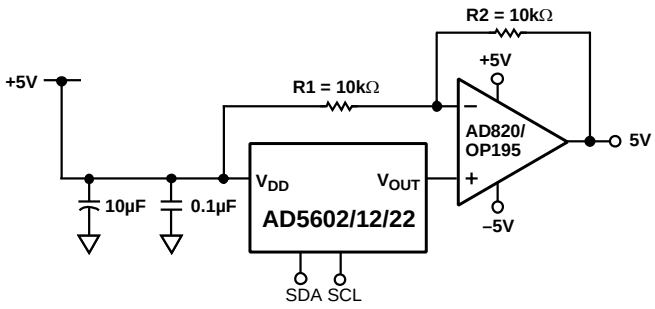

Figure 30. Bipolar Operation with the AD5602/12/22

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5602/12/22 should have separate analog and digital sections, each having its own area of the board. If the AD5602/12/22 is in a system where other devices require an AGND to DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5602/12/22.

The power supply to the AD5602/12/22 should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should be physically as close as possible to the device with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor has low effective series resistance (ESR) and effective series inductance (ESI), e.g., common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

OUTLINE DIMENSIONS

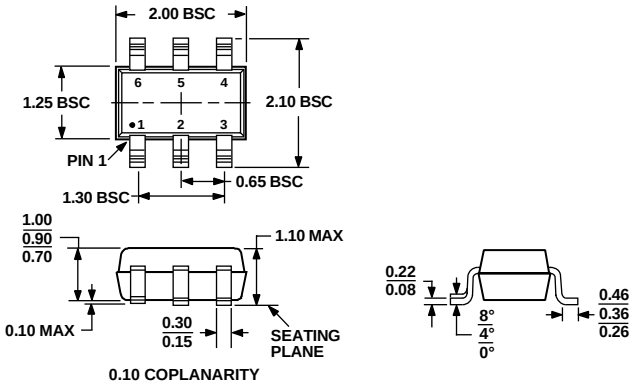

Figure 31. 6-Lead Plastic Surface Mount Package [SC70]
(KS-6)
Dimensions shown in millimeters