

HN62418 Series

HN62428 Series

8M (512K x 16-bit) and (1M x 8-bit) Mask ROM

■ DESCRIPTION

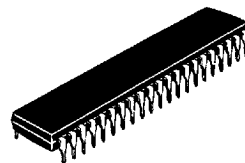
The Hitachi HN62418/428 Series is an 8-Megabit CMOS Mask Programmable Read Only Memory organized either as 524,288 x 16-bit or as 1,048,576 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition, the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62418/428 is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP and 44-lead Plastic QFP packages. The HN62418 is also packaged in a 44-lead TQFP, a 44-lead Plastic SOP and TSOP and a 48-lead Plastic SOP.

■ FEATURES

- Single Power Supply
 $V_{CC} = 5\text{ V} \pm 10\%$
- Fast Access Time:
150 ns (max)
- Low Power Consumption:
Active Current: 100 mW (typ)
Standby Current: 5 μ W (typ)
- User Selectable Organization:
1M x 16-bit (Word-Wide)
2M x 8-bit (Byte-Wide)
Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
42-pin Plastic DIP
44-lead Plastic QFP
44-lead TQFP
44-lead Plastic SOP
48-lead Plastic SOP
44-lead Plastic TSOP (Type II)



(DP-42)



(FP-44A)



(TFP-44)



(FP-44D)



(FP-48DA)



(TTP-44D)

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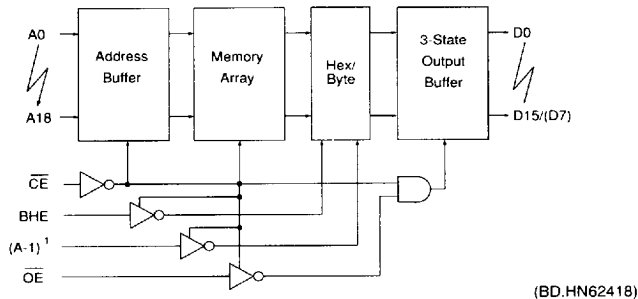
ORDERING INFORMATION

Type No.	Access Time	Package
HN62418/428P	150 ns/200 ns	42-pin Plastic DIP (DP-42)
HN62418/428FP	150 ns/200 ns	44-lead Plastic QFP (FP-44A)
HN62418/428TFP	150 ns/200 ns	44-lead TQFP (TFP-44)
HN62418/428FB	150 ns/200 ns	44-lead Plastic SOP (FP-44D)
HN62418/428F	150 ns/200 ns	48-lead Plastic SOP (FP-48DA)
HN62418/428TT	150 ns/200 ns	44-lead Plastic TSOP (TTP-44D)

PIN DESCRIPTION

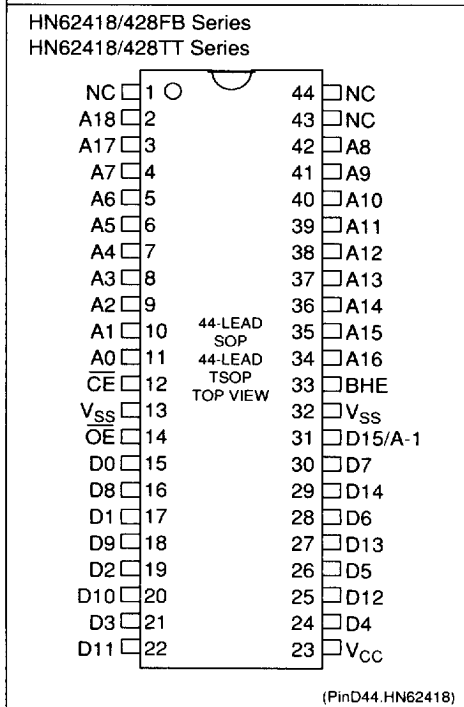
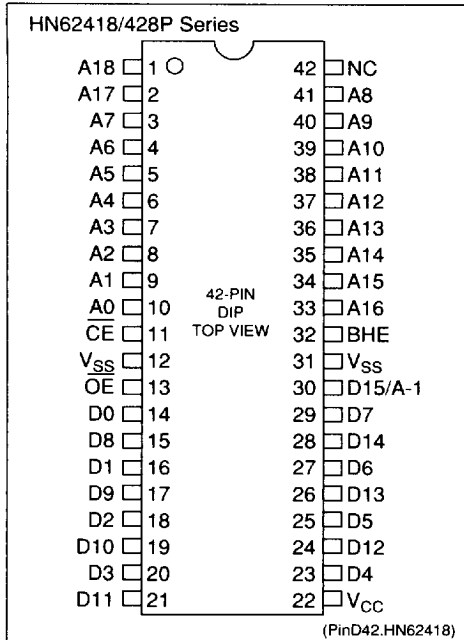
Pin Name	Function
$A_0 - A_{18}$	Address
A_{-1}	Address (Word-Wide)
$D_0 - D_{15}$	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



- Notes:
- A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
 - $BHE = V_{IH}$: 16-bit ($D_{15} - D_0$)
 $BHE = V_{IL}$: 8-bit ($D_7 - D_0$)
When BHE is low, $D_{14} - D_8$ are in high impedance states.

■ PIN ARRANGEMENT



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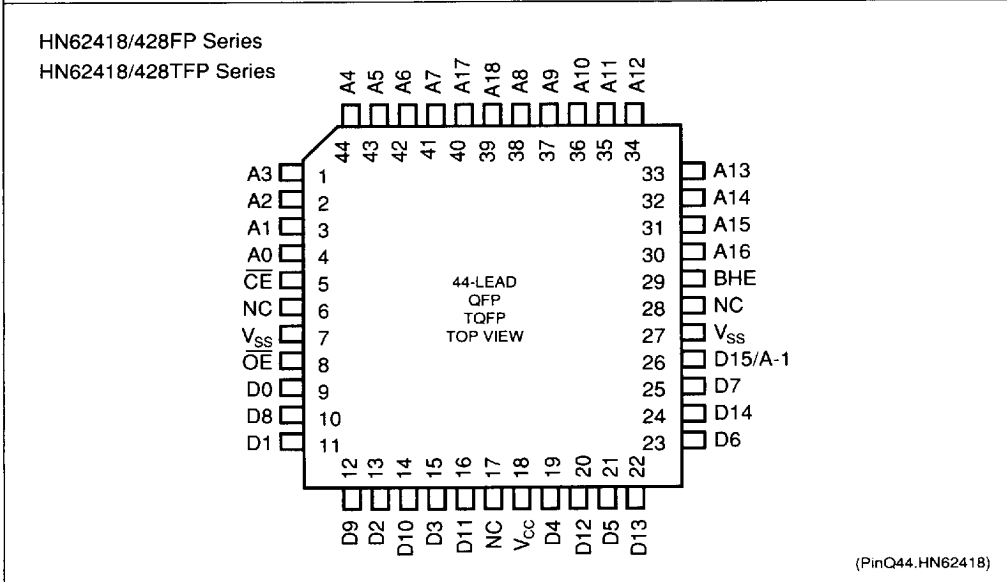
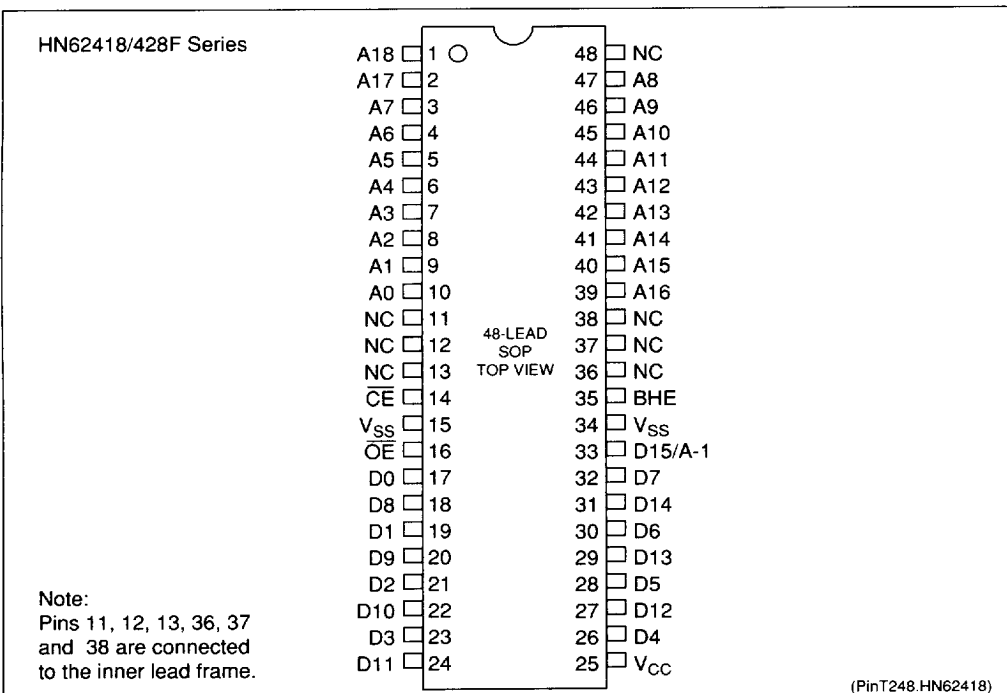
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■ PIN ARRANGEMENT (cont.)



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■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage ¹	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage ¹	V_T	-0.3 to $V_{CC} + 0.3$	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS} .

■ CAPACITANCE

($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 25^\circ C$, $V_{IN} = 0V$, $f = 1MHz$)

Item	Symbol	Min.	Max.	Unit
Input Capacitance ¹	C_{IN}	-	15	pF
Output Capacitance ¹	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0$ to $70^\circ C$)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	μA	$V_{IN} = 0$ to V_{CC}
Output Leakage Current	I_{LO}	-	10	μA	$\overline{CE} = 2.2V$, $V_{OUT} = 0$ to V_{CC}
Operating V_{CC} Current	I_{CC}	-	50	mA	$V_{CC} = 5.5V$, $I_{DOUT} = 0mA$, $t_{RC} = \text{Min.}$
Standby V_{CC} Current	I_{SB}	-	30	μA	$V_{CC} = 5.5V$, $\overline{CE} \geq V_{CC} - 0.2V$
Input Voltage	V_{IH}	2.2	$V_{CC} + 0.3$	V	
	V_{IL}	-0.3	0.8	V	
Output Voltage	V_{OH}	2.4	-	V	$I_{OH} = -205 \mu A$
	V_{OL}	-	0.4	V	$I_{OL} = 1.6 mA$

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■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION
 $(V_{CC} = 5V \pm 10\%, V_{SS} = 0V, T_a = 0 \text{ to } 70^\circ\text{C})$
Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: $\leq 10 \text{ ns}$
- Output load: 1 TTL Gate + $CL = 100 \text{ pF}$ (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62418		HN62428		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	150	-	200	-	ns
Address Access Time	t_{AA}	-	150	-	200	ns
CE Access Time	t_{ACE}	-	150	-	200	ns
OE Access Time	t_{OE}	-	70	-	100	ns
BHE Access Time	t_{BHE}	-	150	-	200	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from CE	t_{DHC}	0	-	0	-	ns
Output Hold Time from OE	t_{DHO}	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	ns
CE to Output in High Z	t_{CHZ}^1	-	70	-	70	ns
OE to Output in High Z	t_{OHZ}^1	-	70	-	70	ns
BHE to Output in High Z	t_{BHZ}^1	-	70	-	70	ns
CE to Output in Low Z	t_{CLZ}^1	10	-	10	-	ns
OE to Output in Low Z	t_{OLZ}^1	10	-	10	-	ns
BHE to Output in Low Z	t_{BLZ}^1	10	-	10	-	ns

Note: 1. t_{CHZ} , t_{OHZ} , and t_{BHZ} define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

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