V7001
SDR-SDRAM Memory Controller

Features

- JEDEC standard SDR-SDRAM supported
- Transaction pipeline for maximum utilization of the Memory Bus
- 3 Request buffers for transaction pipeline
- Supports CAS latencies of 1, 2 and 3
- 4 or 8 beat burst transactions supported
- Supports up to 4 chip selects of Memory devices
- Page mode support for up to 16 open pages
- Supports flexible Row and Column addressing
- Supports up to 4GB of Memory Address space
- Supports Registered DIMM Mode
- Supports Auto Refresh and Self Refresh
- Refresh for populated banks only
- Automatic Refresh of idle slots
- Interrupt generation for invalid address requests
- Programmable Refresh rate
- Programmable timing parameters
- Configuration register read/ write interface fully complies with standard OCP Slave (basic signals)
- Configurable 8/16/32/64-bit OCP Slave interface for register configuration
- Configurable 8/16/32/64-bit memory data bus interface for data transfers

Functional Overview

SDR is a very high performance memory controller to interface with SDR-SDRAM memory devices. It is having three bus interfaces, Memory interface, Configuration bus interface and Host interface. Configuration bus and Host Interface are to communicate with the Host. The configuration bus facilitates to program the internal SDR configuration registers. And the Host bus is used to initiate the actual memory data transactions. Host places the Read/Write requests on this bus and the SDR core correspondingly performs the data transactions. This bus width is same as the memory data bus width. The typical usage of the core in system is shown in Fig 1: V7001 Megacell in a Typical System.

The SDR core is having three internal request buffers which can store three different transaction requests from the Host. Even though the response to the Host is in order with reference to transaction launching, all the transactions in the internal request buffers will be pipelined for effective utilization of the SDRAM Memory Bus interface. Because of processing three requests at same time, the required commands can be launched for all the three requests at appropriate time to achieve the maximum data bandwidth.

The SDR supports up to 4 chip selects and each chip select address range is programmable. Interrupt can be asserted if the requested address is not falling in any of the chip select address range or when there is an overlap between two chip select address ranges. The external interfaces to the core are indicated in Fig 2: V7001 Megacell I/O Diagram

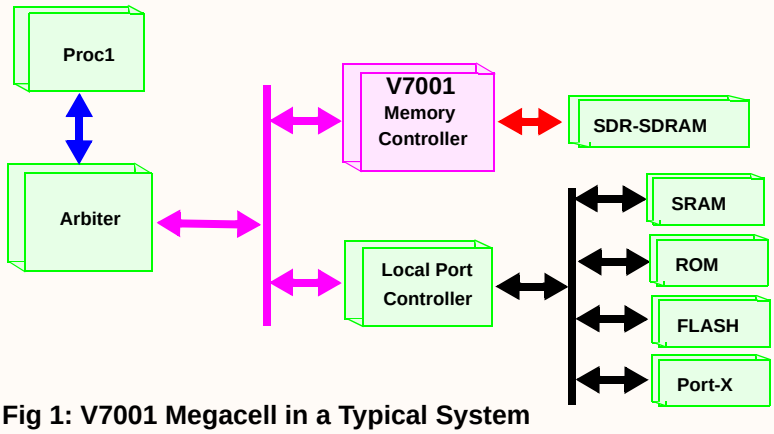

Fig 1: V7001 Megacell in a Typical System

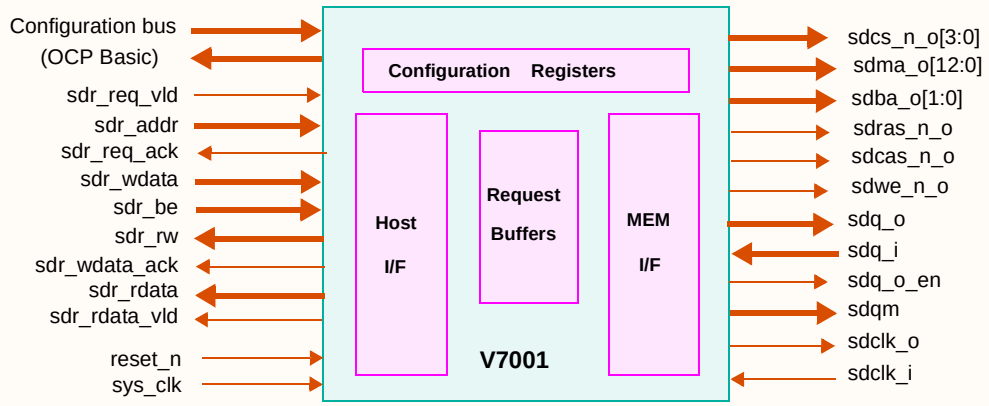

Fig 2: V7001 Megacell I/O Diagram

Performance Specifications

Parameter	Value	Remarks
Gate Count	~26 K	for 32-bit configuration bus and 32-bit memory bus
Code Coverage	100%	Block, Arc, State Transitions, Expressions, Events
OpenMORE Score	96%	
Technology	0.18µ	Artisan, TSMC
Frequency	170 MHz	STA verified with pre-route, pre-scan netlist

Target Applications

- Can be easily interfaced to any SoC designs that need to interact with SDR-SDRAM
- In embedded memory intensive applications

Test Coverage

- Design is highly synchronous and scan friendly
- Fault coverage is 94% with ATPG vectors

Deliverables

- Fully synthesizable Verilog RTL source code
- Documentation - Data Sheet, User Guide, Verification Description Document
- Self checking Verification Suite
- Synthesis Scripts
- Scripts for STA & DFT (optional)

QualCore Logic, Inc.
1289, ANVILWOOD AVENUE
SUNNYVALE, CA - 94089, USA
Tel: 408 541 0730 Fax: 408 541 0740
E-mail: sales@qualcorelogic.com
http://www.qualcorelogic.com