Target Specification

TENTATIVE

Dec. 18, 2007

No. DPBCL0001404-05

HITACHI

LIQUID CRYSTAL DISPLAY MODULE
TECHNICAL DATA

TX06D103VM0AAA

CONTENTS

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RECORD OF REVISIONS

Date	Sheet No.	Summary

3. GENERAL DATA

(1) Product Name	TX06D103VM0AAA
(2) Module Dimensions	42.62 (W) mm x 60.5(H) mm x 2.45 (t) mm
(3) Active Area Dimensions	36.72 (W) mm x 48.96 (H) mm
(4) Pixel Pitch	0.153 (W) mm x 0.153 (H) mm
(5) Resolution	240 x 3 (R, G, B) (W) x 320 (H) dots
(6) Color Pixel Arrangement	RGB Vertical Stripe
(7) Display Mode	Transmissive Type, Normally Black Mode, IPS
(8) Number of Colors	65,536 Colors (8-bit, 16-bit CPU - I/F) 262,144 Colors (9-bit, 18-bit CPU - I/F)
(9) Viewing Direction	-
(10) Backlight	Light Emitting Diode (LED) Four LEDs connected in Series
(11) Weight	12.0g
(12) Power Supply Voltage	Vcc = 2.8 V (typ)
(13) Interface I/O power supply	1.75V $\leq$ I/OVcc $\leq$ Vcc
(14) LCD Driver IC	R61505U
(15) Interface	8-bit / 9-bit / 16-bit / 18-bit CPU bus (80 CPU series)

4. ABSOLUTE MAXIMUM RATINGS

4. 1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS OF LCD

VSS = 0 V

Item	Symbol	Min	Max	Unit	Note
Power Supply for Logic and Analog	Vcc	-0.3	4.6	V	(1), (2)
Power Supply for Interface	I/OVcc	-0.3	4.6	V	(1), (2)
Input Voltage	V_{IN}	-0.3	I/OVcc+0.3	V	(1), (3)
LED Reverse Voltage	VR	-	5	V	(1), (4)
LED Forward Current	ILED	-	35	mA	(4), (5)
Static Electricity	-	-	±2	kV	(6)

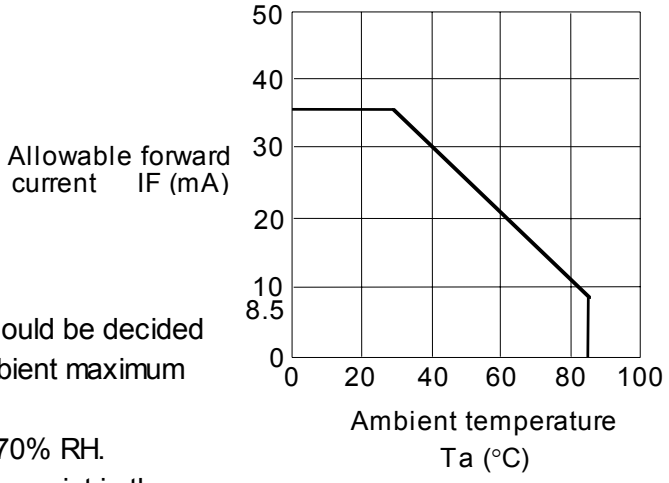
Notes (1) All voltage values are referred to GND.

(2) I/OVcc ≤ Vcc

(3) Applies to the RESET*, RD*, WR*, CS*, RS,VSYNC*, IM0, IM3 and DB17-0 pins.

(4) Ta = 25 deg C, per piece of LED.

(5) Relationship between ambient temperature and allowable forward current



The operating current should be decided after considering the ambient maximum temperature of LEDs.

(6) 100 pF, 1.5 kohm, 25°C, 70% RH.
Static electricity discharge point is the center of LCD's surface.

4. 2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

Item	Operating		Storage		Comment
	Min	Max	Min	Max	
Ambient Temperature	-20°C	70°C	-30°C	80°C	Note (2)
Humidity	Note (1)		Note (1)		No condensation
Corrosive Gas	Not Acceptable		Not Acceptable		

Notes (1) Ta ≤ 40°C: 85% RH max.
Ta > 40°C: Absolute humidity must be lower than the humidity of 85%RH at 40°C.
The polarizer quality is not assured by the above values.

(2) Background color slightly changes depending on ambient temperature and viewing angle.

5. ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS OF LCD

Ta = 25°C, VSS = 0 V

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Power Supply Voltage for Logic and Analog	Vcc	-	2.72	2.8	2.88	V	
Power Supply Voltage for Inteface	I/OVcc	-	1.75	-	Vcc		
Input Voltage for Logic Circuits	Vi	"H" level	0.8 x I/OVcc	-	I/OVcc	V	(1)
		"L" level	0	-	0.2 x I/OVcc		
Output Voltage for Logic Circuits	Vo	"H" level	0.8 x I/OVcc	-	-	V	(2)
		"L" level	-	-	0.2 x I/OVcc		
Input/Output Leak current	ILi	-	-1.0	-	1.0	μA	
Power Supply Current	Icc	All White	-	2.5	4.0	mA	(3)
		Partial	-	1.3	2.5	mA	(4)
		Standby	-	0.1	1.0	μA	(5)
LED Forward Voltage	VLED	-	-	3.2	3.5	V	
LED Forward Current	I LED	-	-	18	Note (6)	mA/LED	
Frame Frequency	fFLM	-	-	85	-	Hz	

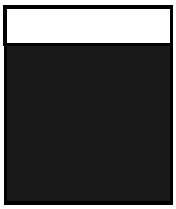
Notes (1) Applies to the RESET*, RD*, WR*, CS*, RS, VSYNC*, IM0, IM3 and DB17-0 pins.

(2) Applies to the FMARK and DB17-0 pins.

(3) Vcc = I/OVcc = 2.8 V, fFLM = 85 Hz

(4) Partial Pattern

40 Lines: White
280 Lines: Black
fFLM = 85 Hz
8-color mode



40 Lines: White

280 Lines: Black

(5) Vcc = I/OVcc = 2.8 V, Standby mode

(6) Refer to Item 4.1

6. OPTICAL CHARACTERISTICS

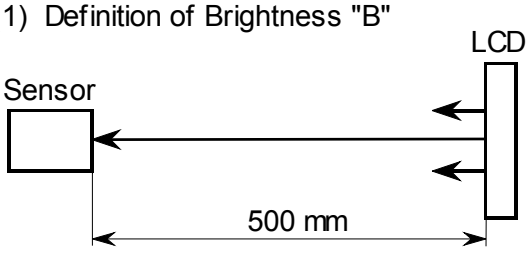
OPTICAL CHARACTERISTICS OF LCD (BACKLIGHT ON)

Item		Symbol	Condition	Min	Typ	Max	Unit	Note
Brightness		B	ϕ=0°, θ=0°	170	250	-	cd/m^2	(1), (2)
Contrast ratio		K	ϕ=0°, θ=0°	200	400	-	-	(1), (6)
Viewing angle		ϕ1 + ϕ2	θ=0°, K≥10	-	160	-	deg	(4), (6), (7)
			θ=90°, K≥10	-	160	-		
Brightness uniformity		-	ϕ=0°, θ=0°	70	80	-	%	(2), (3), (5)
Response time		tr + tf	ϕ=0°, θ=0° Ta=25°C	-	40	70	ms	(8)
Color tone (Primary Color)	Red	x	ϕ=0° θ=0° Maximum Gradient	0.57	0.63	0.69	-	(1)
		y		0.27	0.33	0.39		
	Green	x		0.28	0.34	0.40		
		y		0.53	0.59	0.65		
	Blue	x		0.08	0.14	0.20		
		y		0.05	0.11	0.17		
	White	x		0.25	0.31	0.37		
		y		0.26	0.32	0.38		

Common conditions for measurement

Measurement environment : Dark room
Ambient temperature : Ta = 25°C
Sequence : Follow Item 8.4.2, SEQUENCE.
Power supply voltage : Vcc = I/OVcc = 2.8 V
Backlight current : 18 mA

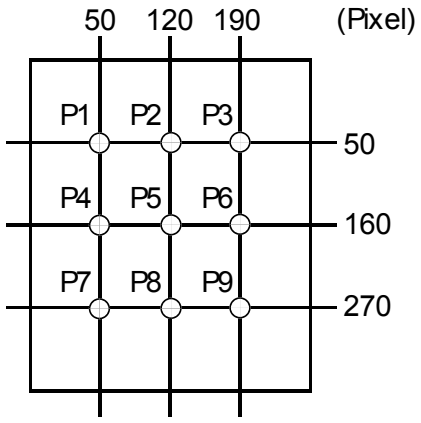
Notes (1) Definition of Brightness "B"



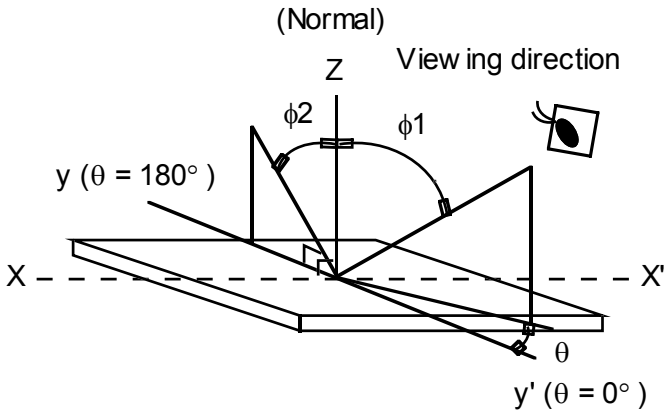
Sensor : TOPCON / BM-5A or equivalent
Measurement point : Center of LCD's active area

(2) Display image for measurement : White

Notes (3) Measurement point



(4) Definitions of θ and ϕ



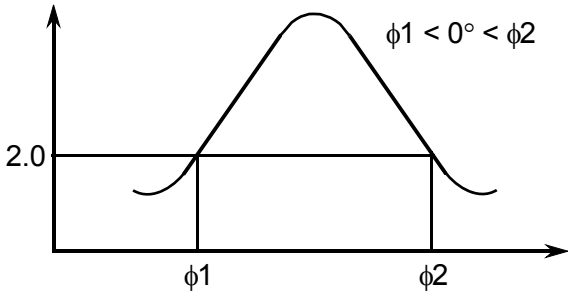
(5) Definition of the brightness uniformity

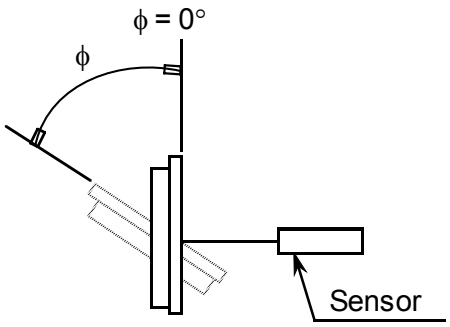
Uniformity = Brightness (min.) / Brightness (max.) x 100(%)

(6) Definition of Contrast "K"

$$K = \frac{\text{Brightness when displaying White raster}}{\text{Brightness when displaying Black raster}}$$

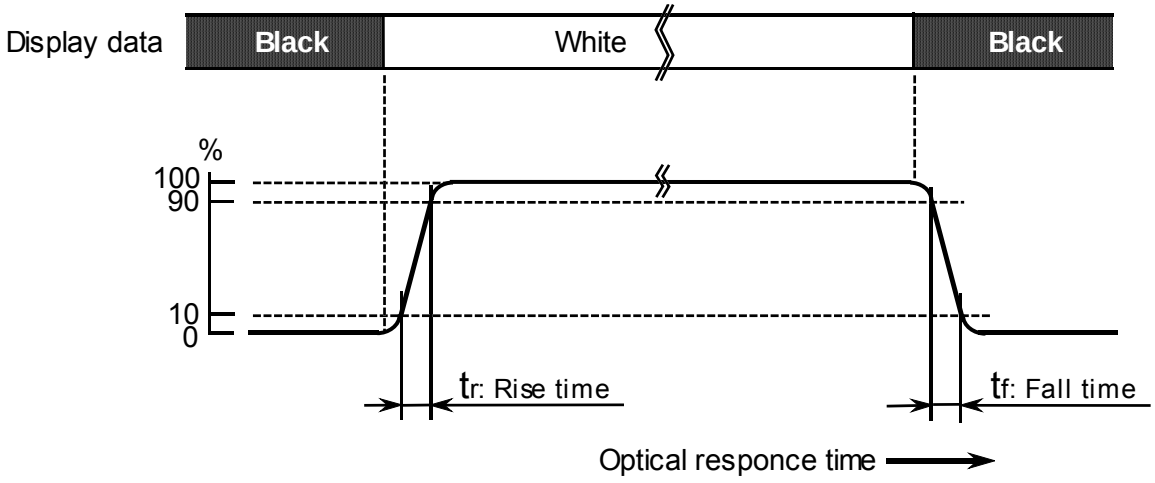
(7) Definition of viewing angle ϕ1 and ϕ2



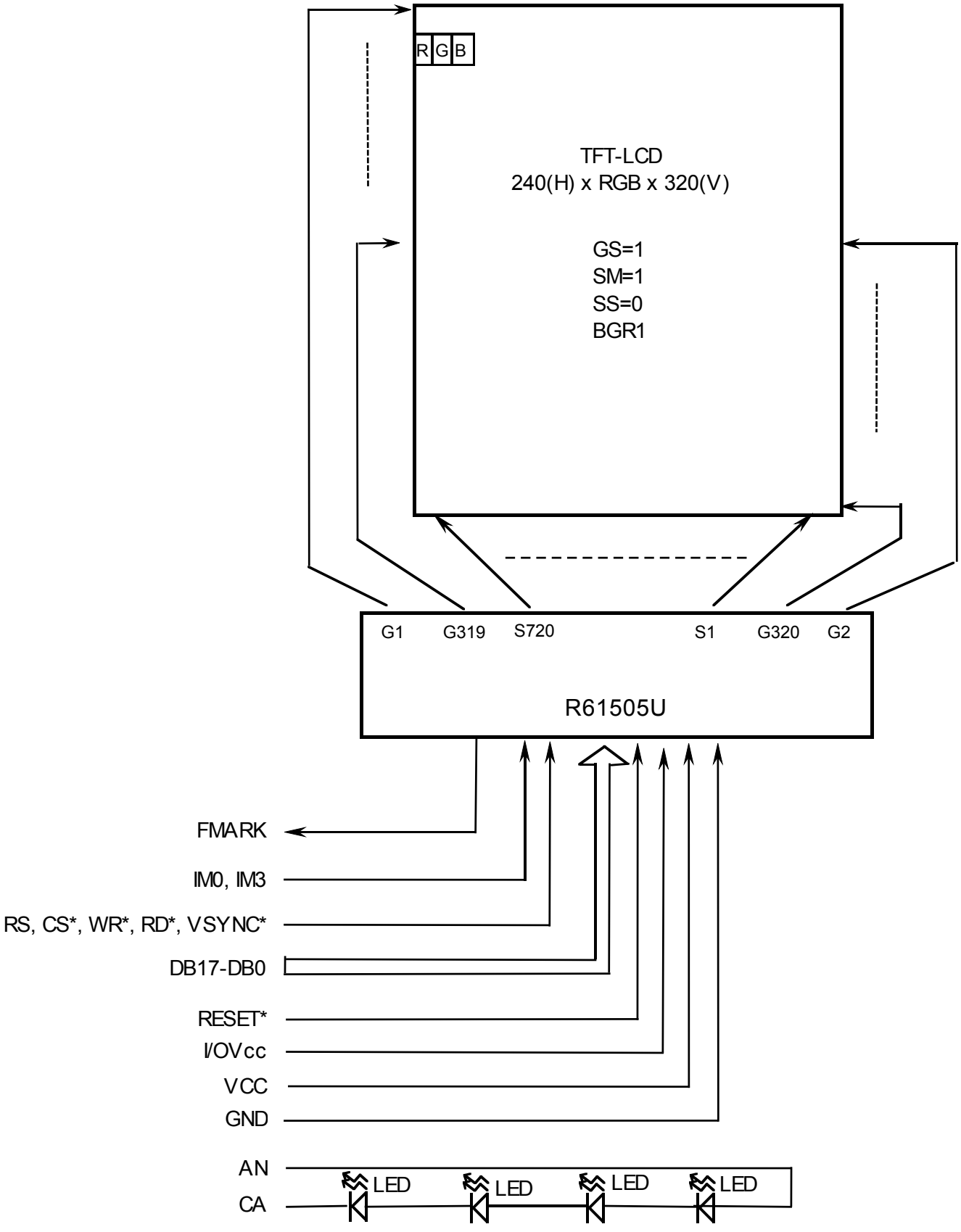


Sensor : BM-5A or equivalent

(8) Definition of optical response time



7. BLOCK DIAGRAM



8. INTERFACE

8.1 INTERNAL PIN CONNECTION (8 / 9 / 16/18-bit CPU bus correspondence)

Pin No.	Signal	Function	Pin No.	Signal	Function
1	GND	GND	21	DB3	Data Bus (Instruction & Display Data)
2	GND	GND	22	DB2	Data Bus (Instruction & Display Data)
3	ID	ID(I/OVcc)	23	DB1	Data Bus (Instruction & Display Data)
4	IM0	MPU Interface Switching	24	DB0	Data Bus (Instruction & Display Data)
5	IM3	MPU Interface Switching	25	RD*	Read
6	RESET*	Reset	26	WR*	Write
7	DB17	Data Bus (Instruction & Display Data)	27	RS	Data/Command Identification
8	DB16	Data Bus (Instruction & Display Data)	28	CS*	Chip Select
9	DB15	Data Bus (Instruction & Display Data)	29	I/OVcc	Power Supply for Interface
10	DB14	Data Bus (Instruction & Display Data)	30	I/OVcc	Power Supply for Interface
11	DB13	Data Bus (Instruction & Display Data)	31	Vcc	Power Supply for Logic and Analog
12	DB12	Data Bus (Instruction & Display Data)	32	Vcc	Power Supply for Logic and Analog
13	DB11	Data Bus (Instruction & Display Data)	33	NC	NC (No Connection)
14	DB10	Data Bus (Instruction & Display Data)	34	AN	Power Supply for LED
15	DB9	Data Bus (Instruction & Display Data)	35	CA	GND for LED
16	DB8	Data Bus (Instruction & Display Data)	36	VSYNC*	Line synchronous signal
17	DB7	Data Bus (Instruction & Display Data)	37	FMARK	Frame head pulse signal
18	DB6	Data Bus (Instruction & Display Data)	38	NC	NC (No Connection)
19	DB5	Data Bus (Instruction & Display Data)	39	GND	GND
20	DB4	Data Bus (Instruction & Display Data)			

Suitable Connector : HIROSE FH26-39S-0.3SHW(5)

8.2 CPU INTERFACE MODE SETTING

8.2.1 CPU Interface Mode Selection

PIN No.	SIGNAL	80-System Bus Interface			
		18-bit	16-bit	9-bit	8-bit
		262k Colors	65k Colors	262k Colors	65k Colors
4	IM0	GND	GND	I/OVcc	I/OVcc
5	IM3	I/OVcc	GND	I/OVcc	GND

Select the interface mode and colors by setting bits of IM0 and IM3.

8.2.2 Unused Data Bus Connection

Bus Interface		**18-bit**	**16-bit**	**9-bit**	**8-bit**
Data Bus Pins		**DB17-0**	**DB17-10 DB8-1**	**DB17-9**	**DB17-10**
Unused Data Bus Pins		**-**	**DB9,DB0**	**DB8-0**	**DB9-0**
Pin No.	**Signal**				
7	**DB17**				
8	**DB16**				
9	**DB15**				
10	**DB14**				
11	**DB13**				
12	**DB12**				
13	**DB11**				
14	**DB10**				
15	**DB9**		**GND or I/OVCC**		**GND or I/OVCC**
16	**DB8**			**GND or I/OVCC**	**GND or I/OVCC**
17	**DB7**			**GND or I/OVCC**	**GND or I/OVCC**
18	**DB6**			**GND or I/OVCC**	**GND or I/OVCC**
19	**DB5**			**GND or I/OVCC**	**GND or I/OVCC**
20	**DB4**			**GND or I/OVCC**	**GND or I/OVCC**
21	**DB3**			**GND or I/OVCC**	**GND or I/OVCC**
22	**DB2**			**GND or I/OVCC**	**GND or I/OVCC**
23	**DB1**			**GND or I/OVCC**	**GND or I/OVCC**
24	**DB0**		**GND or I/OVCC**	**GND or I/OVCC**	**GND or I/OVCC**

Unused data bus pins are to be set at GND or I/OVCC.

8.2.3 Display Data Input

Data Bus		DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
18-bit	Transfer 1	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16-bit	Transfer 1	R5 R0	R4	R3	R2	R1	G5	G4	G3	-	G2	G1	G0	B5 B0	B4	B3	B2	B1	-
9-bit	Transfer 1	R5	R4	R3	R2	R1	R0	G5	G4	G3	-	-	-	-	-	-	-	-	-
	Transfer 2	G2	G1	G0	B5	B4	B3	B2	B1	B0	-	-	-	-	-	-	-	-	-
8-bit	Transfer 1	R5 R0	R4	R3	R2	R1	G5	G4	G3	-	-	-	-	-	-	-	-	-	-
	Transfer 2	G2	G1	G0	B5 B0	B4	B3	B2	B1	-	-	-	-	-	-	-	-	-	-

8.3 INTERFACE TIMING

8.3.1 80-System Bus Interface Timing Characteristics <<18 bits / 16 bits>>

[Normal Write Mode (HWM = 0), I/OVcc = 1.75 to 2.8 V]

Vcc = 2.8 V

Item		Symbol	Unit	Min	Typ	Max
Bus cycle time	Write	tCYCW	ns	132	-	-
	Read	tCYCR	ns	473	-	-
Write low-level pulse width		PWLW	ns	48	-	-
Read low-level pulse width		PWLR	ns	179	-	-
Write high-level pulse width		PWHW	ns	74	-	-
Read high-level pulse width		PWHR	ns	263	-	-
Write/read rise/fall time		tWRr, tWRf	ns	-	-	23
Set up time	Write (RS to CS*, WR*)	tAS	ns	0	-	-
	Read (RS to CS*, RD*)	tAS	ns	11	-	-
Address hold time		tAH	ns	3	-	-
Write data set up time		tDSW	ns	27	-	-
Write data hold time		tH	ns	11	-	-
Read data delay time		tDDR	ns	-	-	142
Read data hold time		tDHR	ns	6	-	-

[High-Speed Write Mode (HWM = 1), I/OVcc = 1.75 to 2.8 V]

Vcc = 2.8 V

Item		Symbol	Unit	Min	Typ	Max
Bus cycle time	Write	tCYCW	ns	79	-	-
	Read	tCYCR	ns	473	-	-
Write low-level pulse width		PWLW	ns	42	-	-
Read low-level pulse width		PWLR	ns	179	-	-
Write high-level pulse width		PWHW	ns	27	-	-
Read high-level pulse width		PWHR	ns	263	-	-
Write/read rise/fall time		tWRr, tWRf	ns	-	-	23
Set up time	Write (RS to CS*, WR*)	tAS	ns	0	-	-
	Read (RS to CS*, RD*)	tAS	ns	11	-	-
Address hold time		tAH	ns	3	-	-
Write data set up time		tDSW	ns	27	-	-
Write data hold time		tH	ns	11	-	-
Read data delay time		tDDR	ns	-	-	142
Read data hold time		tDHR	ns	6	-	-

8.3.2 80-System Bus Interface Timing Characteristics <<9 bits / 8 bits>>

[Normal Write Mode (HWM=0)/High-Speed Write Mode (HWM=1), I/OVcc=1.75 to 2.8V]

Vcc = 2.8 V

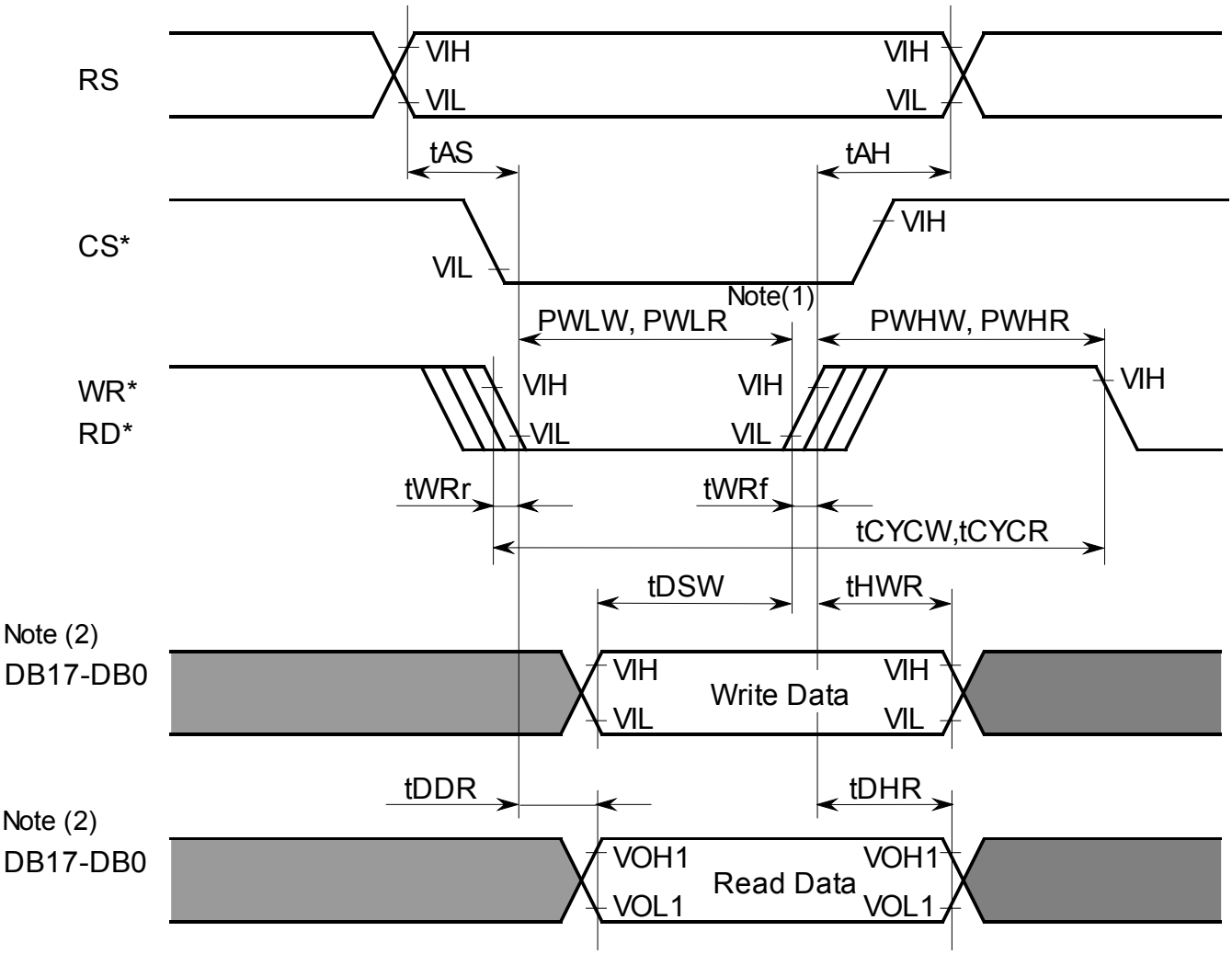
Item		Symbol	Unit	Min	Typ	Max
Bus cycle time	Write	tCYCW	ns	74	-	-
	Read	tCYCR	ns	473	-	-
Write low-level pulse width		PWLW	ns	32	-	-
Read low-level pulse width		PWLR	ns	179	-	-
Write high-level pulse width		PWHW	ns	27	-	-
Read high-level pulse width		PWHR	ns	263	-	-
Write/Read rise/fall time		tWRr, tWRf	ns	-	-	23
Set up time	Write (RS to CS*, WR*)	tAS	ns	0	-	-
	Read (RS to CS*, RD*)	tAS	ns	11	-	-
Address hold time		tAH	ns	3	-	-
Write data set up time		tDSW	ns	27	-	-
Write data hold time		tH	ns	11	-	-
Read data delay time		tDDR	ns	-	-	142
Read data hold time		tDHR	ns	6	-	-

8.3.3 Reset Timing Characteristics

[I/OVcc=1.75 to 2.8V]

Vcc = 2.8 V

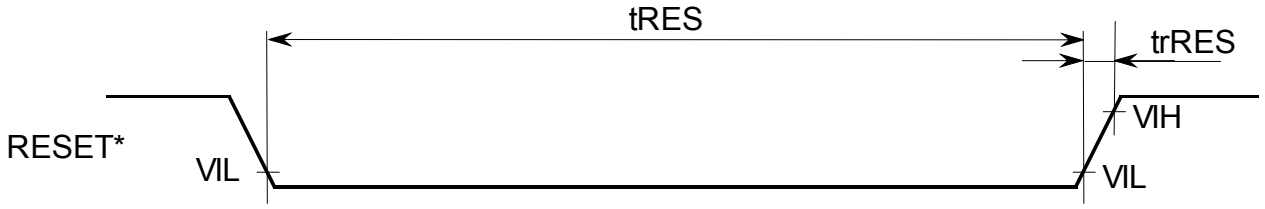
Item	Symbol	Unit	Min	Typ	Max
Reset low-level width	tRES	ms	2	-	-
Reset rise time	trRES	us	-	-	9



Bus Timing

Notes (1) PWLW and PWLR are defined by the overlap period when CS* is low and when WR* or RD* is low.

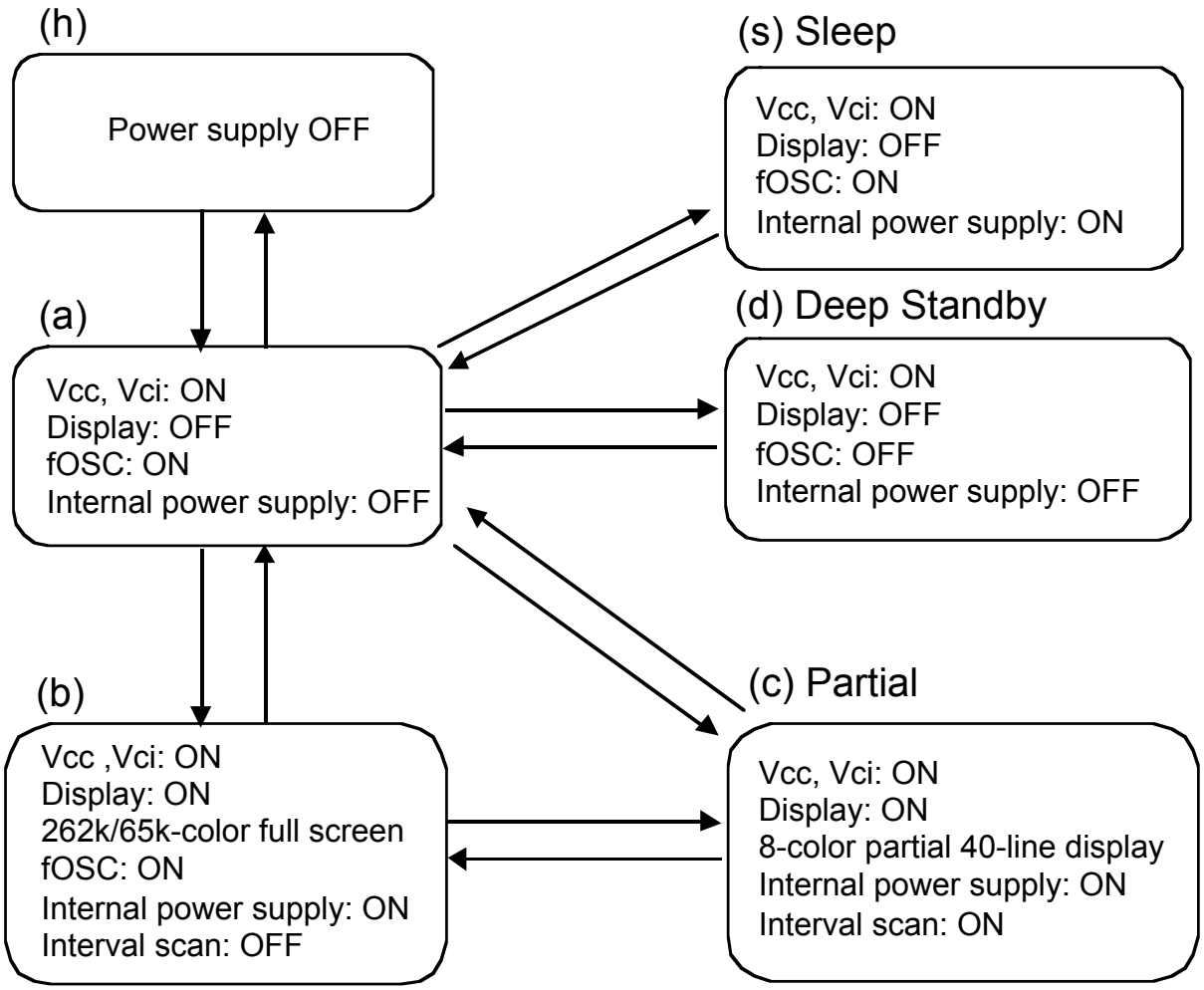
(2) Fix unused DB pins to either Vcc or GND level.



Reset Timing

8.4 REGISTER SETTING

8.4.1 State Transition Diagram of Operation Mode



8.4.2 Sequence

State (h) to (a)

last proporsal

1	Power supply ON	Vcc ON	
2		IoVcc ON	
3		Vci ON	
4		reset* = "L"	
5	Reset	wait	1 ms min
6		reset* = "H"	
7		wait	2 ms
8	Data transfer synchronization	RS=0,DB=0x0000	
9		RS=0,DB=0x0000	
10		RS=0,DB=0x0000	
11		RS=0,DB=0x0000	

State (a) to (h)

last proporsal

1	Power supply OFF	Vci OFF	
2		ioVcc OFF	
3		Vcc OFF	

State (b) to (a), (c) to (a)

last proporsal

1	Display off	R07h	0x0072
2		wait	2 frame
3		R07h	0x0001
4		wait	8 line
5		R07h	0x0000
6	Amplifier OFF	R09h	0x0000
7		R10h	0x0080
8		R11h	0x0660
9		R12h	0x0000
10		wait	30 ms
11		R10h	0x0000

State (a) to (s)

last proporsal

1	Sleep	R10h	0x0002

State (s) to (a)

last proporsal

1	Sleep mode cancellation	R10h	0x0000
2		wait	1 clock Min

State (b) to (c)

last proporsal

1	Display off	R07h	0x0073	
2		wait	2frame min	
3		R02h	0x0400	
4		R10h	0x17A0	
5	Horizontal RAM start address	R50h	0x0000	
6	Horizontal RAM end address	R51h	0x00EF	
7	Vertical RAM start address	R52h	0x0000	
8	Vertical RAM end address	R53h	0x0027	
9	ISC ON	R09h	0x0401	
10	Frame frequency control	R90h	0x0015	
11		wait	2frame min	
12		R20h	0x0000	
13		R21h	0x0000	
14	Write data to GRAM	R22h	-	
15		Display data write		240x40 size
16	Display	R07h	0x107B	
17	Image refresh	R20h	0x0000	
18		R21h	0x0000	
19	Write data to GRAM	R22h	-	
20		Display data write		240x40 size

State (c) to (b)

last proporsal

1	Display off	R07h	0x0073	
2		wait	2frame min	
3	ISC OFF	R09h	0x0000	
4	Power setting	R02h	0x0400	
5		R10h	0x17B0	
7	Vertical RAM end address	R53h	0x013F	
8	Frame frequency control	R90h	0x0015	
9		wait	2frame min	
10		R20h	0x0000	
11		R21h	0x0000	
12	Write data to GRAM	R22h	-	
13		Display data write		240x320 size
14	Display	R07h	0x0173	
15	Image refresh	R20h	0x0000	
16		R21h	0x0000	
17	Write data to GRAM	R22h	-	
18		Display data write		240x320 size

State (a) to (b)				
				last proporsal
1		RA4h	0x0001	
2		wait	1ms	
3	Power sequence control	R07h	0x0021	
4		wait	10 ms	
5		R17h	0x0001	
6		wait	10 ms	
7		R19h	0x0000	
8	Power start (1)	R10h	0x17B0	
9		R11h	0x0016	
10		R12h	0x019E	0x009E
11		R13h	0x1600	
12		R14h	0x8000	
13		wait	10 ms	
14	Power start (2)	R12h	0x01BE	0x00BE
15		wait	120 ms	
16	Driver output control	R01h	0x0500	
17	LCD driving wave control	R02h	0x0400	
18	Entry mode	R03h	0x1230	
19	Display control (2)	R08h	0x0808	
20	ISC control	R09h	0x0000	
21	Display control (4)	R0Ah	0x0008	
22		R0Ch	0x0000	
23		R0Dh	0x0000	
24	Gamma setting	R30h	0x0704	0x0703
25		R31h	0x0003	0x0001
26		R32h	0x0000	0x0004
27		R33h	0x0103	0x0102
28		R34h	0x0000	0x0300
29		R35h	0x0006	0x0103
30		R36h	0x001F	0x001F
31		R37h	0x0704	0x0703
32		R38h	0x0003	0x0001
33		R39h	0x0000	0x0004
34		R3Ah	0x0103	0x0102
35		R3Bh	0x0000	0x0300
36		R3Ch	0x0006	0x0103
37		R3Dh	0x001F	0x001F
38	Horizontal RAM start address	R50h	0x0000	
39	Horizontal RAM end address	R51h	0x00EF	
40	Vertical RAM start address	R52h	0x0000	
41	Vertical RAM end address	R53h	0x013F	
42		R60h	0x2700	
43		R61h	0x0000	
44		R6Ah	0x0000	
45		R80h	0x0000	
46		R81h	0x0000	
47		R82h	0x0027	
48	Frame frequency control	R90h	0x0015	
49		R92h	0x0000	
50		R93h	0x0002	
51		R20h	0x0000	
52		R21h	0x0000	
53	Write data to GRAM	R22h	-	
54		Display data write		240x320 size
55	Display ON	R07h	0x0021	
56		wait	8 line min	
57		R10h	0x17B0	
58		R11h	0x0017	
59		R07h	0x0061	
60		wait	2 frame min	
61		R07h	0x0173	
62	Image refresh	R20h	0x0000	
63		R21h	0x0000	
64		R22h	-	
65		Display data write		240x320 size

State (a) to (b)				
				last proporsal
1		RA4h	0x0001	
2		wait	1ms	
3	Power sequence control	R07h	0x0021	
4		wait	10 ms	
5		R17h	0x0001	
6		wait	10 ms	
7		R19h	0x0000	
8	Power start (1)	R10h	0x17B0	
9		R11h	0x0016	
10		R12h	0x019E	0x009E
11		R13h	0x1600	
12		R14h	0x8000	
13		wait	10 ms	
14	Power start (2)	R12h	0x01BE	0x00BE
15		wait	120 ms	
16	Driver output control	R01h	0x0500	
17	LCD driving wave control	R02h	0x0400	
18	Entry mode	R03h	0x1230	
19	Display control (2)	R08h	0x0808	
20	ISC control	R09h	0x0401	
21	Display control (4)	R0Ah	0x0008	
22		R0Ch	0x0000	
23		R0Dh	0x0000	
24	Gamma setting	R30h	0x0704	0x0703
25		R31h	0x0003	0x0001
26		R32h	0x0000	0x0004
27		R33h	0x0103	0x0102
28		R34h	0x0000	0x0300
29		R35h	0x0006	0x0103
30		R36h	0x001F	0x001F
31		R37h	0x0704	0x0703
32		R38h	0x0003	0x0001
33		R39h	0x0000	0x0004
34		R3Ah	0x0103	0x0102
35		R3Bh	0x0000	0x0300
36		R3Ch	0x0006	0x0103
37		R3Dh	0x001F	0x001F
38	Horizontal RAM start address	R50h	0x0000	
39	Horizontal RAM end address	R51h	0x00EF	
40	Vertical RAM start address	R52h	0x0000	
41	Vertical RAM end address	R53h	0x0027	
42		R60h	0x2700	
43		R61h	0x0000	
44		R6Ah	0x0000	
45		R80h	0x0000	
46		R81h	0x0000	
47		R82h	0x0027	
48	Frame frequency control	R90h	0x0015	
49		R92h	0x0000	
50		R93h	0x0002	
51		R20h	0x0000	
52		R21h	0x0000	
53	Write data to GRAM	R22h	-	
54		Display data write		240x40 size
55	Display ON	R07h	0x0021	
56		wait	8 line min	
57		R10h	0x17B0	
58		R11h	0x0017	
59		R07h	0x0061	
60		wait	2 frame min	
61		R07h	0x107B	
62	Image refresh	R20h	0x0000	
63		R21h	0x0000	
64		R22h	-	
65		Display data write		240x40 size

State (a) to (d)

last proporsal

1	Deep Standby	R10h	0x0004

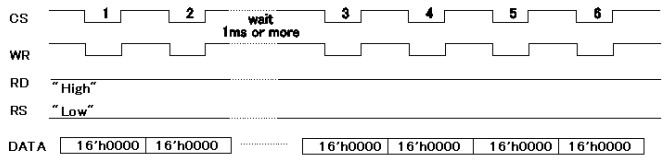
State (d) to (a)

last proporsal

Cancel deep standby mode by inputting CS="Low" and WR="Low" (9-/ 8-bit interface)

1	DSTB mode cancellation (1)	Index write(DATA=8'h00)		*1
2	DSTB mode cancellation (2)	Index write(DATA=8'h00)		
3		wait	1ms min	
4	DSTB mode cancellation (3)	Index write(DATA=8'h00)		
5	DSTB mode cancellation (4)	Index write(DATA=8'h00)		
6	DSTB mode cancellation (5)	Index write(DATA=8'h00)		
7	DSTB mode cancellation (6)	Index write(DATA=8'hF0)		
8		wait	50 ms	

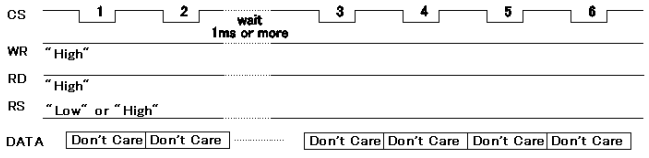
*1 Data Transfer



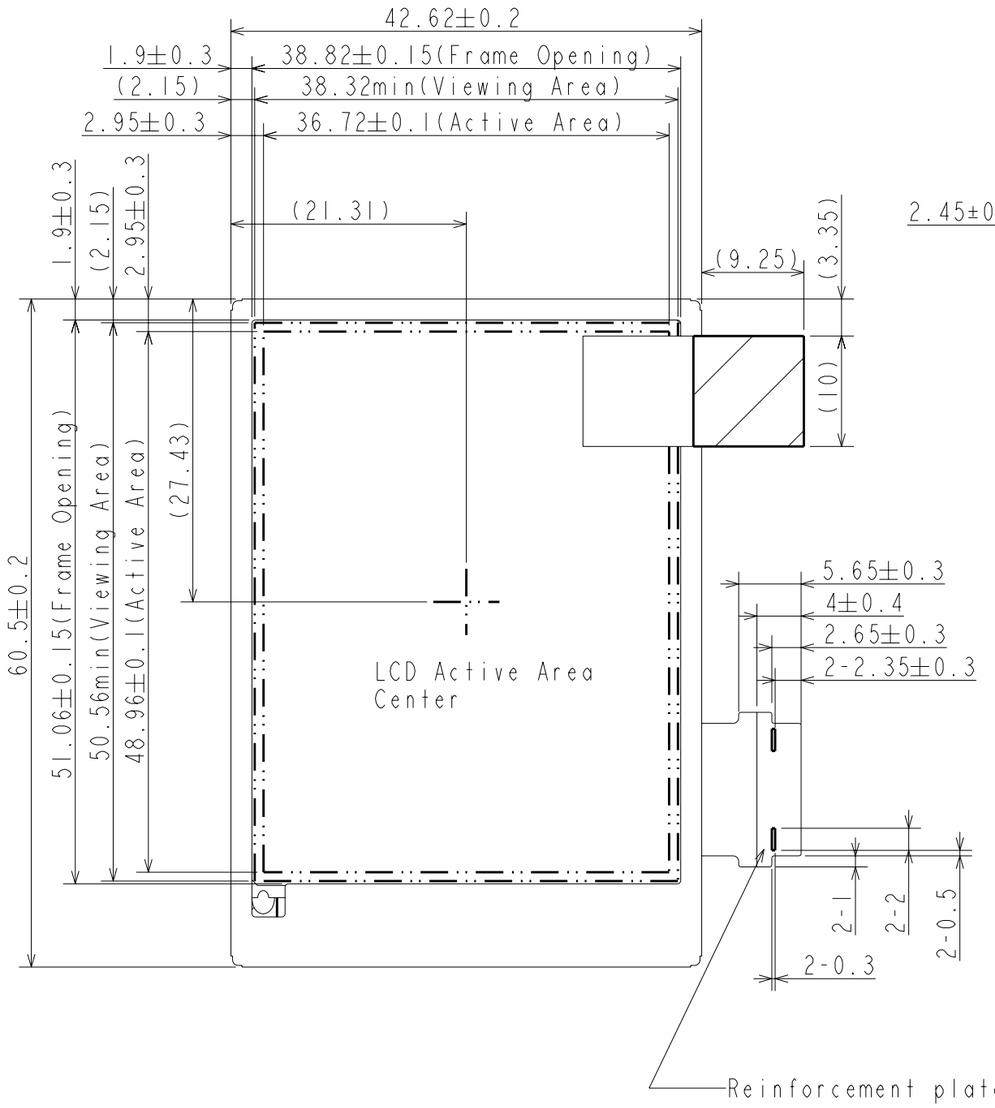
Cancel deep standby mode by inputting CS="Low" (18-/ 16-/ 9-/ 8-bit interface)

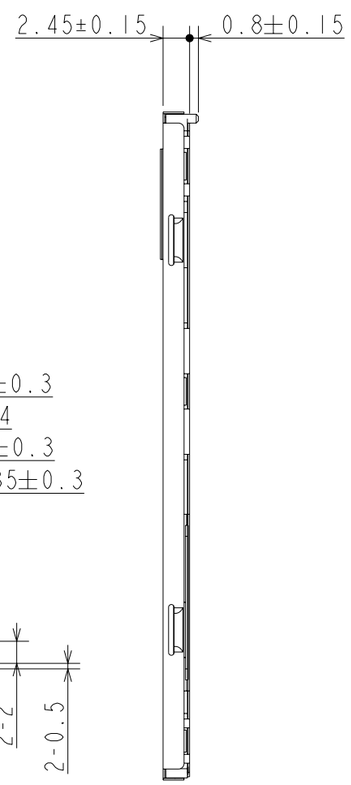
1	DSTB mode cancellation (1)	CS="Low"		*2
2	DSTB mode cancellation (2)	Index write(DATA=8'h00)		
3		wait	1ms	
4	DSTB mode cancellation (3)	CS="Low"		
5	DSTB mode cancellation (4)	CS="Low"		
6	DSTB mode cancellation (5)	CS="Low"		
7	DSTB mode cancellation (6)	CS="Low"		
8		wait	10 ms	

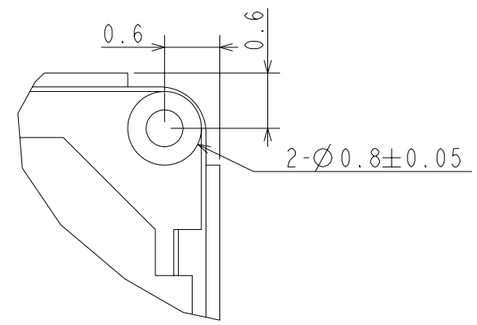
*2 Data Transfer



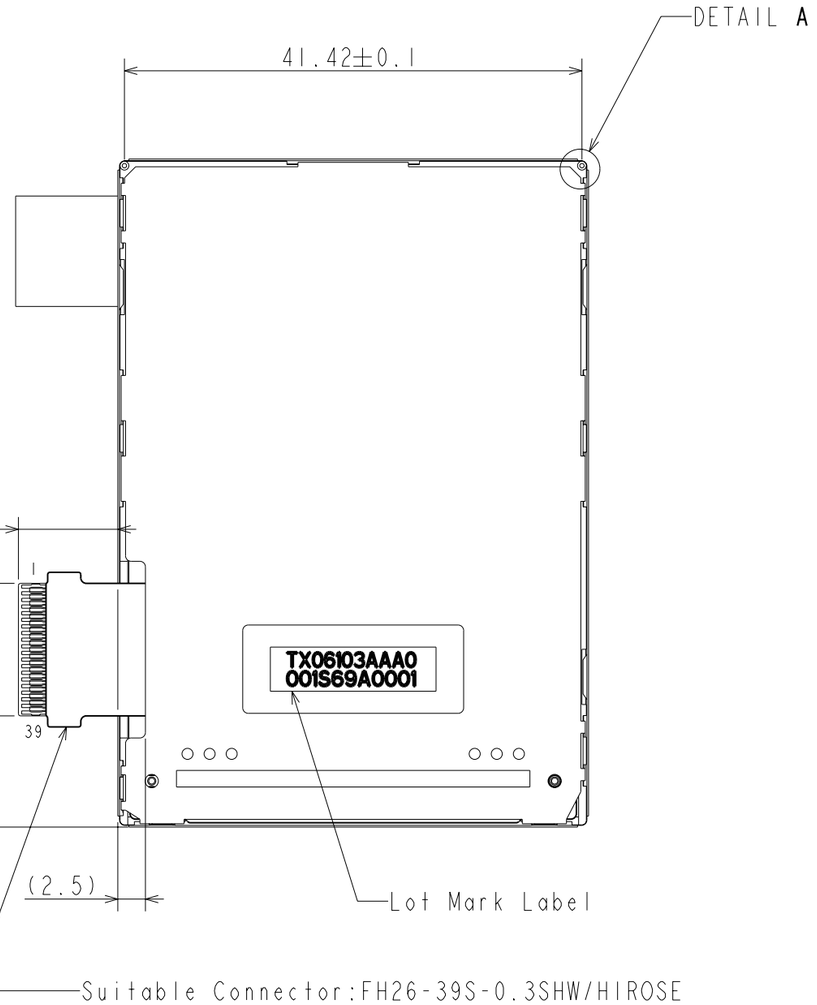
9. DIMISIONNAL OUTLINE







DETAIL A



Unit:mm
Note
(1) The unspecified to tolerance:±0.2

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