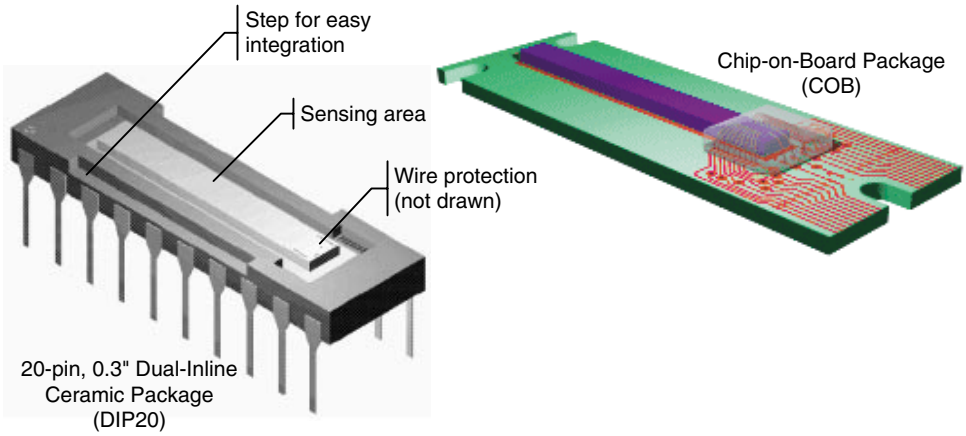
Features

- Sensitive Layer Over a 0.8 µm CMOS Array
- Image Zone: 0.4 x 14 mm = 0.02" x 0.55"
- Image Array: 8 x 280 = 2240 pixels
- Pixel Pitch: 50 µm x 50 µm = 500 dpi
- Pixel Clock: up to 2 MHz Enabling up to 1780 Frames per Second
- Die Size: 1.7 x 17.3 mm
- Operating Voltage: 3V to 5.5V
- Naturally Protected Against ESD: > 16 kV Air Discharge
- Power Consumption: 20 mW at 3.3V, 1 MHz, 25°C
- Operating Temperature Range: 0°C to +70°C: C suffix
- Resistant to Abrasion: >1 Million Finger Sweeps
- Chip-On-Board (COB) package or 20-lead Ceramic DIP available for development, with Specific Protective Layer

Applications

- PDA (Access Control, Data Protection)
- Cellular Phones, SmartPhone (Access e-business)
- Notebook, PC-add on (Access Control, e-business)
- PIN Code Replacement
- Automated Teller Machine, POS
- Building Access
- Electronic Keys (Cars, Home,...)
- Portable Fingerprint Imaging for Law Enforcement
- TV Access

Figure 1. Fingerchip Packages



Thermal Fingerprint Sensor with 0.4 mm x 14 mm (0.02" x 0.55") Sensing Area and Digital Output (On-chip ADC)

FCD4B14 FingerChip™

Rev. 1962C–01/02

Table 1. Pin Description For DIP Ceramic Package

Pin Number	Name	Type
1	GND	GND
2	AVE	Analog output
3	TPP	Power
4	VCC	Power
5	RST	Digital input
6	OE	Digital input
7	De0	Digital output
8	De1	Digital output
9	De2	Digital output
10	De3	Digital output
11	FPL	GND
12	Do3	Digital output
13	Do2	Digital output
14	Do1	Digital output
15	Do0	Digital output
16	GND	GND
17	ACKN	Digital output
18	PCLK	Digital input
19	TPE	Digital input
20	AVO	Analog output

Die Attach is connected to pin 1 and 16, and must be grounded. FPL pin must be grounded.

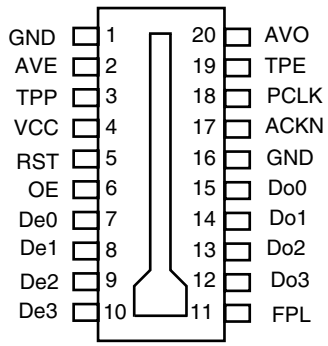
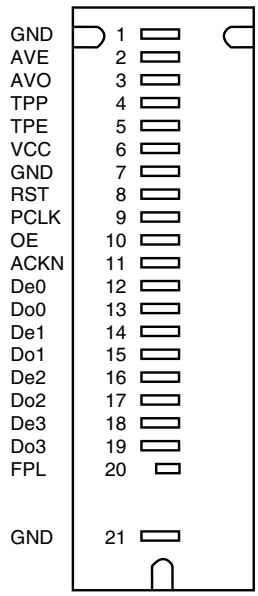


Table 2. Pin Description For Chip-On-Board Package

Pin Number	Name	Type
1	GND	GND
2	AVE	Analog output
3	AVO	Analog output
4	TPP	Power
5	TPE	Digital input
6	VCC	Power
7	GND	GND
8	RST	Digital input
9	PCLK	Digital input
10	OE	Digital input
11	ACKN	Digital output
12	De0	Digital output
13	Do0	Digital output
14	De1	Digital output
15	Do1	Digital output
16	De2	Digital output
17	Do2	Digital output
18	De3	Digital output
19	Do3	Digital output
20	FPL	GND
21	GND	GND

Die Attach is connected to pin 1, 7 and 21, and must be grounded. FPL pin must be grounded.



Description

FCD4B14 is part of the FingerChip Atmel monolithic fingerprint sensor family for which no optics, no prism and no light source are required.

FCD4B14 is a single chip, high performance, low cost sensor based on temperature physical effects for fingerprint sensing.

FCD4B14 has a linear shape, allowing for the capture of a fingerprint image by sweeping the finger across the sensing area. After capturing several images, Atmel proprietary software can reconstruct a full 8-bit fingerprint image, if needed.

FCD4B14 has a small surface combined with CMOS technology, and a Chip-On-Board or ceramic dual-in-line package assembly. These facts contribute to a low-cost device.

FCD4B14 delivers a programmable number of images per second, while an integrated Analog to Digital Converter delivers a digital signal adapted to interfaces such as an EPP parallel port, USB microcontroller or directly to micro-processors. Thus, no frame grabber or glue interface is necessary to send the frames. These facts make FCD4B14 an easy device to include in any system for identification or verification applications.

Table 3. Absolute Maximum Ratings[1]

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{CC}		GND to 6.5	V
Temperature stabilization power	TPP		GND to 6.5	V
Front plane	FPL		GND to V_{CC}	V
Digital input voltage	RST PCLK		GND to V_{CC}	V
Storage temperature	T_{stg}		-50 to +85	°C
Lead temperature (soldering, 10 seconds.)	T_{leads}	Do not solder DIP: socket mandatory	**Forbidden**	°C

Note: 1. Absolute maximum ratings are limiting values, to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum ratings may affect device reliability.

Table 4. Recommended Conditions Of Use

Parameter	Symbol	Comments	Min	Typ	Max	Unit
Positive supply voltage	V_{CC}		3V	5V	5.5V	V
Front plane	FPL	Must be grounded	GND			V
Digital input voltage			CMOS levels			V
Digital output voltage			CMOS levels			V
Digital load	C_L				50	pF
Analog load	C_A R_A	Not connected				pF kΩ
Operating temperature range	T_{amb}	Civil: “C” grade	0 to +70			°C
Maximum current on TPP	ITPP		0		100	mA

Table 5. Resistance

Parameter	Min Value	Standard Method
ESD		
On pins. HBM (Human Body Model) CMOS I/O	2 kV	MIL-STD-883- method 3015.7
On die surface (Zapgun) Air discharge	±16 kV	NF EN 6100-4-2
MECHANICAL ABRASION		
Number of cycles without lubricant multiply by a factor of 20 for correlation with a real finger	200 000	MIL E 12397B
CHEMICAL RESISTANCE		
Cleaning agent, acid, grease, alcohol, diluted acetone	4 hours	Internal method

Table 6. Specifications

Explanation Of Test Levels	
I	100% production tested at +25°C
II	100% production tested at +25°C, and sample tested at specified temperatures (AC testing done on sample)
III	Sample tested only
IV	Parameter is guaranteed by design and/or characterization testing
V	Parameter is a typical value only
VI	100% production tested at temperature extremes
D	100% probe tested on wafer at T_{amb} = +25°C

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Resolution		IV		50		micron
Size		IV		8x280		pixel
Yield: number of bad pixels		I			15	bad pixels
Equivalent resistance on TPP pin		I	23	30	47	Ω

Table 7. 5V. Power supply = +5V; T_{amb} = 25°C; F_{PCLK} = 1 MHz; Duty cycle = 50%; C_{load} 120 pF on digital outputs, analog outputs disconnected otherwise specified.

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Power Requirements						
Positive supply voltage	V_{CC}		4.5	5	5.5	V
Digital positive supply current on V_{CC} pin		I		7	10	mA
C_{load} = 0	I_{CC}	IV		5	6	mA
Power dissipation on V_{CC}		I		35	50	mW
C_{load} = 0	P_{CC}	IV		25	30	mW
Current on V_{CC} in NAP mode	I_{CCNAP}	I			10	µA
Analog Output						
Voltage range	V_{AVx}	I	0		2.9	V
Digital Inputs						
Logic compatibility				CMOS		
Logic “0” voltage	V_{IL}	I	0		1.2	V
Logic “1” voltage	V_{IH}	I	3.6		VCC	V
Logic “0” current	I_{IL}	I	-10		0	µA
Logic “1”current	I_{IH}	I	0		10	µA
Digital Outputs						
Logic compatibility				CMOS		
Logic “0” voltage(1)	V_{OL}	I			1.5	V
Logic “1” voltage(1)	V_{OH}	I	3.5			V

Note: 1. With I_{OL} = 1 mA and I_{OH} = -1 mA

Table 8. 3.3V. Power supply = +3.3V; T_{amb} = 25°C; F_{PCLK} = 1 MHz; Duty cycle = 50%; C_{load} 120 pF on digital outputs, analog outputs disconnected otherwise specified

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Power Requirements						
Positive supply voltage	V_{CC}		3.0	3.3	3.6	V
Digital positive supply current on V_{CC} pin C_{load}= 0	I_{CC}	I IV		6 5	10 6	mA mA
Power dissipation on V_{CC} C_{load} = 0	P_{CC}	I IV		20 17	33 20	mW mW
Current on V_{CC} in NAP mode	I_{CCNAP}	I			10	µA
Analog Output						
Voltage range	V_{AVx}	I	0		2.9	V
Digital Inputs						
Logic compatibility				CMOS		
Logic “0” voltage	V_{IL}	I	0		0.8	V
Logic “1” voltage	V_{IH}	I	2.3		VCC	V
Logic “0” current	I_{IL}	I	-10		0	µA
Logic “1”current	I_{IH}	I	0		10	µA
Digital Outputs						
Logic compatibility				CMOS		
Logic “0” voltage(1)	V_{OL}	I			0.6	V
Logic “1” voltage(1)	V_{OH}	I	2.4			V

Note: 1. With I_{OL} = 1 mA and I_{OH} = -1 mA

Table 9. Switching Performances. T_{amb} = 25°C; F_{PCLK} = 1 MHz; Duty cycle = 50%; C_{load} 120 pF on digital and analog outputs otherwise specified

Parameter	Symbol	Test level	Min	Typ	Max	Unit
Clock frequency	f_{PCLK}	I	0.5	1	2	MHz
Clock pulse width (high)	t_{HCLK}	I	250			ns
Clock pulse width (low)	t_{LCLK}	I	250			ns
Clock setup time (high)/reset falling edge	t_{Setup}	I			0	ns
No data change	t_{NOOE}	IV	100			ns

Table 10. 5.0V. All power supplies = +5 V

Parameter	Symbol	Test level	Min	Typ	Max	Unit
Output delay from PCLK to ACKN rising edge	$t_{PLHACKN}$	I			85	ns
Output delay from PCLK to ACKN falling edge	$t_{PHLACKN}$	I			80	ns
Output delay from PCLK to Data output Dxi	t_{PDATA}	I			70	ns
Output delay from PCLK to Analog output Avx	$t_{PAVIDEO}$	I			170	ns
Output delay from OE to data high-Z	t_{DATAZ}	IV		25		ns
Output delay from OE to data output	t_{ZDATA}	IV		29		ns

Table 11. 3.3V. All power supplies = +3.3 V

Parameter	Symbol	Test level	Min	Typ	Max	Unit
Output delay from PCLK to ACKN rising edge	$t_{PLHACKN}$	I			110	ns
Output delay from PCLK to ACKN falling edge	$t_{PHLACKN}$	I			95	ns
Output delay from PCLK to Data output Dxi	t_{PDATA}	I			85	ns
Output delay from PCLK to Analog output AVx	$t_{PAVIDEO}$	I			190	ns
Output delay from OE to data high-Z	t_{DATAZ}	IV		34		ns
Output delay from OE to data output	t_{ZDATA}	IV		47		ns

Figure 2. Reset

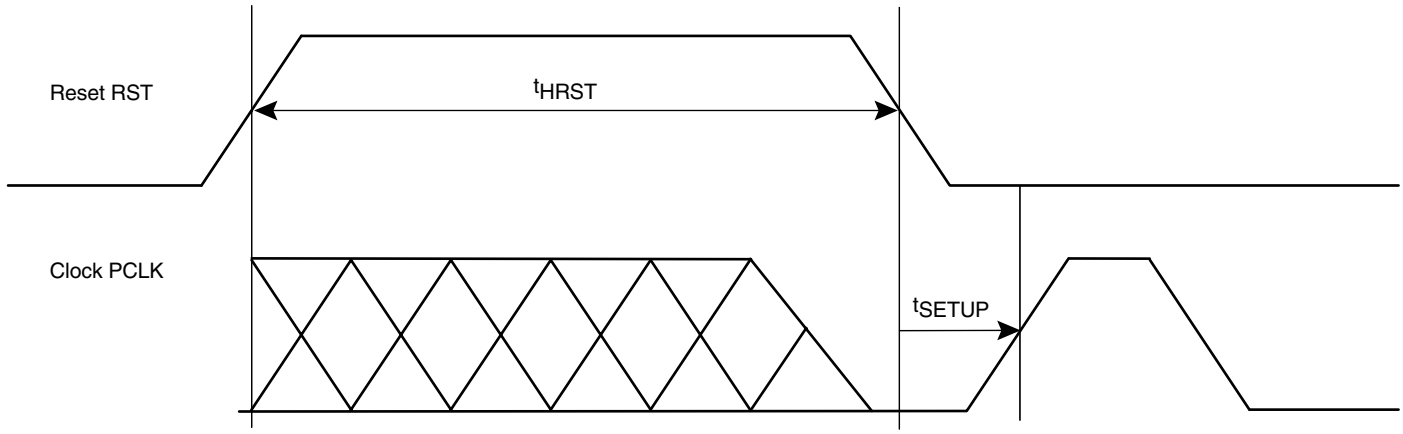


Figure 3. Read One Byte/Two Pixels

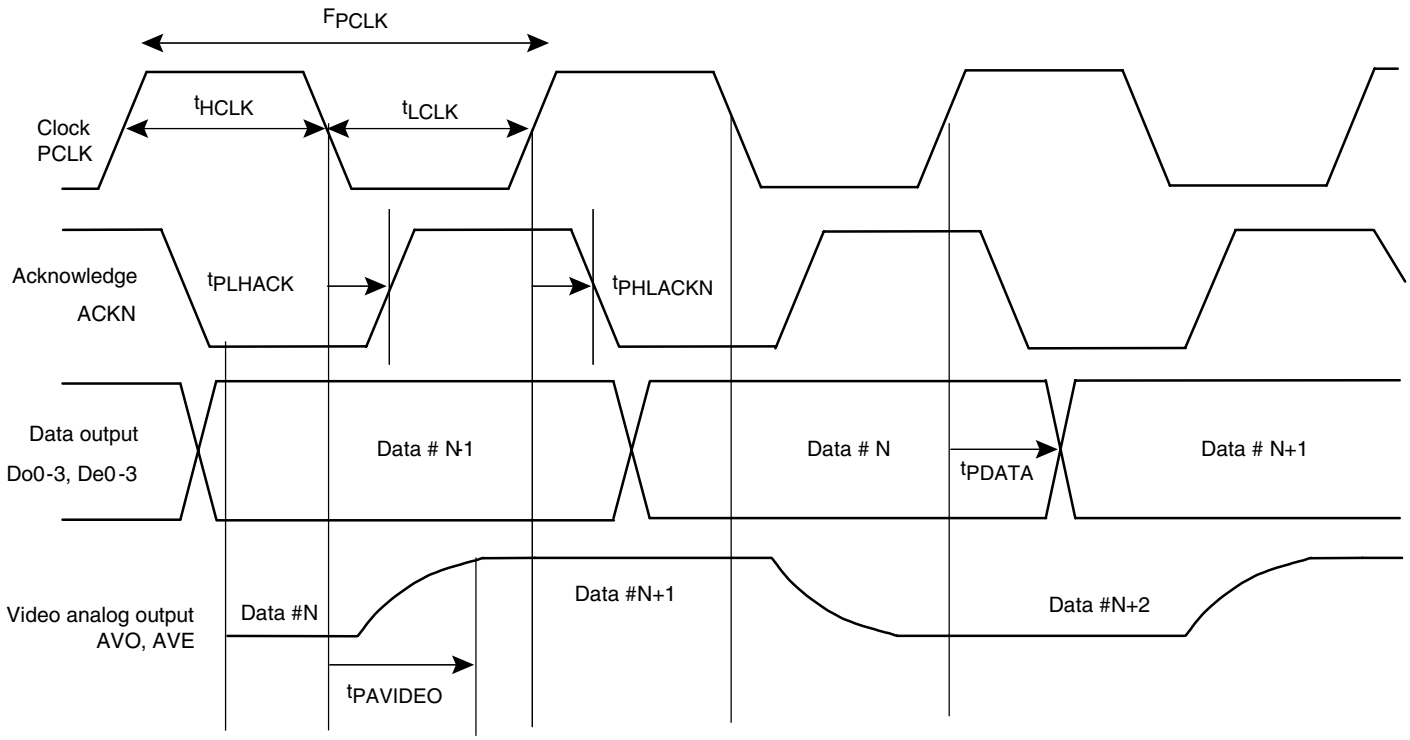


Figure 4. Output Enable

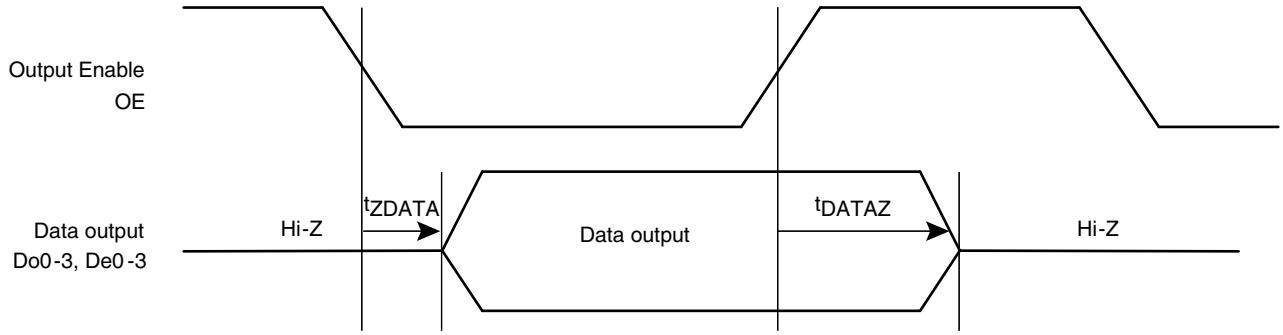
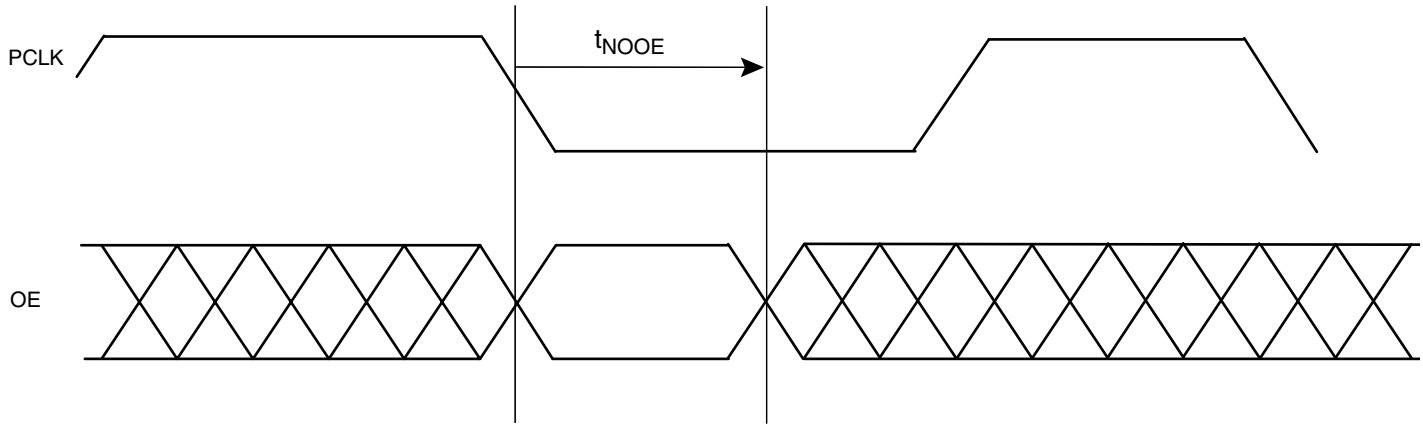
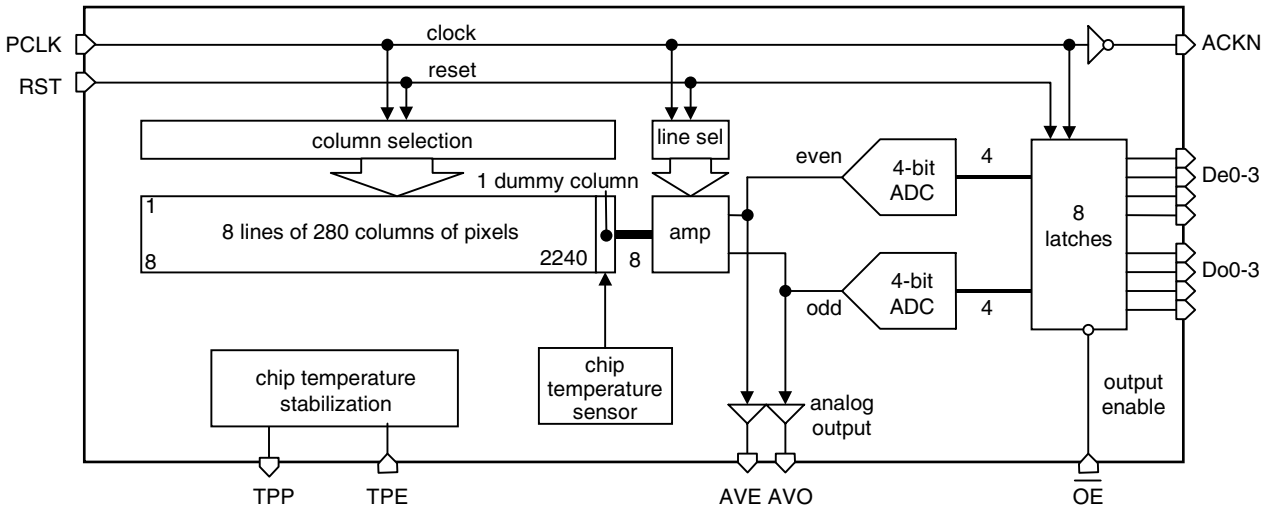


Figure 5. No data change



Note: OE must not change during TNOOE after the PCLK falls. This is to ensure that the output drivers of the data is not driving current, to reduce the noise level on the power supply.

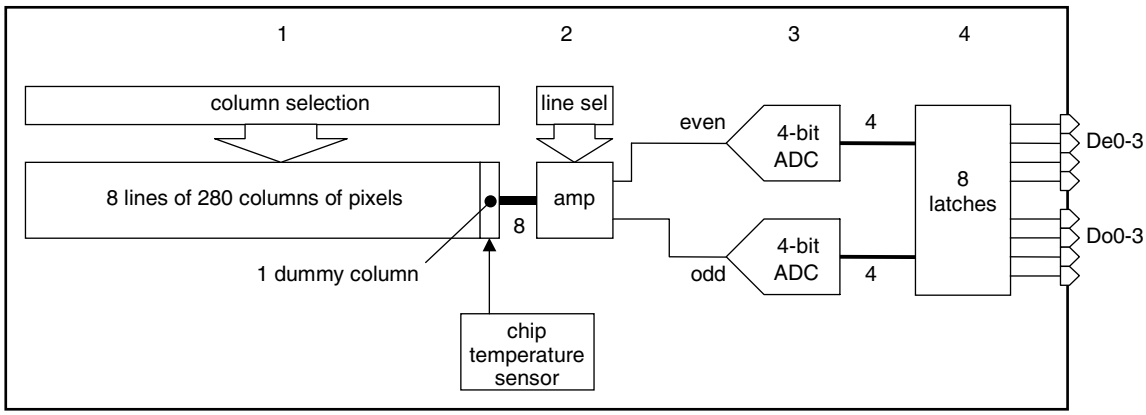
Figure 6. FCD4B14 Block Diagram



Functional Description

The circuit is divided into two main sections: sensor and data conversion. One particular column among 280+1 is selected in the sensor array (1), then each pixel of the selected column sends its electrical information to amplifiers (2) (one per line), then two lines at a time are selected (odd and even) so that two particular pixels send their information to the input of two 4-bit Analog-to-Digital Converters (3), so 2 pixels can be read for each clock pulse (4).

Figure 7. Functional Description



Sensor

Each pixel is a sensor in itself. The sensor detects a temperature differential between the beginning of acquisition and the reading of information: this is the integration time. The integration time begins with a reset of the pixel to a predefined initial state. Note that the integration time reset has nothing to do with the reset of the digital section.

Then, at a rate depending on the sensitivity of the pyroelectric layer, on the temperature variation between the reset and the end of the integration time, and on the duration of the integration time, electrical charges are generated at the pixel level.

Analog-to-Digital Converter/ Reconstructing an 8-bit Fingerprint Image

An Analog-to-Digital Converter (ADC) is used to convert the analog signal coming from the pixel into digital data that can be used by a processor.

As the data rate for parallel port and USB is in the range of 1 MB per second and at least a rate of 500 frames per second is needed to reconstruct the image with a fair sweeping speed for the finger, two 4-bit ADCs have been used to output 2 pixels at a time on 1 byte.

Start Sequence

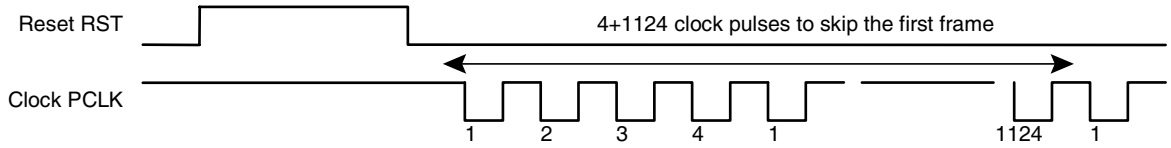
A reset is not necessary between each frame acquisition!

Start sequence must consist of:

1. Set the RST pin to high
2. Set the RST pin to low
3. Send 4 clock pulses (due to pipe-line)
4. Send clock pulses to skip the first frame

Note that the first frame never contains relevant information because the integration time is not correct.

Figure 8. Start Sequence



Reading the Frames

A frame consists of 280 true columns + 1 dummy column of 8 pixels. As two pixels are output at a time, a system must send 281x4 = 1124 clock pulses to read one frame.

Reset must be low when reading the frames.

Read One Byte/Output Enable

Clock is taken into account on the falling edge and data are output on the rising edge.

For each clock pulse, after the start sequence, a new byte is output on the Do0-3, De0-3 pins. This byte contains 2 pixels: 4-bit on Do0-3 (odd pixels), 4-bit on De0-3 (even pixels).

To output the data, the output enable (OE) pin must be low. When OE is high, the Do0-3 and De0-3 pins are in high impedance state. This enables an easy connection to a microprocessor bus without additional circuitry-it will enable data output by using a chip select signal. Note that the FCD4B14 is always sending data: there is no data exchange to perform using read/write mode.

Power Supply Noise

IMPORTANT: When a falling edge is applied on OE (i.e when the Output Enable becomes active), then some current is drained from the power supply to drive the 8 outputs, producing some noise. It is important to avoid such noise just after the falling edge of the clock PCLK, when the pixels information is evaluated: the timing diagram figure 5 and time T_{NOOE} defines the interval time where the power supply must be as quiet as possible.

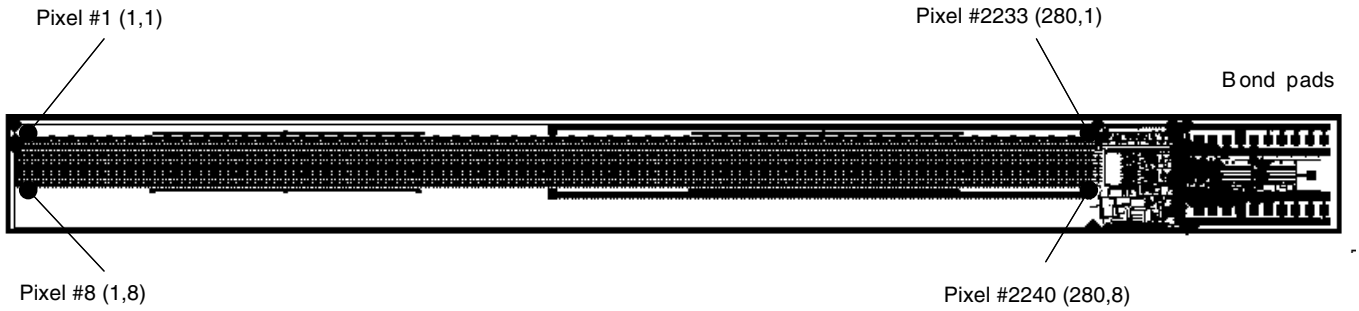
Video Output

An analog signal is also available on pins AVE and AVO. Note that video output is available one clock pulse before the corresponding digital output (one clock pipe-line delay for the analog to digital conversion).

Pixel Order

After a reset, pixel number one is located on the upper left corner, looking at the chip with bond pads to the right. For each column of 8 pixels, pixels 1-3-5-7 are output on odd data Do0-3 pins, pixels 2-4-6-8 are output on even data De0-3 pins. Most significant bit is bit #3, least significant is bit #0.

Figure 9. Pixel Order



Synchronization: The Dummy Column

A dummy column has been added to the sensor to act as a specific pattern to detect the first pixel. So, 280 true columns + 1 dummy column are read for each frame.

The 4 bytes of the dummy column contain a fixed pattern on the two first bytes, and temperature information on the last two bytes.

Dummy Byte	Odd	Even
Dummy Byte 1 DB1:	111X	0000
Dummy Byte 2 DB2:	111X	0000
Dummy Byte 3 DB3:	rrrr	nnnn
Dummy Byte 4 DB4:	tttt	pppp

Note: x represents 0 or 1

The sequence 111X0000 111X0000 appears on every frame (exactly every 1124 clock pulses), so it is an easy pattern to recognize for synchronization purposes.

Thermometer

The dummy bytes DB3 and DB4 contains some internal and temperature information.

The even nibble nnnn in DB3 can be used to measure an increase (or decrease) of the chip temperature, using the difference between two measures of the same physical device. The following table gives values in Kelvin.

nnnn Decimal	nnnn Binary	Temperature differential with code 8 in Kelvin
15	1111	11.2
14	1110	8.4
13	1101	7
12	1100	5.6
11	1011	4.2
10	1010	2.8
9	1001	1.4
8	1000	0
7	0111	-1.4
6	0110	-2.8
5	0101	-4.2
4	0100	-5.6
3	0011	-7
2	0010	-8.4
1	0001	-11.2
0	0000	< -16.8

For code 0 and 15, the absolute value is a minimum (saturation).

When the image contrast becomes low because of a low temperature difference between the finger and the sensor, it is recommended to use the temperature stabilization circuitry to increase the temperature of two codes (i.e. from 8 to 10), to get at least an increase >1.4 Kelvin of the sensor. This enables to recover enough contrast to get a proper fingeprint for recognition purpose.

Integration Time and Clock Jitter

The FCD4B14 is not very sensitive to clock jitter (clock variation). The most important requirement is a regular integration time that ensures the frame reading rate is also as regular as possible, in order to get consistent fingerprint slices.

If the integration time is not regular, contrast will vary from one frame to another.

Note that it is possible to introduce some waiting time between each set of 1124 clock pulses, but the overall time of one frame read must be regular. This waiting time is generally the time needed by the processor to perform some calculation over the frame (to detect the finger, for instance).

Figure 10. Read One Frame

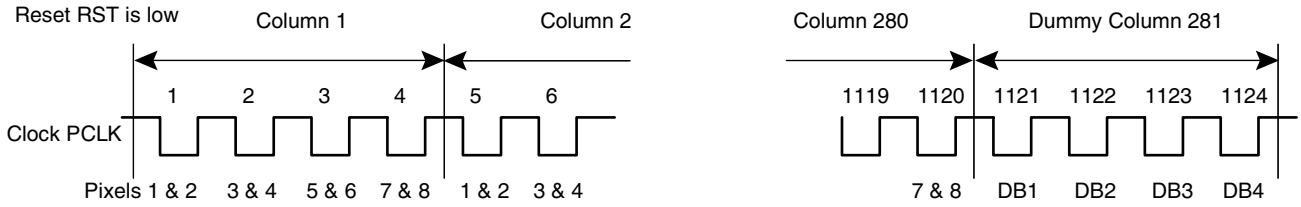
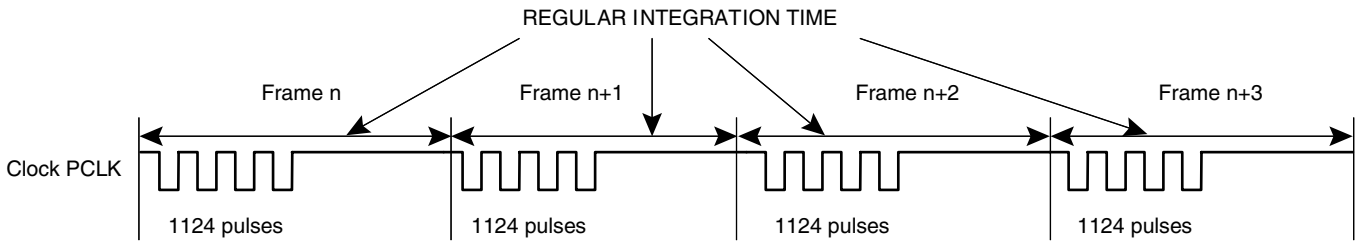


Figure 11. Regular Integration Time



Power Management

Nap Mode

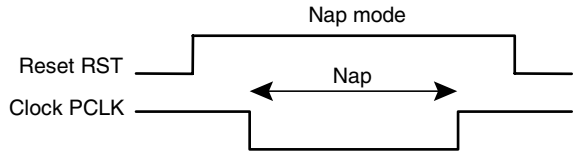
Several strategies are possible to reduce power consumption when not in use.

The simplest and most efficient is to cut the power supply, using external means.

A nap mode is also implemented in the FCD4B14. To activate this nap mode, user must:

1. Set the reset RST pin to high. Doing this, all analog sections of the device are internally powered down.
2. Set the clock PCLK pin to high (or low), thus stopping the entire digital section.
3. Set the TPE pin to low or disconnect TPP to stop the temperature stabilization feature.
4. Set Output Enable OE pin to high, so that output are forced in HiZ.

Figure 12. Nap Mode



In Nap Mode, all internal transistors are in shut mode. Only leakage current is drained in power supply, generally less than the tested value.

Static Current Consumption

When the clock is stopped (set to 1) and the reset is low (set to 0), the analog sections of the device drain some current and the digital section does not consume current if the outputs are connected to a standard CMOS input (= no current is drained in the I/O). In this case the typical current value is 5 mA. This current does not depend on the voltage (i.e. it is almost the same from 3V to 5.5V).

Dynamic Current Consumption

When the clock is running, the digital sections are consuming current, and particularly the outputs if they are heavily loaded. In any case, it should be less than the testing machine (120 pF load on each I/O), 50 pF maximum is recommended.

Connected to a USB interface chip (see application note 26 related to the FCDEMO4 kit) at 5V, and running at about 1 MHz, the FCD4B14 consumes less than 7 mA on VCC pin.

Temperature Stabilization Power Consumption (TPP pin)

When the TPE pin is set to 1, current is drained via the TPP pin. The current is limited by the internal equivalent resistance given in table 4 and a possible external resistor.

Most of the time, TPE is set to 0 and no current is drained in TPP. When the image contrast becomes low because of a low temperature differential (less than one Kelvin), then it is recommended to set TPE to 1 during a short time so that the dissipated power in the chip elevates the temperature, enabling to recover contrast. The necessary time to increase the chip temperature of one Kelvin depends on the dissipated power, the thermal capacity of the silicon sensor and the thermal resistance between the sensor and the surroundings.

As a rule of thumb, dissipating 300 mW in the chip elevates the temperature of 1 Kelvin in one second. With the 30 Ω typical value, 300 mW is 3V applied on TPP.

Packaging:
Mechanical Data

Figure 13. COB: Top View (all dimensions in mm)

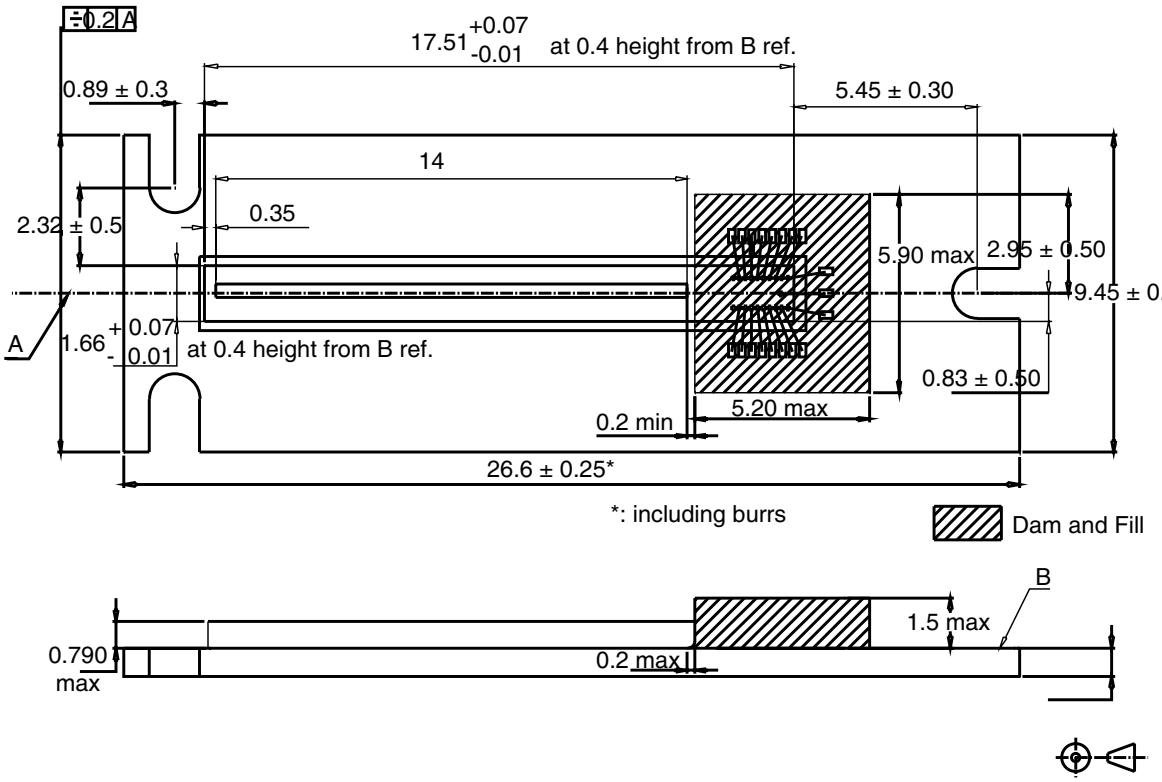


Figure 14. COB: Bottom View (all dimensions in mm)

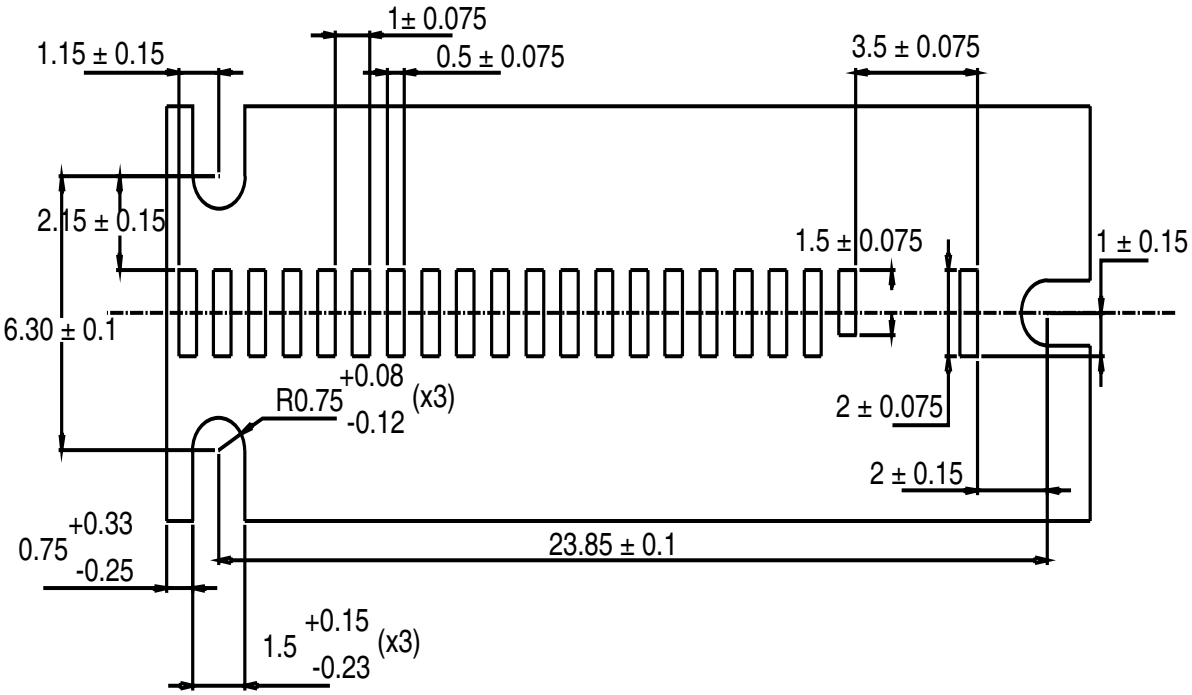
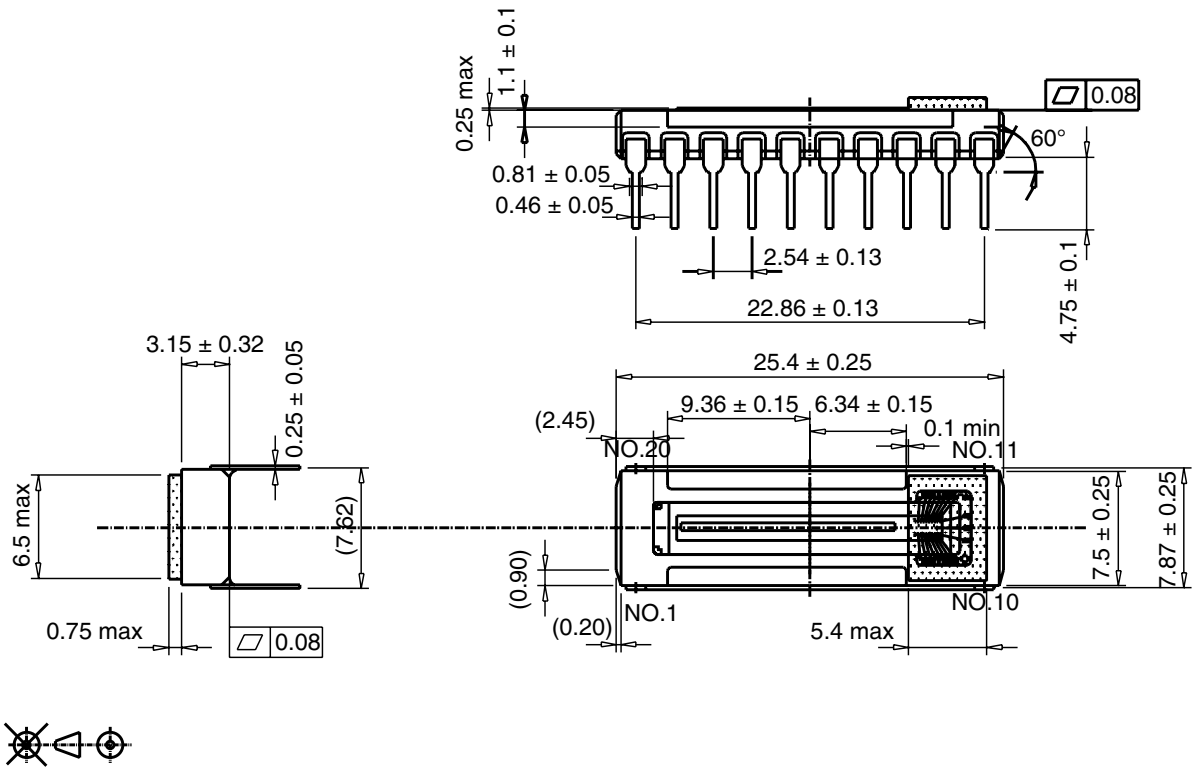
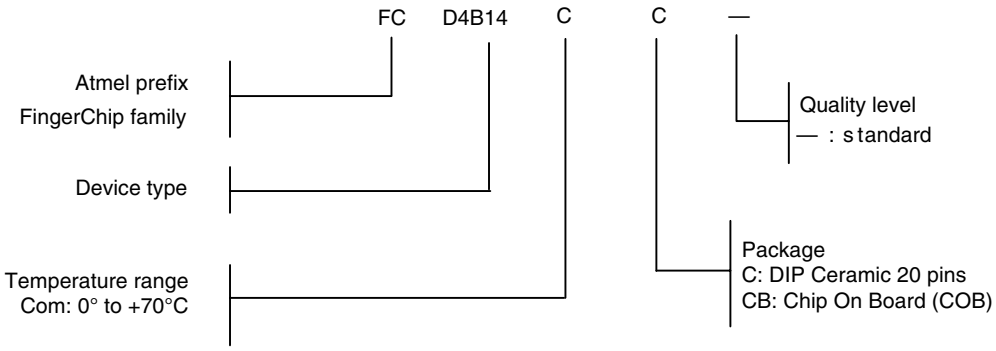


Figure 15. DIL Package (all dimensions in mm)



Ordering Information

Package Device



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