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DEI 1016
ARINC 429 Transceiver

Features

- Two Receivers and One Transmitter
- Harris/Holt/Raytheon Pin for Pin Replacement
- Wraparound Self-Test mode
- Word length of 25 or 32 bits
- Parity Status and generation of Receive and Transmit Words
- 8 Word Transmitter buffer
- Low Power CMOS processing
- Supports multiple ARINC data busses: 429, 571, 575, 706.

General Description:

The DEI 1016 provides an interface between a standard avionics type serial digital data bus and a 16-bit-wide digital data bus. The interface circuit consists of a single channel transmitter with an 8X32 bit buffer, two independent receive channels, and a host programmable control register to select operating options. The two receiver channels operate identically, each providing a direct electrical interface to an ARINC data bus.

The transmitter circuit contains an 8 word by 32 bit buffer memory and control logic which allows the host to write a block of data into the transmitter. The block of data is transmitted automatically by enabling the transmitter with no further attention by the host computer. Data is transmitted in TTL format on the D0(A)/D0(B) output pins. The signal format is compatible with DEI's extensive line of ARINC 429 Line drivers for easy connection to the ARINC data bus.
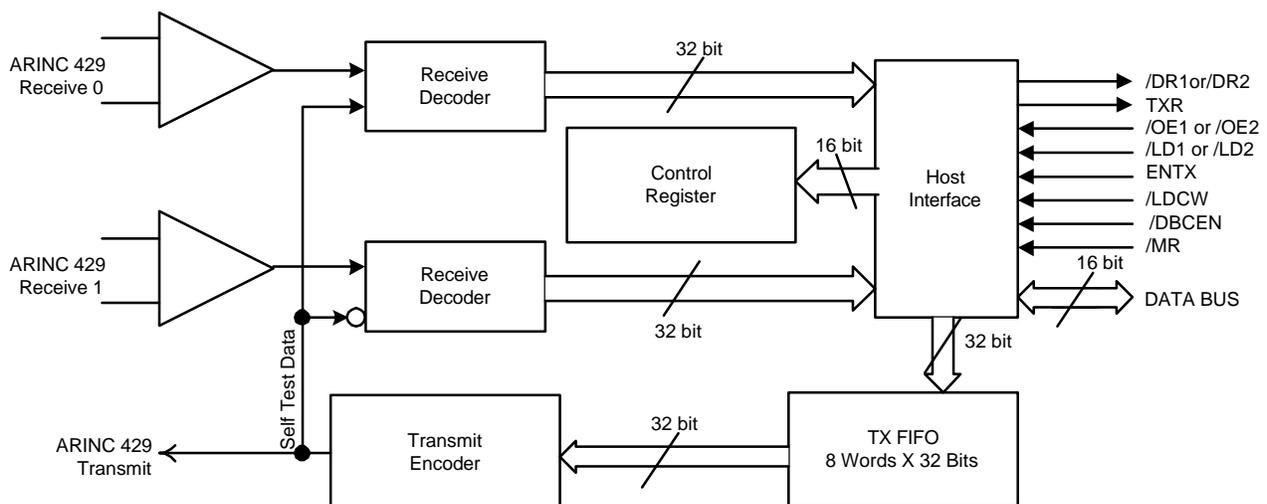
Figure 1: DEI1016 Block Diagram

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Table 1: DEI 1016 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	-0.5	+7.0	V
DC Input Voltage (except pins DI1(A,B) and DI2(A,B))	V_{IN}	-0.3	$V_{CC} + 0.3$	V
Voltage at pins DI1(A,B) and DI2(A,B)	V_{IN}	-29	+29	V
DC Output Current per pin		-25	+25	mA
DCV or GND current per pin		-50	+50	mA
Storage Temperature	T_{STG}	-65	+150	°C
Operating Temperature	T_O	-55	+125	°C
1MCK Clock Frequency			1.16	MHz

Table 2: DEI 1016 DC Electrical Characteristics

Unless noted, operating connections: V_{DD} = 5V ± 10%, T = -40ºC ~ +85ºC

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ARINC LINE INPUTS						
Logic 1 Input Voltage	V_{IH}	V_{DIFF} DI(A) and DI(B)	6.5	10	13	V
Logic 0 Input Voltage	V_{IL}	V_{DIFF} DI(A) and DI(B)	-6.5	-10	-13	V
Null Input Voltage	V_{NUL}	V_{DIFF} DI(A) and DI(B)	-2.5	0	+2.5	V
Common Mode Voltage	V_{CM}				±5	V
Differential Input Impedance	R_I		12			kΩ
Input Impedance to V_{DD}	R_H		12			kΩ
Input Impedance to GND	R_G		12			kΩ
Differential Input Capacitance	C_I				20	pF
Input Capacitance to V_{DD}	C_H				20	pF
Input Capacitance to GND	C_G				20	pF
ALL OTHER INPUTS (including bi-directional)						
Max low level Input Voltage	V_{IL}				0.8	V
Min high level Input Voltage	V_{IH}		2			V
Max Input Current	I_{IN}	V_{IN} = GND to V_{DD}			±10	μA
Input Capacitance	C_{IN}				15	pF
ALL OUTPUTS (including bi-directional)						
Min High level output voltage	V_{OH}	I_{OH} = 20μA (CMOS) I_{OH} = 6mA (TTL)	V_{DD} –0.1 2.7			V
Max Low level output voltage	V_{OL}	I_{OL} = 20μA (CMOS) I_{OL} = 6mA (TTL)			0.1 0.4	V
POWER SUPPLY INPUT						
Supply Current	I_{DD}	1MCK = 1MHz		5	10	mA
Supply Voltage	V_{DD}		4.5	5	5.5	VDC

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Table 3: DEI 1016 AC Electrical Characteristics						
		Data Rate 100kbps		Data Rate 12.5kbps		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS
1MCK Frequency	f_{1MCK}		1.01		1.01	MHz
1MCK Duty Cycle	CK_{DC}	40	60	40	60	%
1MCK Rise/Fall Time	T_{CRF}		10		10	ns
Master Reset Pulse Width	T_{MR}	200		200		ns
Transmitter Data Rate (1MCK = 1MHz)	T_{DR}	99	101	12.4	12.6	kbps
Receiver Data Rate (1MCK = 1MHz)	R_{DR}	95	105	9.0	14.5	kbps

Table 4: Pin Definitions	
SYMBOL	DEFINITION
V_{DD}	+5VDC ±10%; Power Supply
DI1(A)	Data In 1, HI (Input, ARINC 429 compatible) ARINC 429 "A" data input to receiver 1.
DI1(B)	Data In 1, LO (Input, ARINC 429 compatible) ARINC 429 "B" data input to receiver 1.
DI2(A)	Data In 2, HI (Input, ARINC 429 compatible) ARINC 429 "A" data input to receiver 2.
DI2(B)	Data In 2, LO (Input, ARINC 429 compatible) ARINC 429 "B" data input to receiver 2.
/DR1	Data Ready Receiver 1. (Output, active low) Logic "0" indicates valid data in receiver 1.
/DR2	Data Ready Receiver 2. (Output, active low) Logic "0" indicates valid data in receiver 2.
SEL	Receiver data select. Selects receiver word 1 or 2 to be read by the data bus.
/OE1	Receiver 1 data enable. (input, active Low). Logic "0" enables selected data from receiver 1 on to the data bus.
/OE2	Receiver 2 data enable. (input, active Low). Logic "0" enables selected data from receiver 2 on to the data bus.
D0-D15	16-bit Data Bus (bi-directional, tri-state) Bi-directional data bus for reading data from either receivers, or for writing data into the transmitter memory or control register.
/LD1	Load Transmitter word 1 (input, active Low) Logic "0" pulse loads word 1 into the transmitter memory from data bus.
/LD2	Load Transmitter word 2 (input, active Low) Logic "0" pulse loads word 2 into the transmitter memory from data bus.
TXR	Transmitter Ready (output, active High) Logic "1" indicates the transmitter memory is empty and ready to accept new data.
DO(A)	Transmitter Data, HI (output, active High, return to zero) Logic "1" indicates transmitter data bit is a 1. The signal returns to zero for second half of bit time.
DO(B)	Transmitter Data, LO (output, active High, return to zero) Logic "1" indicates transmitter data bit is a "0". The signal returns to zero for second half of bit time.
ENTX	Enable Transmitter (input, active High) Logic "1" enables transmitter to send data from transmitter memory. This must be logic "0" while writing data into transmitter memory. Transmitter memory is cleared by high-to-low transition.
/LDCW	Load Control Register (input, active Low) Logic "0" pulse loads control register from the data bus.
1MCK	External Clock (input, TTL compatible) Master clock used by both the receivers and transmitter. The 1MHz rate is a X10 clock for the HI data rate (100 kbps), and a X80 clock for LO data rate (12.5 kbps)
TXCK	Transmitter Clock (output) Delivers a clock frequency equal to the transmit data rate. The clock is always enabled and in phase with the data. The clock is a logic "1" during the first half of the data bit time.
/MR	Master Reset (input, active Low pulse) Logic "0" resets transmitter memory, bit counters, word counter, gap timers, /DRx, and TXR. Used on power up and system reset.
/DBCEN	Data Bit Control Enable (input, active low with internal pull up to V_{DD}) Logic "0" enables the transmitter parity bit control function as defined by control register bit 4 (PAREN). Logic "1" forces transmitter parity bit insertion regardless of PAREN value. Pin is normally left open or tied to ground.

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## Functional Description:

The DEI 1016 supports a number of various options which are selected by data written into the control register. Data is written into the control register from the 16-bit data bus when the /LDCW signal is pulsed to a logic "0". The twelve control bits control the following functions:

1) Word Length (32 or 25 bits)
2) Transmitter bit 32 (Parity or Data)
3) Wrap around self test.
4) Source Destination code checking of received data.
5) Transmitter parity (even or odd)
6) Transmitter and Receiver data rate (100 or 12.5 kbps)

Table 5: Control Register Format			
BIT	SYMBOL	BIT	SYMBOL
D15 (MSB)	WLSEL	D7	X1
D14	RCVSEL	D6	SDENB1
D13	TXSEL	D5	/SLFTST
D12	PARCK	D4	PAREN
D11	Y2	D3	NOT USED
D10	X2	D2	NOT USED
D9	SDENB2	D1	NOT USED
D8	Y1	D0	NOT USED

Table 6: DEI 1016 Control Word		
NAME	DATA BIT	DESCRIPTION
PAREN	D4	Transmitter Parity Enable. Enables parity bit insertion into transmitter data bit 32. Parity is always inserted if /DBCEN is open or HI. If /DBCEN is LO, Logic "0" on PAREN inserts data on bit 32, and Logic "1" on PAREN inserts parity on bit 32.
/SLFTST[1]	D5	Self Test Enable. Logic "0" enables a "wrap around" test mode which internally connects the transmitter outputs to both receiver inputs, bypassing the receiver front end. The test data is inverted before going into receiver 2 so that its data is the complement of that received by receiver 1. The transmitter output is active during test mode.
SDEN1[2]	D6	S/D Code Check Enable for receiver 1. Logic "1" enables the Source/Destination Decoder for receiver 1.
X1, Y1[2]	D7, D8	S/D compare code RX1. If the receiver 1 S/D code check is enabled (SDENB1=1), then incoming receiver data S/D fields will be compared to X1, Y1. If they match, the word will be accepted by receiver 1; if not, it will be ignored. X1 (D7) is compared to serial data bit 9, Y1 (D8) is compared to serial data bit 10.
SDEN2[2]	D9	S/D Code Check Enable for receiver 1. Logic "1" enables the Source/Destination Decoder for receiver 1.
X2, Y2[2]	D10, D11	S/D compare code RX2. If the receiver 2 S/D code check is enabled (SDENB2=1), then incoming receiver data S/D fields will be compared to X2, Y2. If they match, the word will be accepted by receiver 2; if not, it will be ignored. X2 (D10) is compared to serial data bit 9, Y2 (D11) is compared to serial data bit 10.
PARCK	D12	Parity Check Enable. Logic "1" inverts the transmitter parity bit for test of parity circuits. Logic "0" selects normal odd parity; logic "1" selects even parity.
TXSEL[3]	D13	Transmitter Data Rate Select. Logic "0" sets the transmitter to the HI data rate. HI rate is equal to the clock rate divided 10. Logic "1" sets the transmitter to the LO data rate. LO rate is equal to the clock rate divided by 80.
RCVSEL[4]	D14	Receiver Data Rate Select. Logic "0" sets both receivers to accept the HI data rate. The nominal HI data rate is the input clock divided by 10. Logic "1" sets both receivers to the LO data rate. The nominal LO data rate is the input clock divided by 80.
WLSEL[5]	D15	Word Length Select. Logic "0" sets the transmitter and receivers to a 32 bit word format. Logic "1" sets them to a 25 bit word format.
NOT USED	D0-D4	When writing to the control register, the four "not used bits" are "don't care" bits. These four bits will not be used on the chip.

NOTES:
1) The test mode should always conclude with ten null's. This step prevents both receivers from accepting invalid data.
2) SDENBn, Xn & Yn should be changed within 20 bit times after /DRn goes low and the bit stream has been read, or within 30 bit times after a master reset has been removed.
3) TXSEL should only be changed during the time that TXR is high or Master Reset is low.
4) RCVSEL should be changed only during a Master Reset pulse. If changed at any other time, then the next bit stream from both Receiver 1 and Receiver 2 should be ignored.
5) When the control word is written the effect of the WLSEL bit will take effect immediately on the first complete ARINC word received or transmitted following the control word write operation.

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Data Format:

The ARINC serial data is shuffled and formatted into two 16 bit words (WORD1 and WORD2) used by the bi-directional data bus interface. Figure 2 shows the mapping between the 32 bit ARINC serial data and the two data words. Figure 3 describes the mapping for the 25 bit serial word used when control register bit WLSEL is set to logic "1".
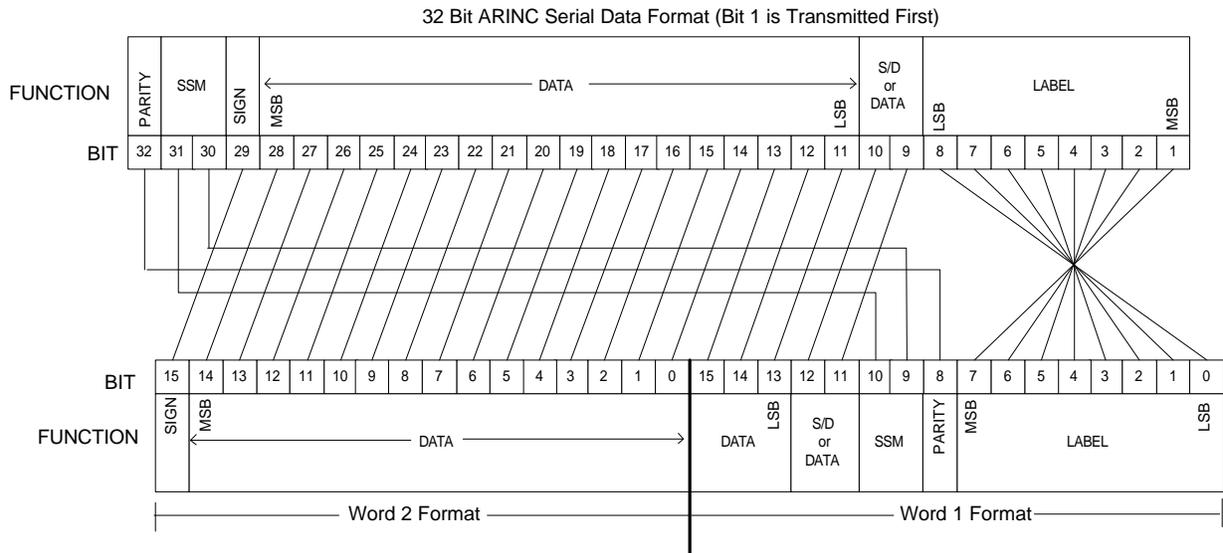
Figure 2: Mapping of Serial Data to/from Word 1 and Word 2 in 32 bit format.
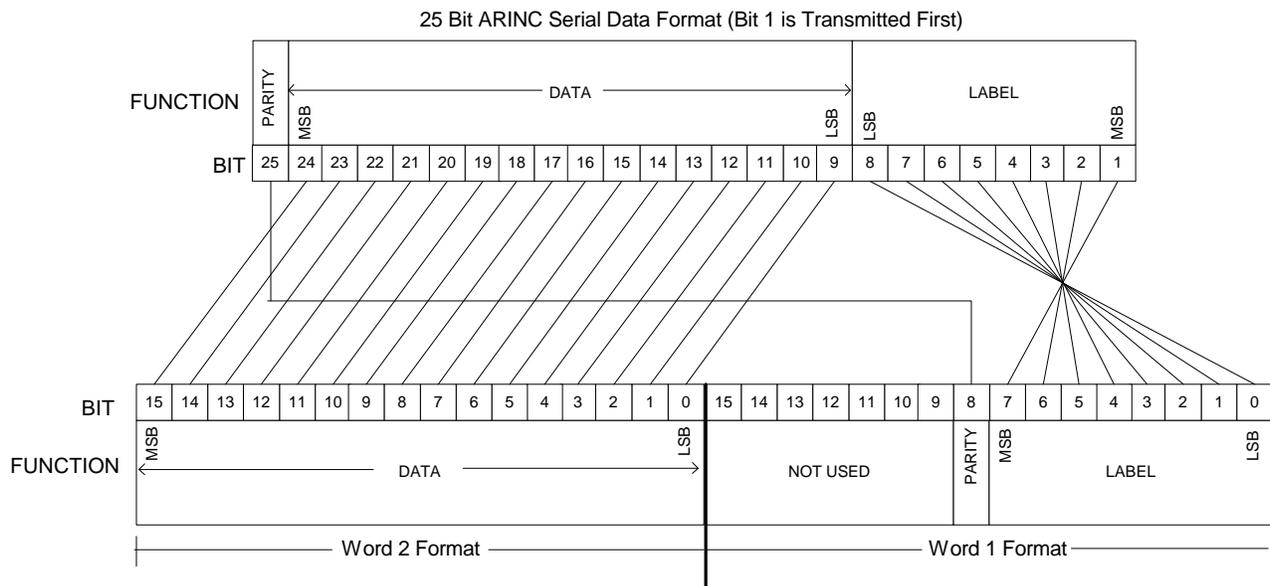
Figure 3: Mapping of Serial Data to/from Word 1 and Word 2 in 25 bit format.

Receiver Operation:

Since the receivers function identically, only one will be discussed in detail. The receiver consists of the following circuits.

Line Receiver

The front end of the Line Receiver functions as a voltage level translator. It transforms the ±10 volt differential ARINC data signals into 5 Volt internal logic levels. The line receivers are protected against shorts to ±29 Volts and provides common mode voltage rejection. The outputs of the Line Receiver are one of two inputs to the Self-Test Data Selector. The other input to the Data Selector is the self-test signal from the transmitter section. The self-test signals are inverted going into Receiver 2. The data selector is controled by Control Register bit D5 (SLFTST).
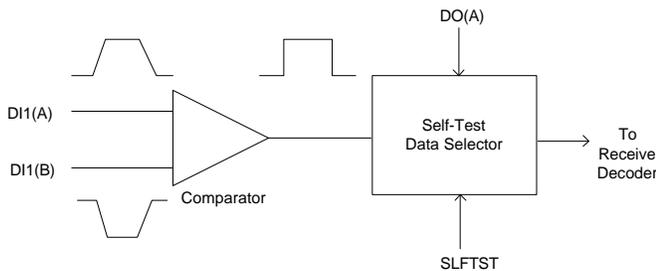

Figure 4: Line Receiver Block Diagram

Incoming Data

The incoming data (either self test or ARINC) is triple sampled by the word gap timer to generate a data clock. The start of each bit is first detected and then verified two receive-clock cycles later. The receive clock is 1MHz for HI speed and 125 KHz for LO speed operation and is generated by the Receiver/Transmitter timing circuit. The receive clock is ten times the normal data rate to ensure no data ambiguity.

Data Clock

The derived data clock then shifts the data down a 32 bit long Data Shift Register. The data word length is selectable for either 25 or 32 bits long by Control Register Bit WLSEL. As soon as the data word is completely received, an internal signal is generated by the word gap timer circuit to enable loading data into the 32 bit receive buffer latch.

S/D Decoder

The Source/Destination decoder compares the user set code (X and Y) with bits 9 and 10 of the data word. The decoder can be enabled and disabled by the SDENB bit of the Control Register. If the two codes are matched, a signal is generated to latch in the received data into the receiver buffer. Otherwise the data word is ignored and not latched into the receive buffer. If the data is latched, the data ready flag (/DRn) is set to indicate to the user that a valid data word is ready to be read.

Parity Control

The parity of the incoming message is checked when either word of the receiver is read. Logic "0" indicates

The received word has an odd number of 1's (no error). Logic "1" indicates the received word has an even number of 1's (error condition). If the data format has data in bit 32 instead of parity, the user software must calculate the value of the 32nd bit. If Word 1 and Word 2 together have an even number of 1's, then data bit 32 is a logic "1". Otherwise, it is a logic "0".

Data Access

To access the receiver data, the user sets the receiver data select input (SEL) to a logic "0" and pulses the output enable (/OEn) line with a logic "0". This causes Data Word 1 to be placed on the 16 bit data bus. To read Word 2, the user sets the data select input (SEL) to a logic "1" and pulses the output enable (/OEn) low to place Word 2 on the data bus. When both Word 1 and Word 2 have been read, DRn will be reset. This reset is triggered by the leading edge of the final /OEn pulse.

If a new data word is received before the previous data has been read from the receiver buffer (as indicated by the /DRn signal flip-flop), the receive buffer will not be over written by the new data. The new data will remain in the shift register until either the /DRn signal is reset and it can be written into the receive buffer or it is overwritten by the next incoming data word. Data in the shift register will be overwritten by new incoming data, while data that has been latched into the receive buffer can not be overwritten.

Data Error Conditions

If the receiver input data word string is broken before the entire data word is received, the receiver will reset and ignore the partially received data word.

If the receiver input data word string is not properly framed with at least 1 null bit before the word and 1 null bit after the word, the receiver will reset and ignore the improperly framed data word.

Transmitter Operation:

The transmitter section consists of an 8 word by 32 bit FIFO, parity generator, transmitter word gap timer, and a TTL output circuit.

FIFO Buffer

The 8x32 buffer memory allows the user to load up to 8 words into the transmitter, enable it, and then ignore it while the transmitter ships out the data without further attention. Data is loaded into the buffer by pulsing /LD1 to load the first 16 bits (WORD 1) from the data bus, and pulsing /LD2 to load WORD 2. /LD1 must always precede /LD2. The transmitter must always be disabled while loading the buffer (ENTX = logic "0").

If the buffer is full and new data is pulsed with /LD1 and /LD2, the last 32 bit word in the buffer will be overwritten. Data will remain in the buffer until ENTX is pulsed to a logic "1", which will activate the FIFO clock and data is shifted out serially to the transmitter driver.

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FIFO Buffer (continued)

The buffer data is transmitted until the last word in the buffer is shifted out. At this time a transmitter ready signal (TXR) is set to a logic "1" indicating that the buffer is empty and ready to receive up to eight more data words. Writing into the buffer memory is disabled when ENTX is set to logic "1".

Transmitter Ready Signal (TXR)

The transmitter ready flag (TXR) is set to logic "0" with the first occurrence of an /LD2 pulse to indicate that the buffer is not empty.

Output Register

The output register is designed such that it can shift out a word of 25 bits or 32 bits. The length is controlled by control register bit "WLSEL".

TX Word Gap Timer

The TX word gap timer circuit inserts a 4 bit time gap between words. This gives a minimum requirement of a 29 bit time or a 36 bit time for each word transmission. The 4 bit time gap is also automatically maintained when the next new block of data is loaded into the buffer, which may take less than one bit time.

Parity Generator

The parity generator calculates either odd or even parity as specified by control register bit "PARCK". Odd parity is normally used; even parity is available to test the receiver parity check circuit. Odd parity means that there is an odd number of 1's in the 25 or 32 bit serial word. Bit 8 of word one is replaced with a parity bit if parity is selected by the control register bit "PAREN" and the /DBCEN pin. Otherwise, bit 8 is passed through as data.

Transmitter Output

The transmitter driver outputs three TTL compatible signals: 1) DO(A), 2) DO(B), and 3) TXCLK. DO(A) and DO(B) are the transmitter data in two rail, return-to-zero format. DO(A) indicates a logic "1" data bit by going to a "1" for the 1st half of a bit time, then returning to "0" for the 2nd half; DO(B) remains at "0" for the whole bit time. In the same fashion, DO(B) indicates a logic "0" data bit by pulsing HI while DO(A) remains LO. A null bit is indicated when both signals remain LO. It is illegal for both signals to be logic "1". The TXCLK is a free running clock signal of 50% duty cycle and in phase with transmitter data. The clock will always be logic "1" during the first half of a bit time.

Power-Up Reset

An internall power-up reset circuit prevents erroneous data transmission before an external master reset has been applied.

25-bit Word Operation:

The TRANSCEIVER implements a 25 bit word format which may be used in non-ARINC applications to enhance data transfer rate. The format is a simplified version of the 32 bit ARINC word and is described in Figure 3. It consists of an 8 bit label, a 16 bit data word, and a parity bit. The parity bit can optionally be replaced with a 17th data bit.

The Source/Destination code checking option can be enabled in either receiver. It will operate on bits 9 and 10 of the 25 bit word.

Self-Test Operation:

By selecting the control register bit (/SLFTST) self test option, the user may perform a functional test of the TRANSCEIVER and support circuitry. The user can write data into the transmitter and it will be internally wrapped around into both receivers. The user can then verify reception and integrity of the data. The receiver line interface and the user's line drivers will not be tested.

By setting the transmitter to use even parity, the user can test the receiver's parity circuit operation.

Power-up reset and Master Reset:

The user must apply an active Lo pulse to the Master Reset pin (/MR) after power up or upon system reset. Preceding the master reset at power-up an internal power-up reset occurs which will clear the transmitter such that no erroneous serial data stream will be transmitted before master reset. Receivers, control register, and internal control logic are reset by master reset.

After resetting the device, the user must program the control register before beginning normal operation. The control register may be reprogrammed without additional reset pulses.

Processor Interface:

Figure 7 shows a typical reset and initialization sequence. The user must pulse the /MR pin low to reset the device. To load the Control Register from the data bus, the /LDCW pin is pulsed low while the desired control data is applied on the data bus.

Figure 5 shows a typical transmitter loading sequence. It begins with the transmitter completing transmission of the previous data block. The TXR flag goes HI to notify the user that data may be loaded into the buffer. The user sets ENTX to LO to disable the Transmitter and proceeds to load a total of six ARINC words into the buffer. (Note that up to eight words could have been loaded). The user then enables the transmitter by setting ENTX to a logic "1" and the transmitter begins it's sequence of sending out data words. Although not shown in the figure, the transmitter loading sequence can be interrupted by receiver reading cycle with no interference between the two operations.

Figure 6 shows a typical receiver reading sequence. Both receivers notify the user of valid data ready by setting their respective /DRn lines to logic "0". The user responds by first reading the two data words from Receiver 1 and then from Receiver 2. The SEL line is normally a system address line and may assume any state, but must be valid when the /OEn line is pulsed low.

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Transmitter Ready (TXR)

Enable Transmitter (ENTX)

Load Word 1 (/LD1)

Load Word 2 (/LD2)

Data Bus (D0 - D15)

(W1) (W2) (W1) (W2) (W1) (W2) (W1) (W2) (W1) (W2) (W1) (W2)

Transmitter Data (DO(A)/DO(B))

Word 8

Word 1

TX Starts First Word
User Enables TX
User Loads 6th Word
User Loads 5th Word
User Loads 4th Word
User Loads 3rd Word
User Loads 2nd Word
TXR low indicates TX not Empty
User Loads 1st Word
User Disables TX
TXR HIGH indicates TX is empty and user may load data
TXR transmitts last word from buffer

Figure 5: Typical Transmitter Load Sequence

Data Ready 1 (/DR1)

Data Ready 2 (/DR2)

Data Enable 1 (/OE1)

Data Enable 2 (/OE2)

Receiver Select (SEL)

XXXXXXXXXXXXXXXX XXX XXXXXXX XXX XXXXXXXXXXXXXXXXXXXXXX

Data Bus (out) (D0 - D15)

Word 1 Word 2 Word 1 Word 2

$\overline{DR2}$ HIGH indicates RX2 is empty
User Reads Word 1 and Word 2 from RX2
$\overline{DR1}$ HIGH indicates RX1 is Empty
User reads Word 1 and Word 2 from RX1
$\overline{DR2}$ LOW indicates reception of valid data from RX2
$\overline{DR1}$ LOW indicates RX1 is empty

Figure 6: Typical Receiver Read Sequence

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$\overline{\text{MR}}$

t_{MR}

t_{PWLD}

$\overline{\text{LDCW}}$

D0 - D15

Valid Data
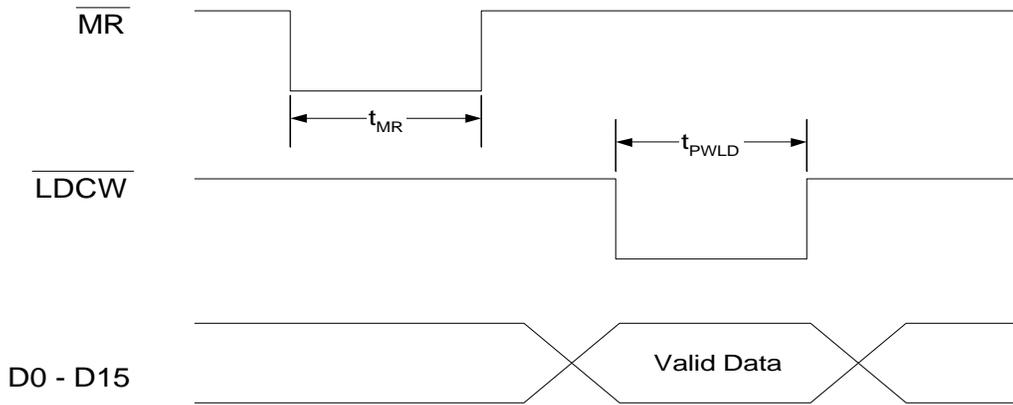
Figure 7: Reset and Initialization Sequence

ARINC DATA

BIT 31

BIT 32

t_{DDRN}

Data Ready Flag
(DR1 or DR2)

Data Word Select
(SEL)

Don't Care

Don't Care

Don't Care

Data Enable
(OE1 or OE2)

t_{SSEL}

t_{HSEL}

t_{DDROE}

t_{PWOE}

t_{OEOE}

t_{DOEDR}

Data Bus
(D0 - D15)

Word 1 Valid

Word 2 Valid

t_{DDR}

t_{DTS}
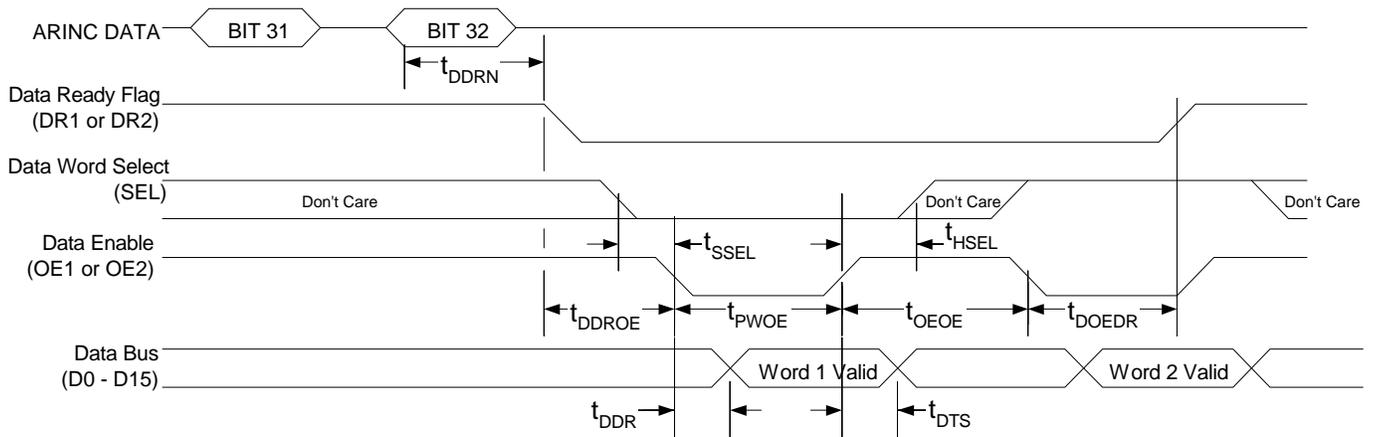
Figure 8: Receiver Read Operation and Timing

Load Word 1
(/LD1)

t_{PWLD}

t_{LL}

Load Word 2
(/LD2)

t_{SDW}

t_{HDW}

Data Bus
(D0 - D15)

Word 1 Valid

Word 2 Valid

Transmitter Ready
(TXR)

t_{DTXR}
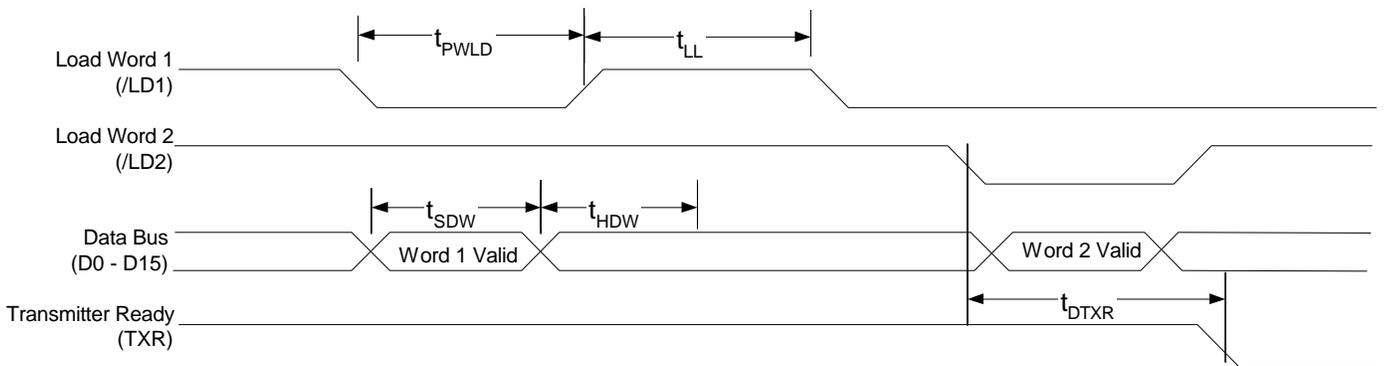
Figure 9: Transmitter Write Operation and Timing
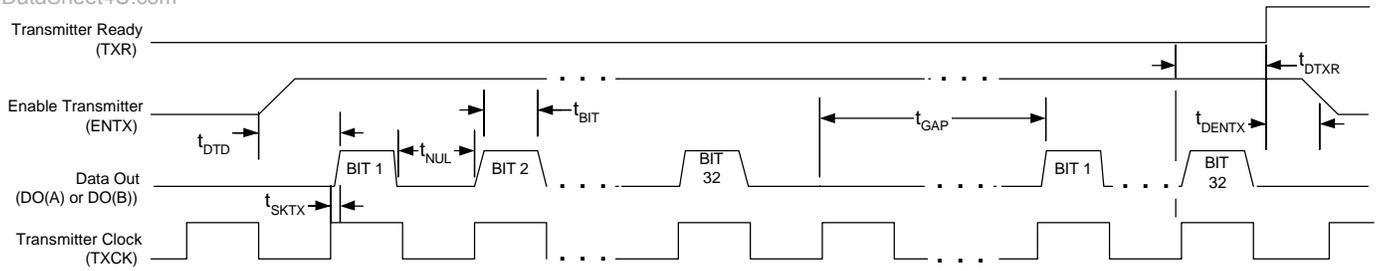
Figure 10: Transmitter Timing Diagram

Table 7: DEI 1016 AC Timing Characteristics						
		Data Rate 100kbps		Data Rate 12.5kbps		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS
WRITE CYCLE TIMING						
/LD1, /LD2 and /LDCW Pulse Width	t_{PWLD}	130			130	ns
Delay between consecutive Load Pulses	t_{LL}	0		0		ns
Data to /LD⇑ Set-Up Time	t_{SDW}	110		110		ns
Data to /LD⇑ Hold Time	t_{HDW}	0		0		ns
Delay /LD2⇑ to TXR⇓	t_{DTXR}		840		840	ns
READ CYCLE TIMING						
Delay, Bit 32/25 in to /DR⇓	t_{DDRN}		16		128	μs
Delay, /DRn⇓ to /OEn⇓	t_{DDROE}	0		0		ns
/OE1 or /OE2 Pulse Width	t_{PWOE}	200		200		ns
Delay between consecutive /OE pulses	t_{OEOE}	50		50		ns
Delay, 2nd /OE⇑ to /DRn⇑	t_{DOEDR}	200			200	ns
SEL to /OE⇓ to valid data	t_{SSEL}	20		20		ns
SEL to /OE⇑ hold time	t_{HSEL}	20		20		ns
Delay /OE⇓ to valid data	t_{DDR}		200		200	ns
SEL to /OE⇑ to data HI-Z	t_{DTS}	10	50	10	50	ns
TRANSMITTER TIMING						
Delay, ENTX⇑ to output data[1]	t_{DTD}		25		200	μs
Output Data null time	t_{NUL}	4.95	5.05	39.6	40.4	μs
Output data bit time	t_{BIT}	4.95	5.05	39.6	40.4	μs
Data skew between TXCK⇑ (⇓) and DO⇑ (⇓)	t_{SKTX}	0	±50	0	±50	ns
Data word gap time	t_{GAP}	39.6	40.4	316.8	323.2	μs
Delay, end of TX Word to TXR⇑	t_{DTXR}		50		50	ns
Delay, TXR⇑ to ENTX⇓	t_{DENTX}	0		0		ns

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Serial Interface:

The DEI1016 consits of two receive channels and one transmit channel. Each receive channel operates independently of each other and the transmitter. The receive data is asynchronous to the transmitter data and can also be at a different data rate than the transmitter.

Transmitter

The transmitter clock is free running and in phase with the transmitter data. The transmitter data (DO(A) and DO(B)) are TTL level signals. There are always at least 4 null bits between data words. An external ARINC line driver is required to interface the transmitter to the ARINC serial data bus. See ARINC 429 LINE DRIVERS below.

Receiver

The receiver signals (DI(A) and DI(B)) are differential, bipolar, return-to-zero logic signals. The ARINC channels can be connected directly to the receiver with no external components.

ARINC 429 Line Driver

Device Engineering offers a complete line of ARINC line drivers that support the ARINC 429, 571, and 575 standards. Please visit our website at http://www.deiaz.com to view and download data sheets for our line drivers.
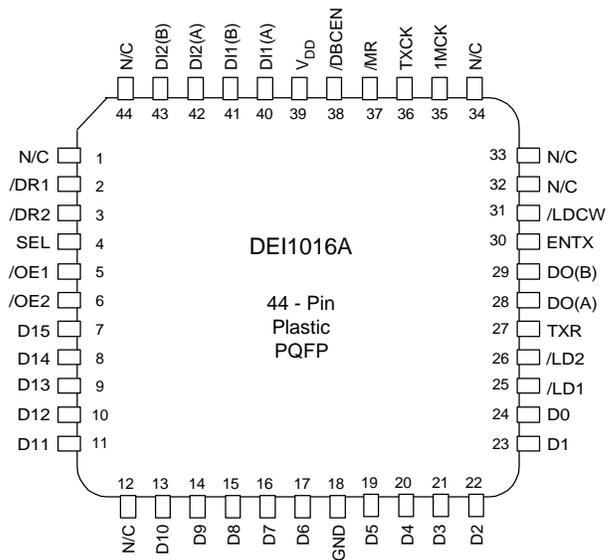
Figure 12: DEI1016A Pin-Out
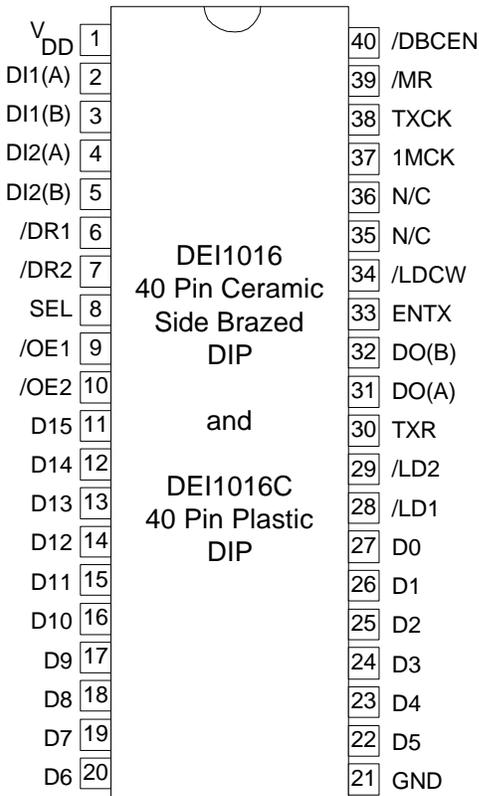
Figure 11: DEI1016 and DEI1016C Pin-Out
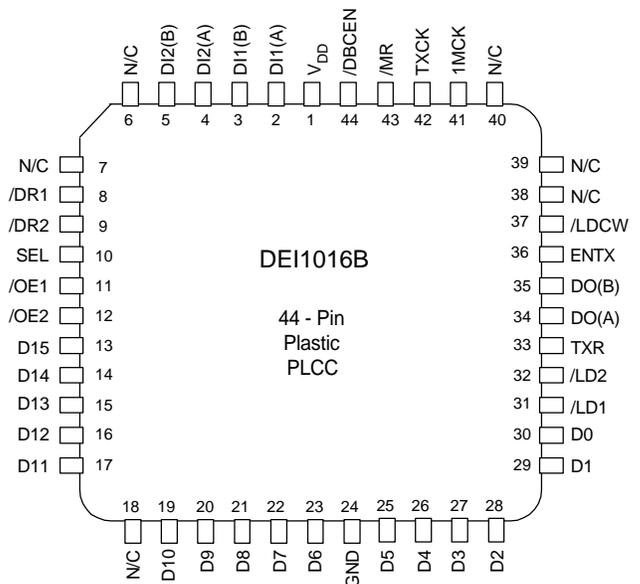
Figure 13: DEI1016B Pin-Out

.575 - .605

.590 - .615

0.008 - .012

Aluminum Bond Wire

DIE

Kovar Lid AuSn Solder Seal

Plated Kovar or Alloy 42 Lead

CuAg Braze

Tungsten Metallization

Lead 1 ID

2.060 MAX

.005 MIN

0.040 - 0.065

0.005 MIN

0.125 - .200

0.180 MAX

0.100 TYP

0.015 - .020
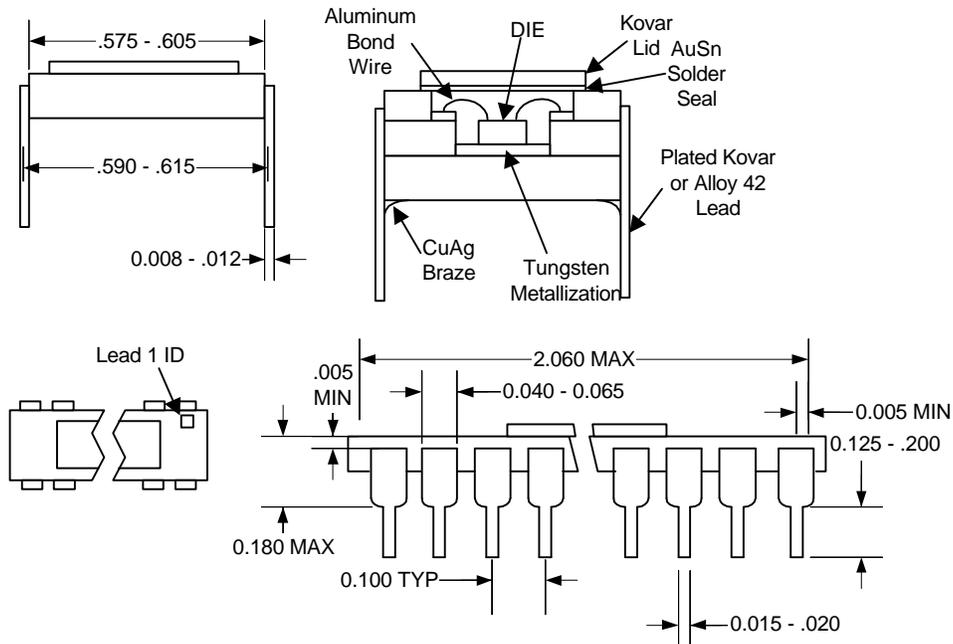
Figure 14: DEI1016 40 Pin Ceramic Side Braze DIP Package Dimensions
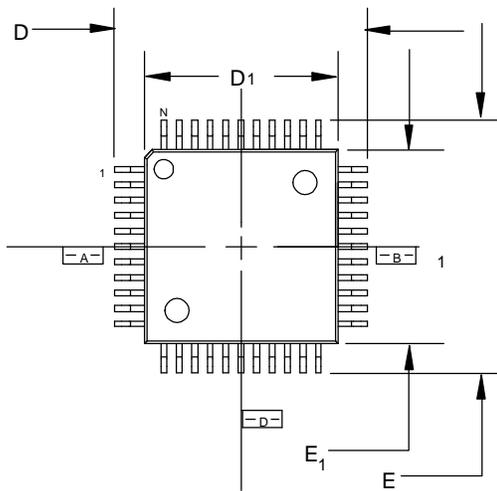
NOTES

1. ALL DIMENSIONS IN MILLIMETERS
2. DIMENSIONS SHOWN IN CHART ARE NOMINAL WITH TOLERANCES AS INDICATED
3. FOOT LENGTH "L" IS MEASURED AT GAGE PLANE AT 0.25 ABOVE THE SEATING PLANE.

FOOTPRINT (BODY +)		3.90 mm
DIMS.	TOLS.　LEADS	44L
A	MAX.	2.45
A$_1$	MIN./MAX.	.25/.50
A$_2$	+.10/-.05	2.00
D	P.25	13.90
D$_1$	P.10	10.00
E	P.25	13.90
E$_1$	P.10	10.00
L	+.15/-.10	.88
e	BASIC	.80
b	P.05	.30
Θ		0D-7D
ddd		.12 NOM.
ccc	MAX.	.10

D
D$_1$
N
1
- A -
- B -
1
- D -
E$_1$
E

10D TYP.
A$_2$
A
A$_1$
e
10D TYP.

0.30 RAD. TYP.
0.20 RAD. TYP.

6DP4°
STANDOFF
A$_1$
A
.25
SEATING PLANE
- C -
0.17 MAX.
Θ
b
L
ddd C A-B D
LEAD COPLANARITY
ccc C
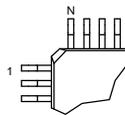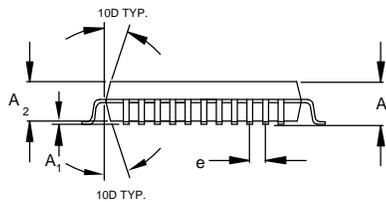
N
1
ANOTHER VARIATION OF PIN 1 VISUAL AID
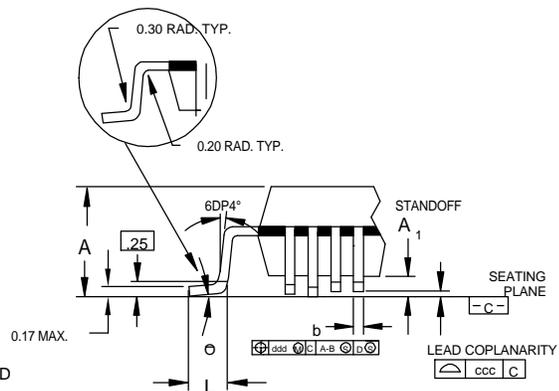
Figure 15: DEI1016A 44 Lead 3.90mm PQFP Package Dimensions

NOTES : 1. ALL DIMENSIONS IN INCH.
2. SURFACE FINISH : MATTE, CHARMILLE # 24-27
3. LEAD COPLANARITY AFTER FORM TO BE WITHIN .004

0.690

0.654

.029 +/- .003

.045 X 45 DEG
CHAMFER
FOR SQUARE PKG.

.017 +/- .004

PIN 1 IDENT.
.070 DIA X .025 DP.

0.690 0.654

.045 X 45 DEG
CORNER CHAMFER

.050 P .002

0.023/0.029 X 30D

30D
7D

7 +/-2 DEG

7D

PKG. CHAMFER FOR RECTANGULAR PKG.

0.152
0.010

.006 MIN
.035 R
TYP

7 +/-2 DEG

.020 MIN
.015 REF

.010 MIN

.030 P.005

ANOTHER VARIATION OF CASTELLATION

Figure 16: DEI1016B 44 Lead PLCC Package Dimensions

2.050 +/-.005

Pin 1

Dimensions Are in Inches(mm)

0.03 RAD

.550 +/-.005

0.020 MIN

.610 +/-.010

.220 MAX

.060

0 - 10 deg

0.100 TYP

0.150 +/-.005

0.018

.640 +/-.020

0.125
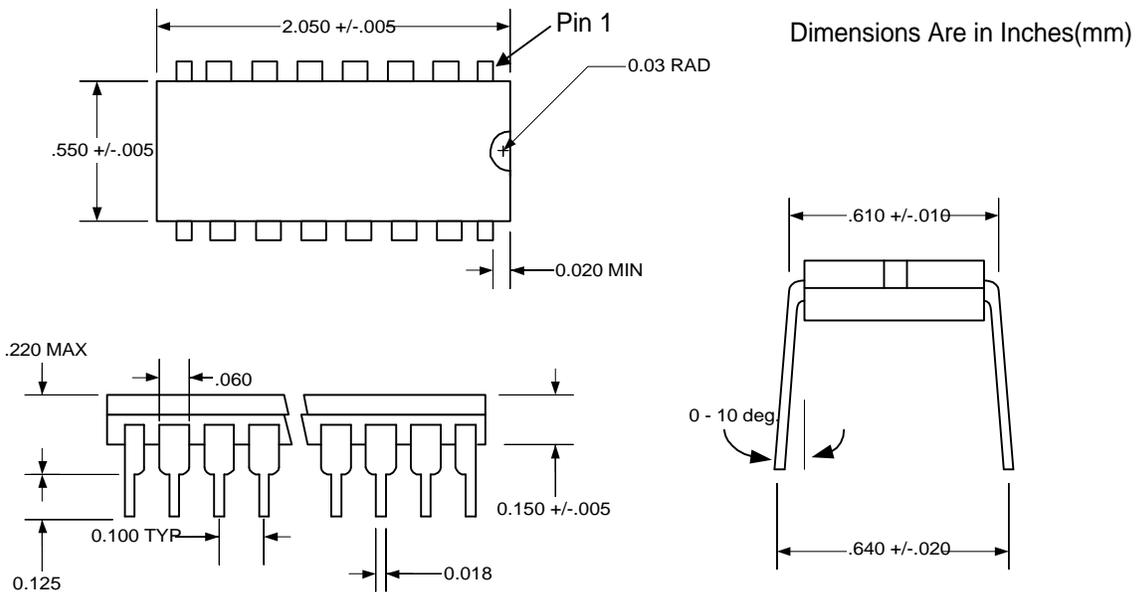
Figure 17: DEI1016C 40 Pin Plastic DIP Package Dimensions

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