TFT LCD Tentative Specification

MODEL NO.: V370H1 - L01

LCD TV Head Division	
AVP	

QRA Dept.	TVHD/PDD		
	DDIII	DDII	DDI
Approval	Approval	Approval	Approval

LCD TV Marketing and Project Management Dept.	
Project Manager	

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 0.0	Apr.21,'04	All	All	Tentative Specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V370H1- L01 is a 37" TFT Liquid Crystal Display module with 20-CCFL Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 HDTV format and can display true 16.7M colors (8-bit/color). The inverter module for backlight is optionally build-in.

1.2 FEATURES

-Ultra wide viewing angle – Super MVA technology

-High brightness (550 nits)

- High contrast ratio (>600:1)

- Fast response time

- High color saturation NTSC 75%

- HDTV (1920 x 1080 pixels) resolution, true HDTV format .

- DE (Data Enable) only mode

- LVDS (Low Voltage Differential Signaling) interface

1.3 APPLICATION

- TFT LCD TVs

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	820.8(H) x 461.7 (V) (37.07" diagonal)	mm	(1)
Bezel Opening Area	828.8 (H) x 470.9 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch	0.1425 (H) x 0.4275 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Hard coating (2H), Anti-reflective coating < less 2% reflection	-	-

1.5 MECHANICAL SPECIFICATIONS

Item			Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)		884.1	884.8	885.5	mm	
	Vertical(V)		525.4	525.9	526.4	mm	
	Depth(D)	W/PCB-Cover	-	43.54	-	mm	
		W/I INV	-	52.24	-	mm	
Weight			8950	9150	9350	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	(100)	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	(1.0)	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

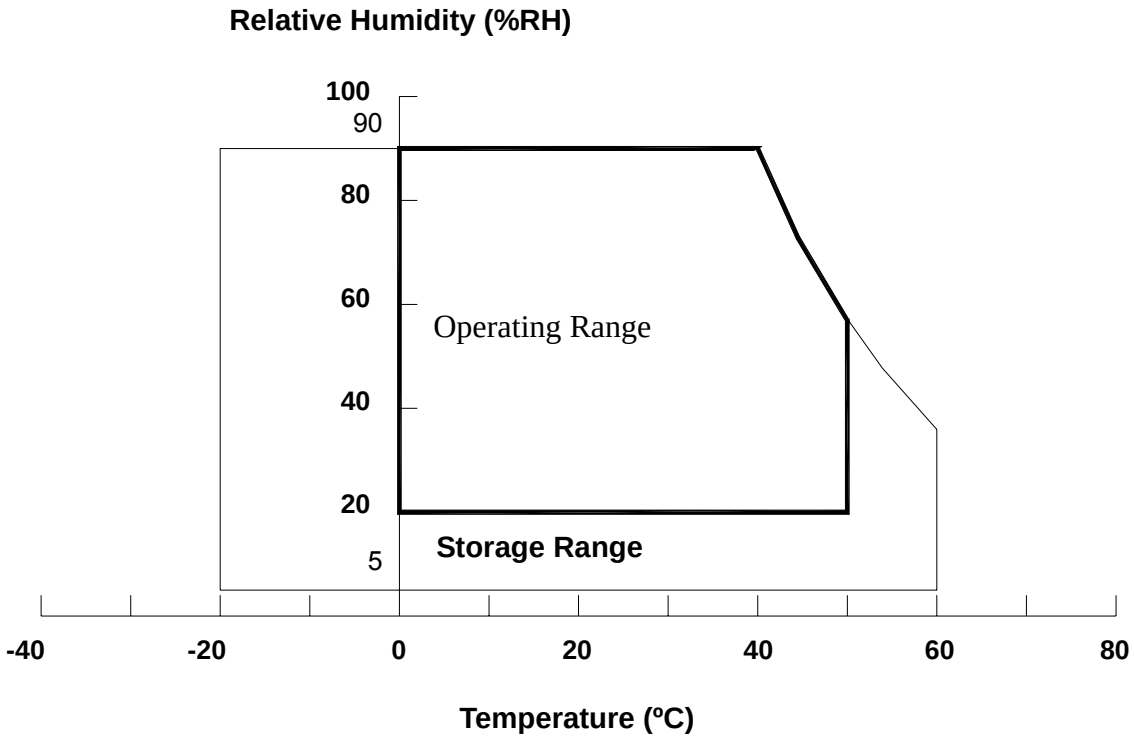
(c) No condensation.

Note (2) The temperature of panel display area surface should be 0 ºC Min. and 60 ºC Max.

Note (3) 2 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	20	V	(1)
Logic Input Voltage	V_{IN}	-0.3	4	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Lamp Voltage	V_W	Ta = 25 °C	—	—	3000	V_{RMS}	
Input Voltage	V_{BL}	—	—	120	(132)	V	(1), (2), I_L = 5.5 mA
Control Signal Level	—	—	-0.3	—	7	V	(1), (2), (4)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp and inverter (Refer to 3.2 for further information).

Note (3) Protect inverters from moisture condensation and freezing.

Note (4) The control signal level is including On/Off Control Voltage, Internal PWM Control Voltage, External PWM Control Voltage and Internal/External PWM Selection Voltage.

3. ELECTRICAL CHARACTERISTICS

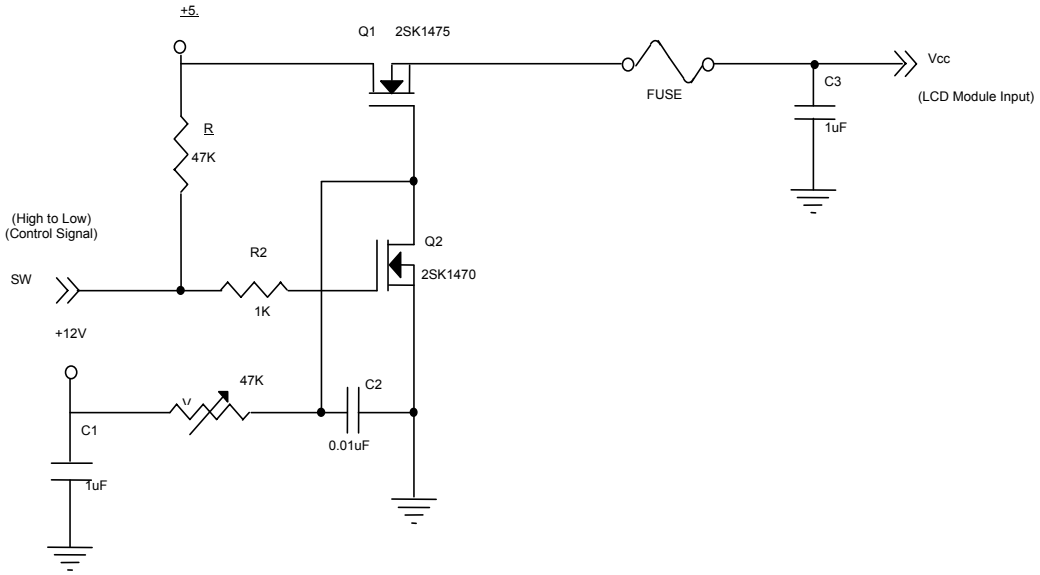
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

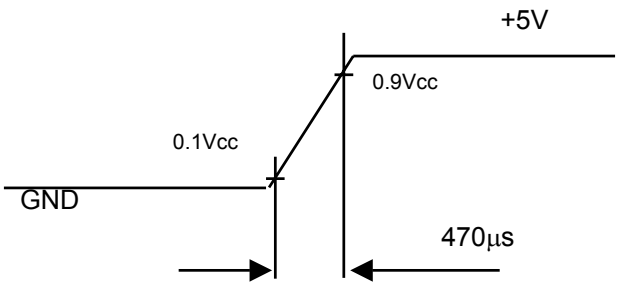
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	16.2	18	19.8	V	-
Ripple Voltage		V_{RP}	-		200	mV	-
Rush Current		I_{RUSH}	-	4	4.5	A	(2)
Power Supply Current	White	Icc	-	0.75	TBD	A	(3)a
	Black		-	0.41	TBD	A	(3)b
	Vertical Stripe		-	TBD	TBD	A	(3)c
LVDS differential input high threshold voltage		V_{TH}	-	-	+100	mV	
LVDS differential input low threshold voltage		V_{TL}	-100	-	-	mV	
LVDS common input voltage		Vic	1.125	1.25	1.375	V	
Terminating Resistor		RT	-	100	-	ohm	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470μs



Note (3) The specified power supply current is under the conditions at Vcc = 5 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

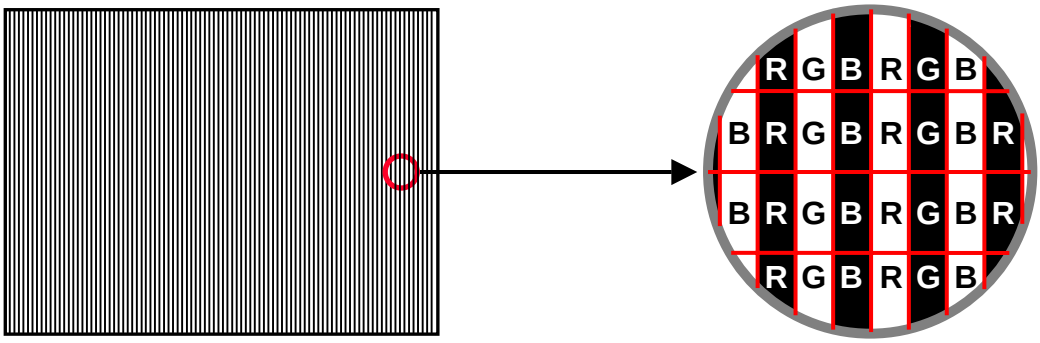
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



Active Area

3.2 BACKLIGHT UNIT

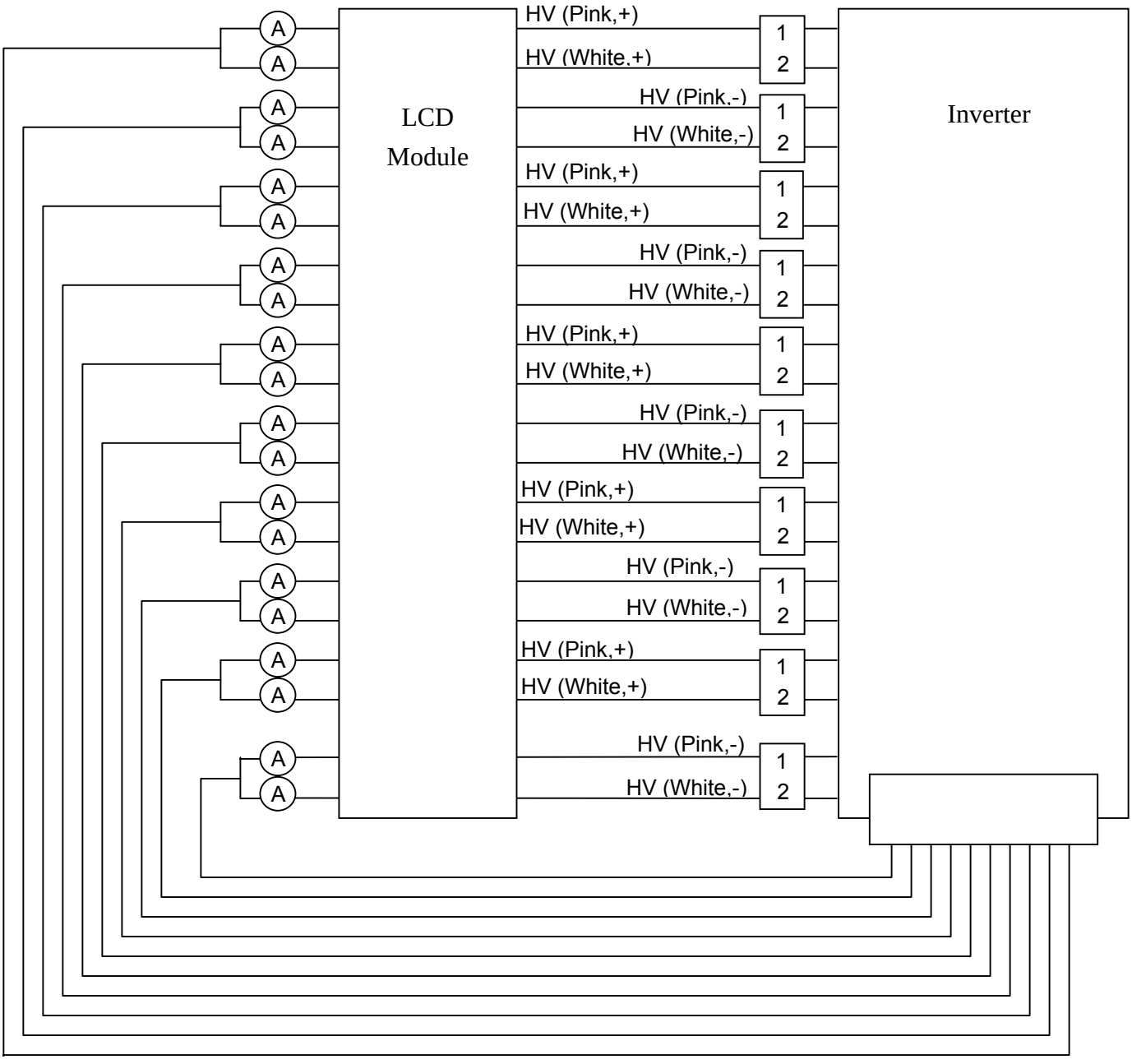
3.2.1 CCFL CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	1113	1237	1361	V_{RMS}	I_L = (5.5) mA
Lamp Current	I_L	5.2	5.5	5.8	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	2460	-	3000	V_{RMS}	(2), Ta = 25 ºC
		2800	-	3000	V_{RMS}	(2), Ta = 0 ºC
Operating Frequency	F_L	40	55	70	KHz	(3)
Lamp Life Time	L_{BL}	50K	-	-	Hrs	(5)

3.2.2 INVERTER CHARACTERISTICS

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P_{BL}	-	170	-	W	(5), I_L = 5.5mA
Input Voltage	V_{BL}	108	120	132	V_{DC}	
Input Current	I_{BL}	-	1.4	-	A	Non Dimming
Input Ripple Noise	-	-	-	2.5	V_{P-P}	VBL=108V
Backlight Starting Voltage	V_{BS}	2750	-	3000	V_{RMS}	Ta = 0 ºC
		2410	-	3000	V_{RMS}	Ta = 25 ºC
Oscillating Frequency	F_W	51	54	57	kHz	
Dimming frequency	F_B	150	160	170	Hz	
Minimum Duty Ratio	D_{MIN}	-	20	-	%	

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:



Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined by the brightness is larger than 50% or the effective discharge length is shorter than 80% of its original value (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point.) as the time in which it continues to operate under the condition Ta = 25 ±2℃ and I_L = 5.2 ~ 5.8 mArms.

Note (5) The power source capacity should be higher than inverter total power consumption P_{BL} and the transient response of power supply when inverter operate at dimming function also should be considered under design.

3.2.3 INVERTER INTERTFACE CHARACTERISTICS

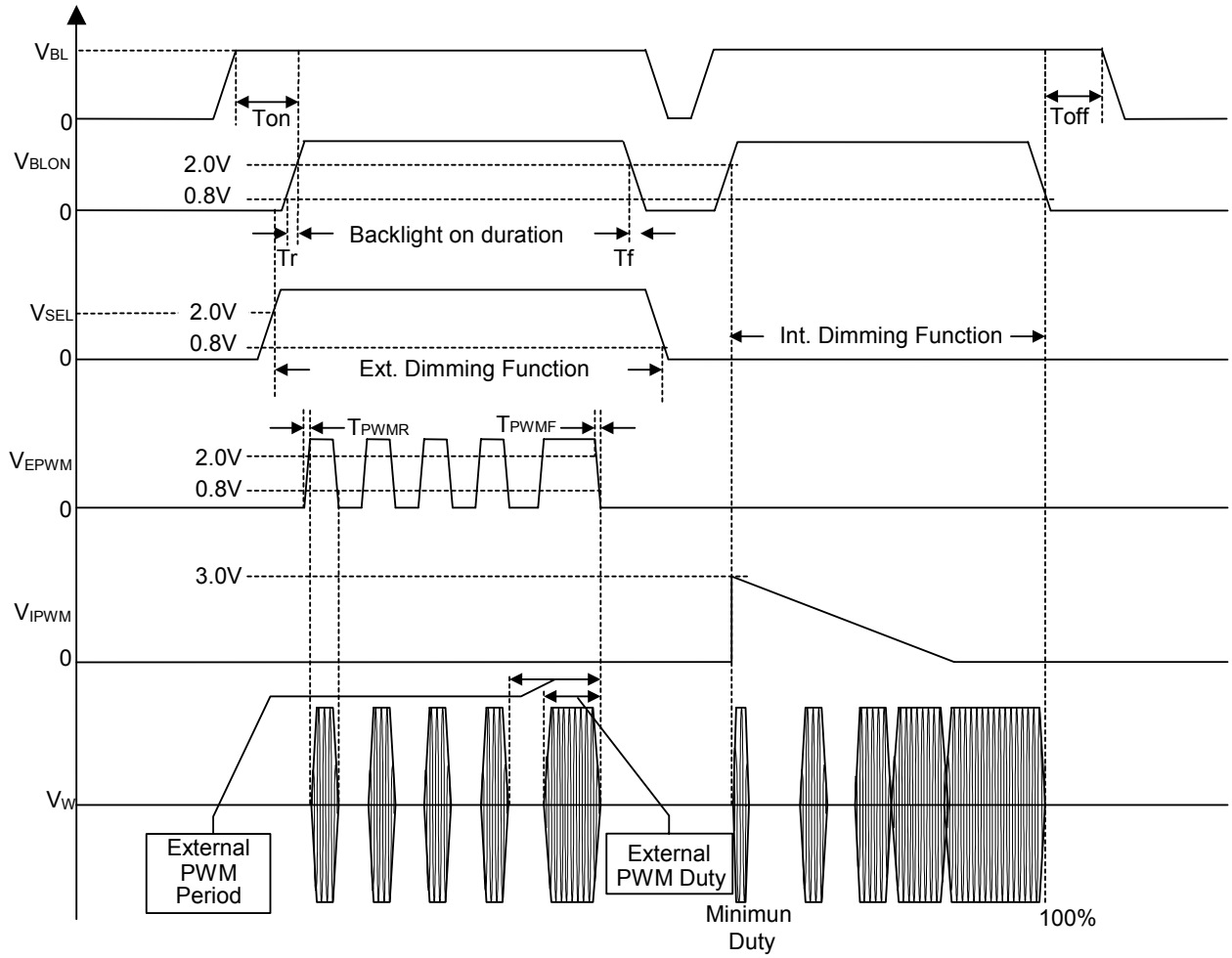
ITEM		SYMBOL	TEST CONDITION	MIN	TYPE	MAX	UNIT	NOTE(1-2)
On/Off Control Voltage	ON	V_{BLON}	—	2.0	—	5.0	V	See as below
	OFF		—	0	—	0.8	V	
Internal/External PWM Select Voltage	HI	V_{SEL}	—	2.0	—	5.0	V	Ext. Dim. Control
	LO		—	0	—	0.8	V	Int. Dim. Control
Internal PWM Control Voltage	MAX	V_{IPWM}	V_{SEL} = L	—	—	3.0	V	Minimum Duty Ratio
	MIN		V_{SEL} = L	—	0	—	V	Maximum Duty Ratio
External PWM Control Voltage	HI	V_{EPWM}	V_{SEL} = H	2.0	—	5.0	V	ON Duration
	LO		V_{SEL} = H	0	—	0.8	V	OFF Duration
Control Signal Rising Time		Tr	—	—	—	100	ms	See as below
Control Signal Falling Time		Tf	—	—	—	100	ms	
PWM Signal Rising Time		T_{PWMR}	—	—	—	50	us	
PWM Signal Falling Time		T_{PWMF}	—	—	—	50	us	
Input impedance		R_{IN}	—	1	—	—	MΩ	
BLON Delay Time		T_{on}	—	300	—	500	mS	(3)
BLON Off Time		T_{OFF}	—	300	—	500	mS	

Note (1) External PWM control signal (E_PWM) should be connected to low in case internal PWM was selected. (SEL = low). Internal PWM control signal (I_PWM) should be connected to ground in case external PWM was selected. (SEL = high) and the, floating of any control signal is not allowed. Besides, The SEL pin should be a definite level before the BLON signal.

Note (2) For dimming control function operation chart was shown as below.

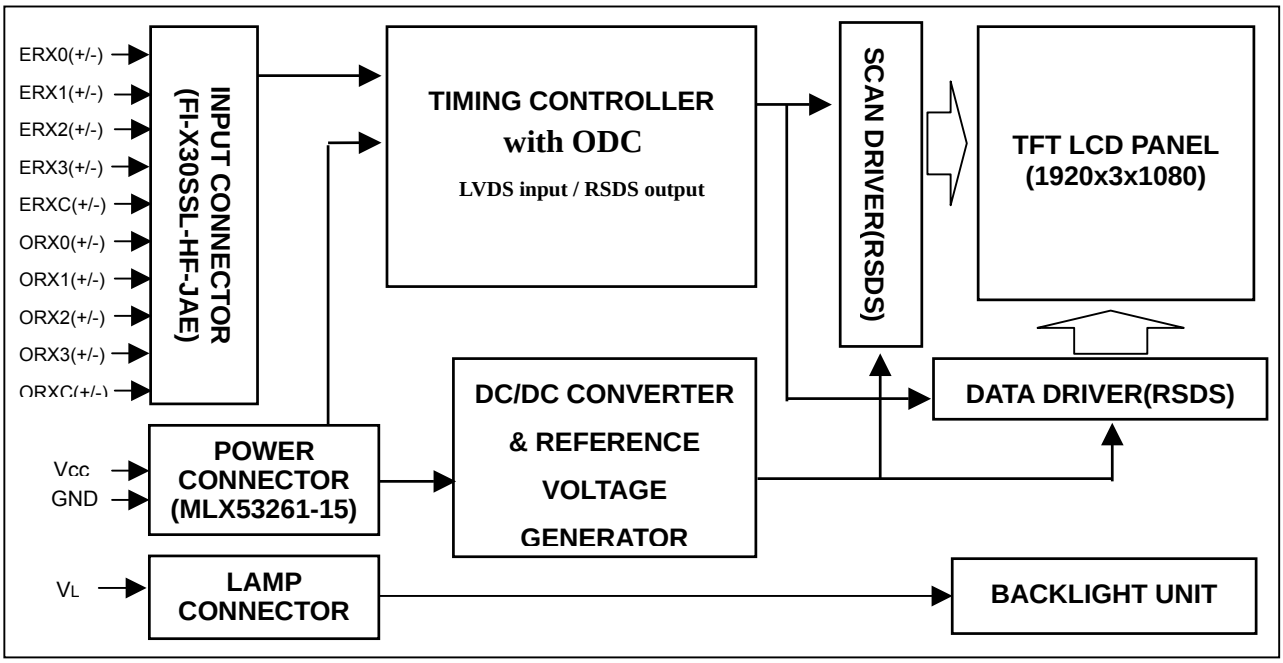
Note (3) The power on sequence was defined as following. Before BLON signal raised, the input power

V_{BL} shall maintain a BLON Delay Time (T_{on}) time in advance.



4. BLOCK DIAGRAM

4.1 TFT LCD MODULEL



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE SIGNAL INPUT

Pin	Name	Description
1	GND	Ground
2	NC	No Connection
3	NC	No Connection
4	NC	No Connection
5	NC	No Connection
6	NC	No Connection
7	NC	No Connection
8	GND	Ground
9	ERX0-	Even pixel, negative LVDS differential data input, channel 0
10	ERX0+	Even pixel, positive LVDS differential data input, channel 0
11	ERX1-	Even pixel, negative LVDS differential data input, channel 1
12	ERX1+	Even pixel, positive LVDS differential data input, channel 1
13	ERX2-	Even pixel, negative LVDS differential data input, channel 2
14	ERX2+	Even pixel, positive LVDS differential data input, channel 2
15	ECLK-	Even pixel, negative LVDS differential clock input
16	ECLK+	Even pixel, positive LVDS differential clock input
17	ERX3-	Even pixel, negative LVDS differential data input, channel 3
18	ERX3+	Even pixel, positive LVDS differential data input, channel 3
19	GND	Ground
20	ORX0-	Odd pixel, negative LVDS differential data input, channel 0
21	ORX0+	Odd pixel, positive LVDS differential data input, channel 0
22	ORX1-	Odd pixel, negative LVDS differential data input, channel 1
23	ORX1+	Odd pixel, positive LVDS differential data input, channel 1
24	ORX2-	Odd pixel, negative LVDS differential data input, channel 2
I25	ORX2+	Odd pixel, positive LVDS differential data input, channel 2
26	OCLK-	Odd pixel, negative LVDS differential clock input
27	OCLK+	Odd pixel, positive LVDS differential clock input
28	ORX3-	Odd pixel, negative LVDS differential data input, channel 3
29	ORX3+	Odd pixel, positive LVDS differential data input, channel 3
30	GND	Ground

Note (1) Connector Part No.: FI-X30SSL-HF (JAE)

5.2 TFT LCD MODULE POWER INPUT

Pin	Name	Description
1	VCC	Power input (+18V)
2	VCC	Power input (+18V)
3	VCC	Power input (+18V)
4	VCC	Power input (+18V)
5	VCC	Power input (+18V)
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND -	Ground
10	GND	Ground
11	NC	No Connection
12	NC	No Connection
13	NC	No Connection
14	NC	No Connection
15	NC	No Connection

Note (1) Connector Part No.: MLX53261-15

5.3 BACKLIGHT UNIT

The pin configuration for the connector is shown in the table below.

CN3-CN12: **BHR-03VS-1**

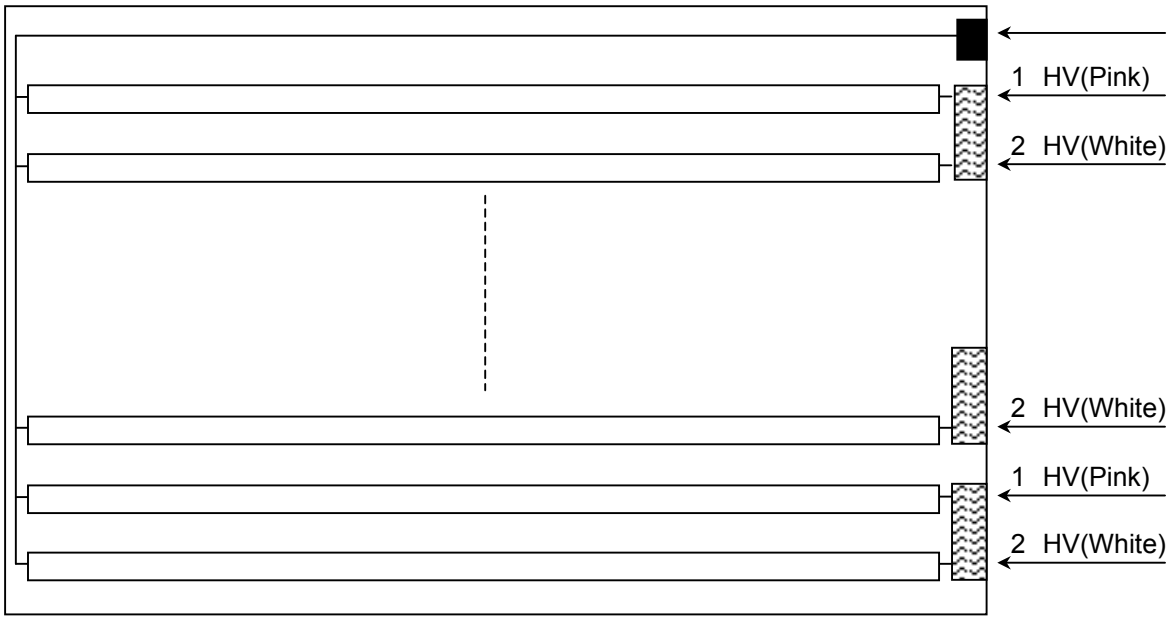
Pin №	Signal name	Feature	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface connector for high voltage side is a model **BHR-03VS-1**, manufactured by JST. The mating connector on inverter part number is SM02(12.0)B-BHS-1-TB or equivalent.

CN10: **ZHR-2** or equivalent

Pin №	Signal name	Feature	Wire Color
1	LV	Low Voltage	Black
2	LV	Low Voltage	Black
3	LV	Low Voltage	Black
4	LV	Low Voltage	Black
5	LV	Low Voltage	Black
6	LV	Low Voltage	Black
7	LV	Low Voltage	Black
8	LV	Low Voltage	Black
9	LV	Low Voltage	Black
10	LV	Low Voltage	Black

Note (2) The backlight interface connector for low voltage side is a model **ZHR-2**, manufactured by JST or equivalent. The mating connector on inverter part number is S10ZR-SM3A-TF(JST) or equivalent.



5.4 INVERTER UNIT

Note : (1) The inverter input power source connector CN1 is a model S8-PH-SM3-TB, manufactured by JST or equivalent. The inverter interface connector CN2 for control signal is a model S10-PH-SM3-TB, manufactured by JST or equivalent.

CN1: S8B-PH-SM3-TB(JST)

Pin №	Signal name	Feature
1	VBL	+120V
2		
3		
4	NC	NC
5		
6	GND	GND
7		
8		

CN2: S10-PH-SM3-TB(JST)

Pin №	Signal name	Feature
1	GND	GND
2		
3		
4	Vcc	+18V
5		
6	SYN	Synchronous Control
7	SEL	Internal/External PWM Selection
8	I_PWM	Internal PWM Control
9	I_PWM	Internal PWM Control
10	BLON	BL ON/OFF

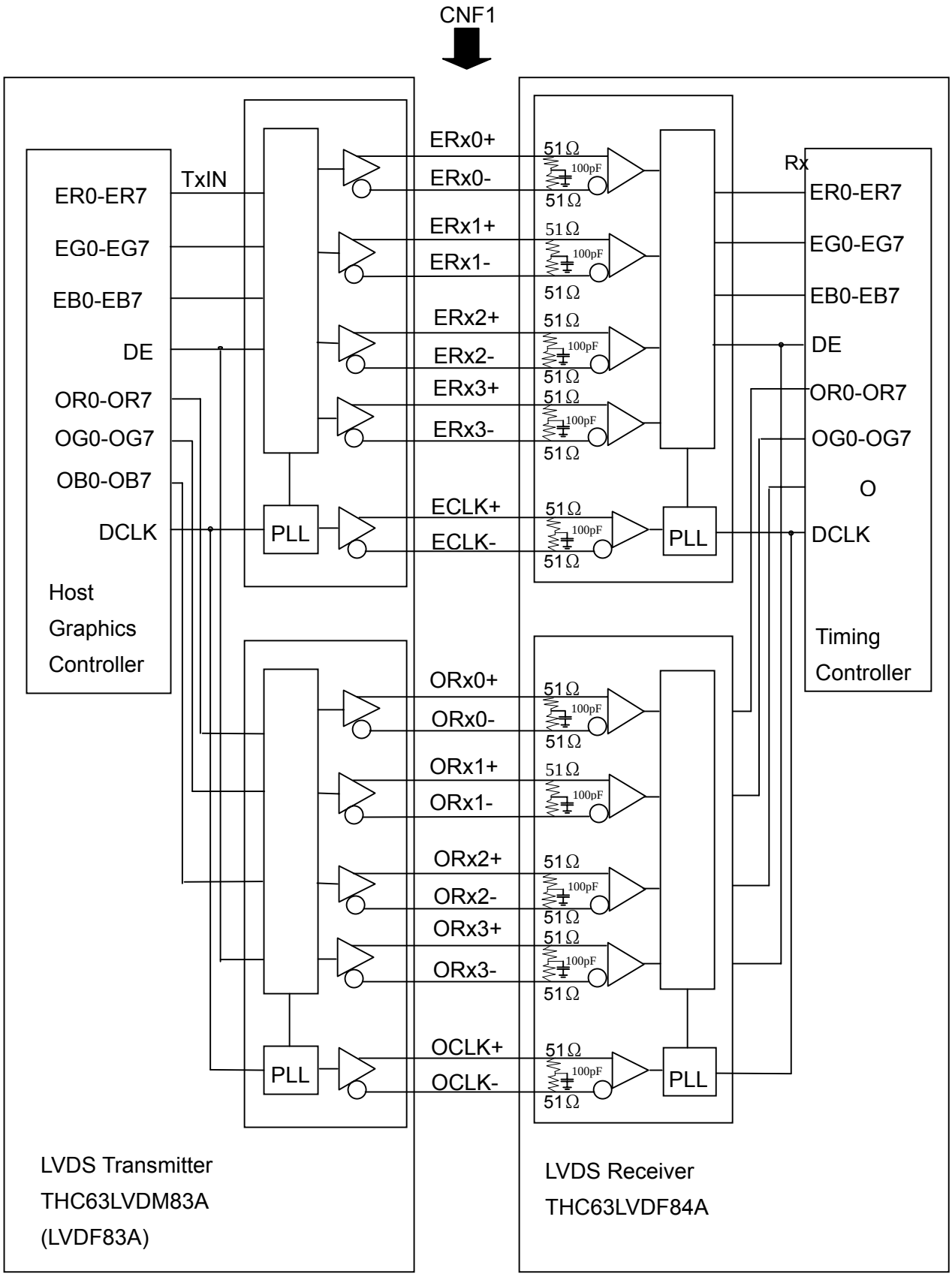
CN3-CN12: SM02(12.0)B-BHS-1-TB(JST)

Pin №	Signal name	Feature
1	CFL HOT	CFL High voltage
2	CFL HOT	CFL High voltage

CN13: S10ZR-SM3A-TF(JST) or equivalent

Pin №	Signal name	Feature
1	Return cable	CFL Low voltage
2	Return cable	CFL Low voltage
3	Return cable	CFL Low voltage
4	Return cable	CFL Low voltage
5	Return cable	CFL Low voltage
6	Return cable	CFL Low voltage
7	Return cable	CFL Low voltage
8	Return cable	CFL Low voltage
9	Return cable	CFL Low voltage
10	Return cable	CFL Low voltage

5.5 BLOCK DIAGRAM OF INTERFACE



ER0~ER7 : Even pixel R data
EG0~EG7 : Even pixel G data
EB0~EB7 : Even pixel B data
OR0~OR7 : Odd pixel R data
OG0~OG7 : Odd pixel G data
OB0~OB7 : Odd pixel B data
DE : Data enable signal
DCLK : Data clock signal

Notes: (1) The system must have the transmitter to drive the module.
(2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.6 LVDS INTERFACE

	SIGNAL	TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT
		PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	
24bit	R0	51	TxIN0			27	Rx OUT0	R0
	R1	52	TxIN1			29	Rx OUT1	R1
	R2	54	TxIN2	TA OUT0+	Rx 0+	30	Rx OUT2	R2
	R3	55	TxIN3			32	Rx OUT3	R3
	R4	56	TxIN4			33	Rx OUT4	R4
	R5	3	TxIN6	TA OUT0-	Rx 0-	35	Rx OUT6	R5
	G0	4	TxIN7			37	Rx OUT7	G0
	G1	6	TxIN8			38	Rx OUT8	G1
	G2	7	TxIN9			39	Rx OUT9	G2
	G3	11	TxIN12	TA OUT1+	Rx 1+	43	Rx OUT12	G3
	G4	12	TxIN13			45	Rx OUT13	G4
	G5	14	TxIN14			46	Rx OUT14	G5
	B0	15	TxIN15	TA OUT1-	Rx 1-	47	Rx OUT15	B0
	B1	19	TxIN18			51	Rx OUT18	B1
	B2	20	TxIN19			53	Rx OUT19	B2
	B3	22	TxIN20			54	Rx OUT20	B3
	B4	23	TxIN21	TA OUT2+	Rx 2+	55	Rx OUT21	B4
	B5	24	TxIN22			1	Rx OUT22	B5
	DE	30	TxIN26			6	Rx OUT26	DE
	R6	50	TxIN27	TA OUT2-	Rx 2-	7	Rx OUT27	R6
	R7	2	TxIN5			34	Rx OUT5	R7
	G6	8	TxIN10			41	Rx OUT10	G6
	G7	10	TxIN11			42	Rx OUT11	G7
	B6	16	TxIN16	TA OUT3+	Rx 3+	49	Rx OUT16	B6
	B7	18	TxIN17			50	Rx OUT17	B7
	RSVD 1	25	TxIN23			2	Rx OUT23	Not connect
	RSVD 2	27	TxIN24	TA OUT3-	Rx 3-	3	Rx OUT24	Not connect
	RSVD 3	28	TxIN25			5	Rx OUT25	Not connect
	DCLK	31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Display timing signal

Notes: (1) RSVD(reserved)pins on the transmitter shall be “H” or “L”.

5.7 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	R7	R6	G5	G4	G3	G2	G1	G0	R7	R6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

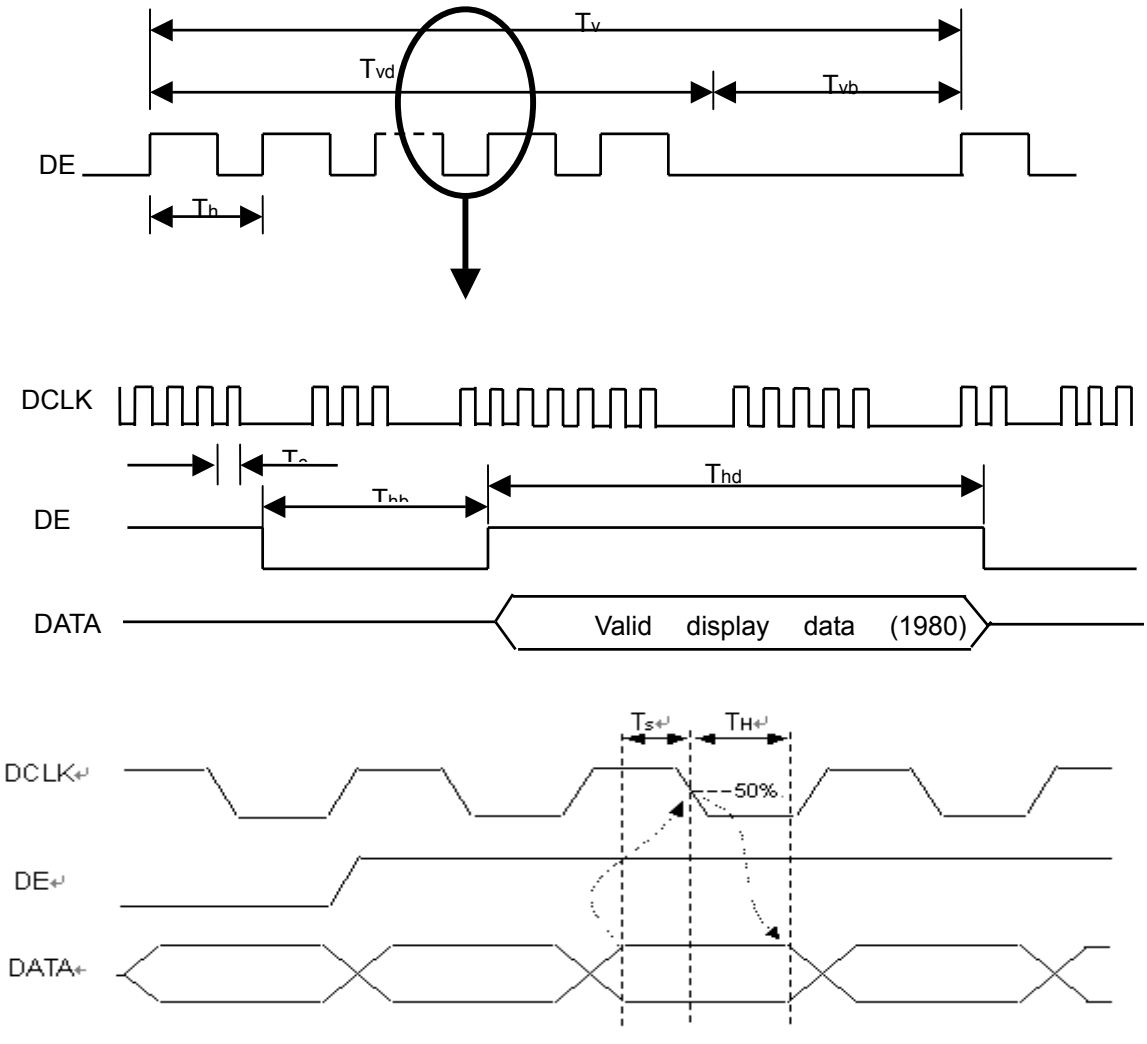
6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Clock	Frequency	1/Tc	(120)	148.5	(160)	MHZ	-
Vertical Active Display Term	Frame Rate	Fr	(57)	60	(63)	Hz	Tv=Tvd+Tvb
	Total	Tv	(1115)	(1125)	(1135)	Th	-
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	(35)	45	(55)	Th	-
Horizontal Active Display Term	Total	Th	(2100)	2200	(2300)	Tc	Th=Thd+Thb
	Display	Thd	1920	1920	1920	Tc	-
	Blank	Thb	(180)	280	(380)	Tc	-
Input data Term	Setup time	Ts	TBD	TBD	TBD	ns	
	Hold time	TH	TBD	TBD	TBD	ns	

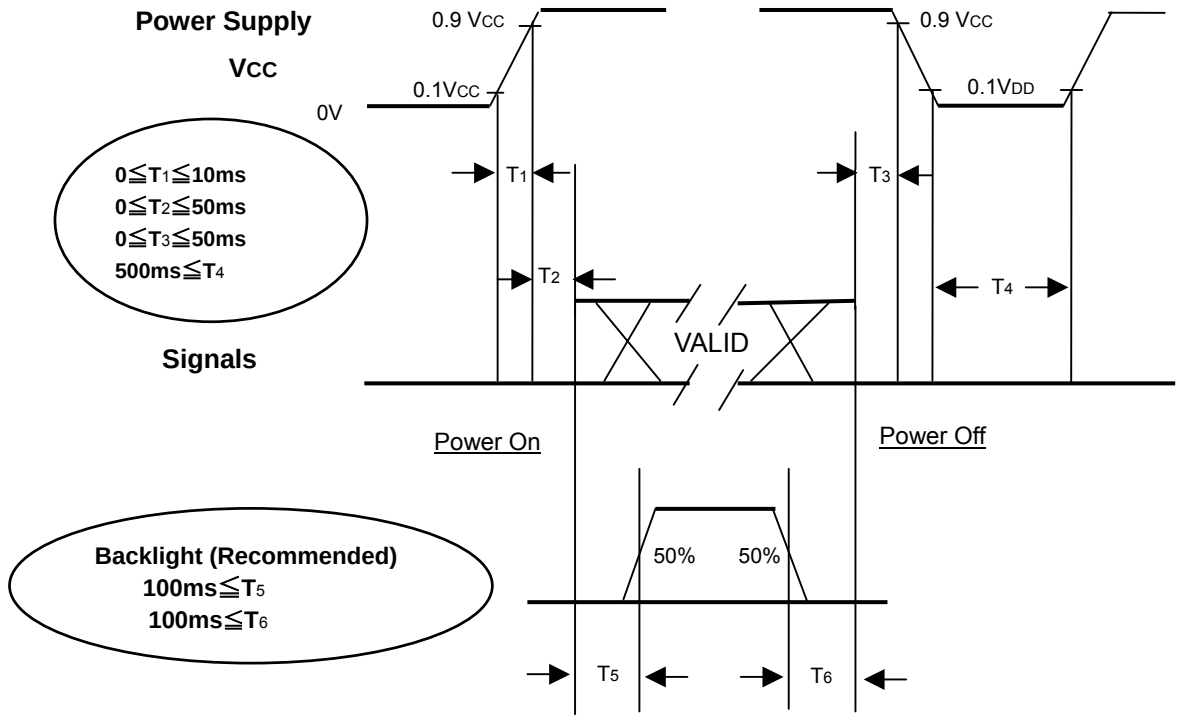
Note: Because of this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

INPUT SIGNAL TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF

Note.

(1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.

(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation of the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case of VCC = off level, please keep the level of input signals on the low or keep a high impedance.

(4) T4 should be measured after the module has been fully discharged between power of and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

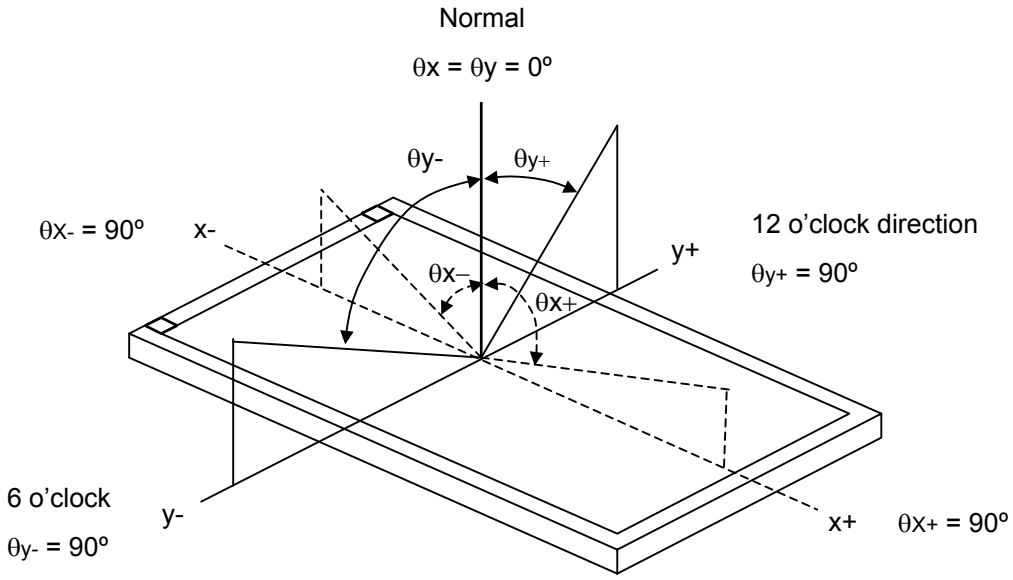
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I_L	(5.5)	mA
Inverter Driving Frequency	F_L	54	KHz
Inverter	--		

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (7).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	-	(700)	-	-	Note(2)
Response Time		T_R		-	(15)	-	ms	Note(3)
		T_F		-	(10)	-	ms	
		Gray to gray			(16.6)		ms	Note(4)
Center Luminance of White		L_C			(550)	-	cd/m^2	Note(5)
Average Luminance of White		L_{AVE}			(500)	-	cd/m^2	
White Variation		δW		-	-	1.3	-	Note(8)
Cross Talk		CT		-	-	4.0	%	Note(6)
Color Chromaticity	Red	Rx			(0.652)		-	
		Ry			(0.333)		-	
	Green	Gx			(0.273)		-	
		Gy			(0.604)		-	
	Blue	Bx			(0.140)		-	
		By			(0.076)		-	
	White	Wx			0.285		-	9, 300K
		Wy			0.293		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	(80)	(85)	-	Deg.	No gray scale inversion
		θ_x-		(80)	(85)	-		
	Vertical	θ_Y+		(80)	(85)	-		
		θ_Y-		(80)	(85)	-		

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

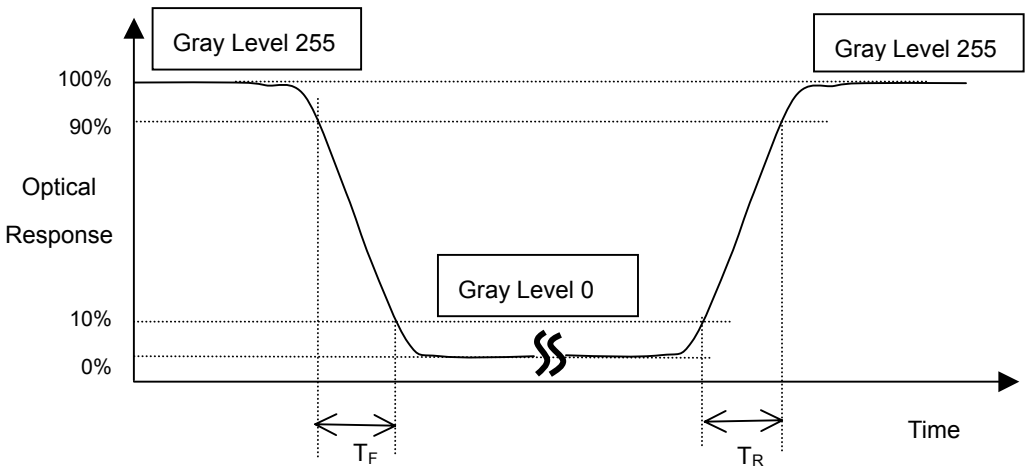
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

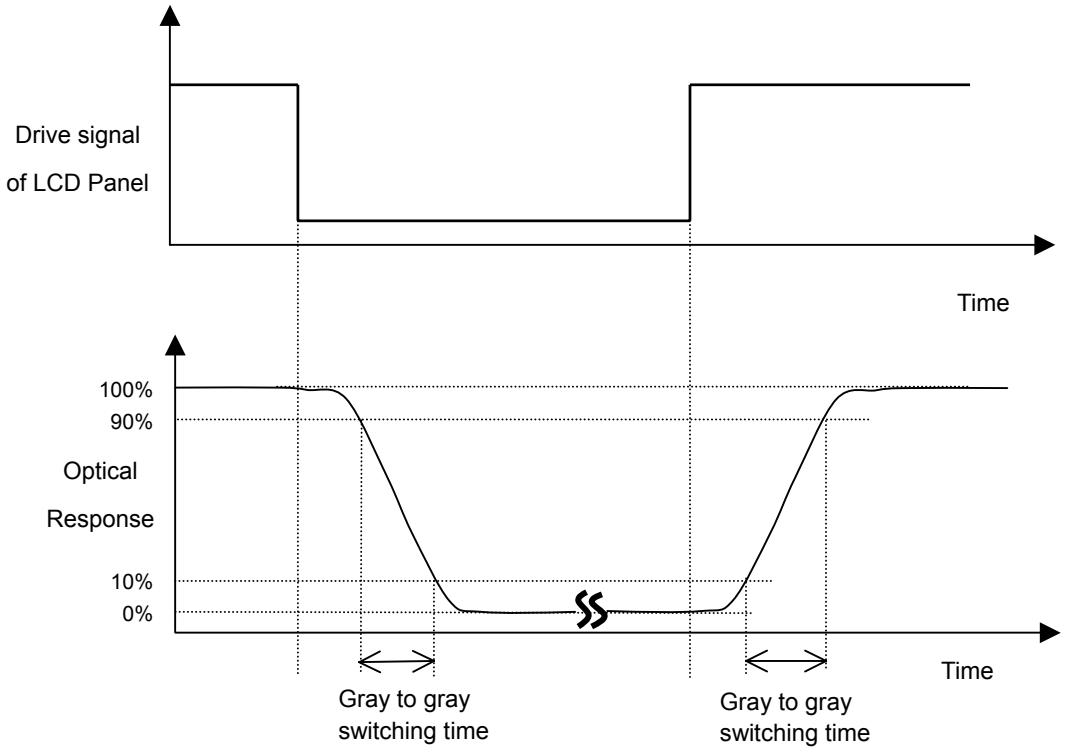
CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (8).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Gray to Gray Switching Time:



Note (5) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L(5)$

$L_{AVE} = [L(1)+ L(2)+ L(3)+ L(4)+ L(5)] / 5$

L (x) is corresponding to the luminance of the point X at the figure in Note (8).

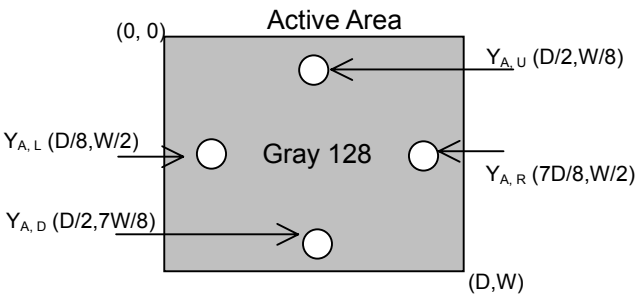
Note (6) Definition of Cross Talk (CT):

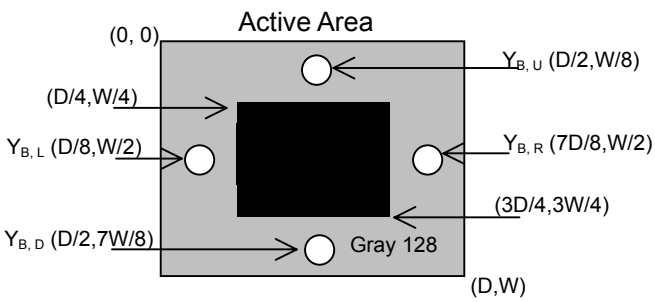
$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where:

Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

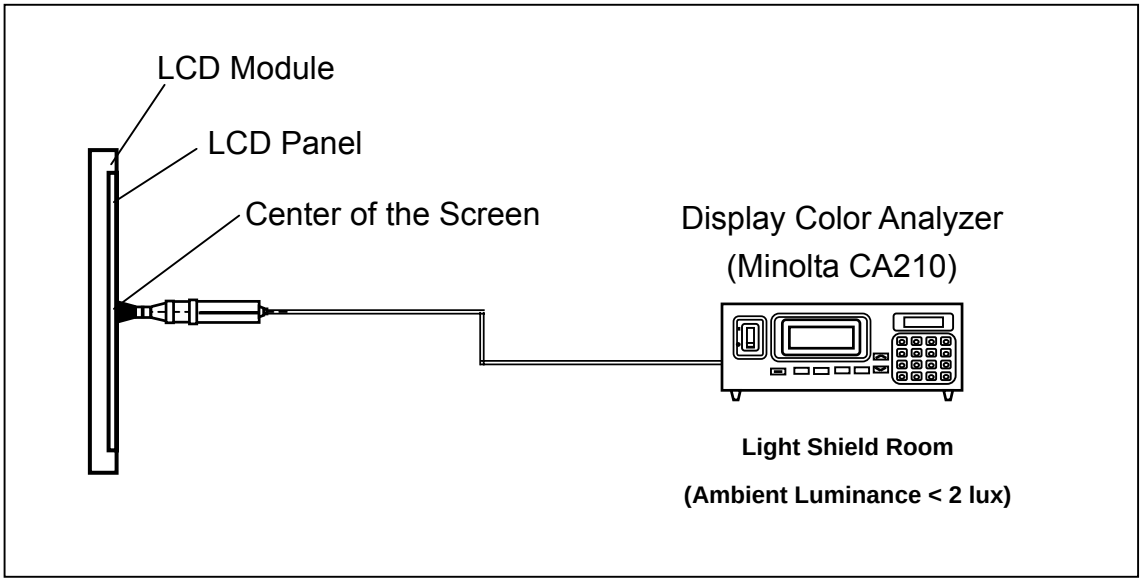
Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)





Note (7) Measurement Setup:

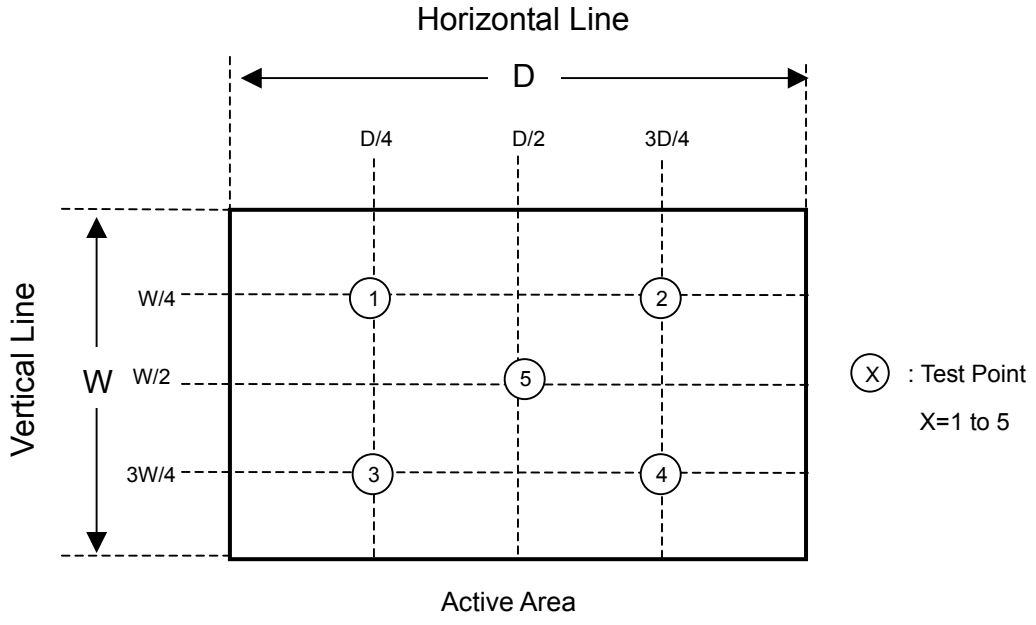
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



Note (8) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.

(4) Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.

(5) Do not pull the I/F connector in or out while the module is operating.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.

(9) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

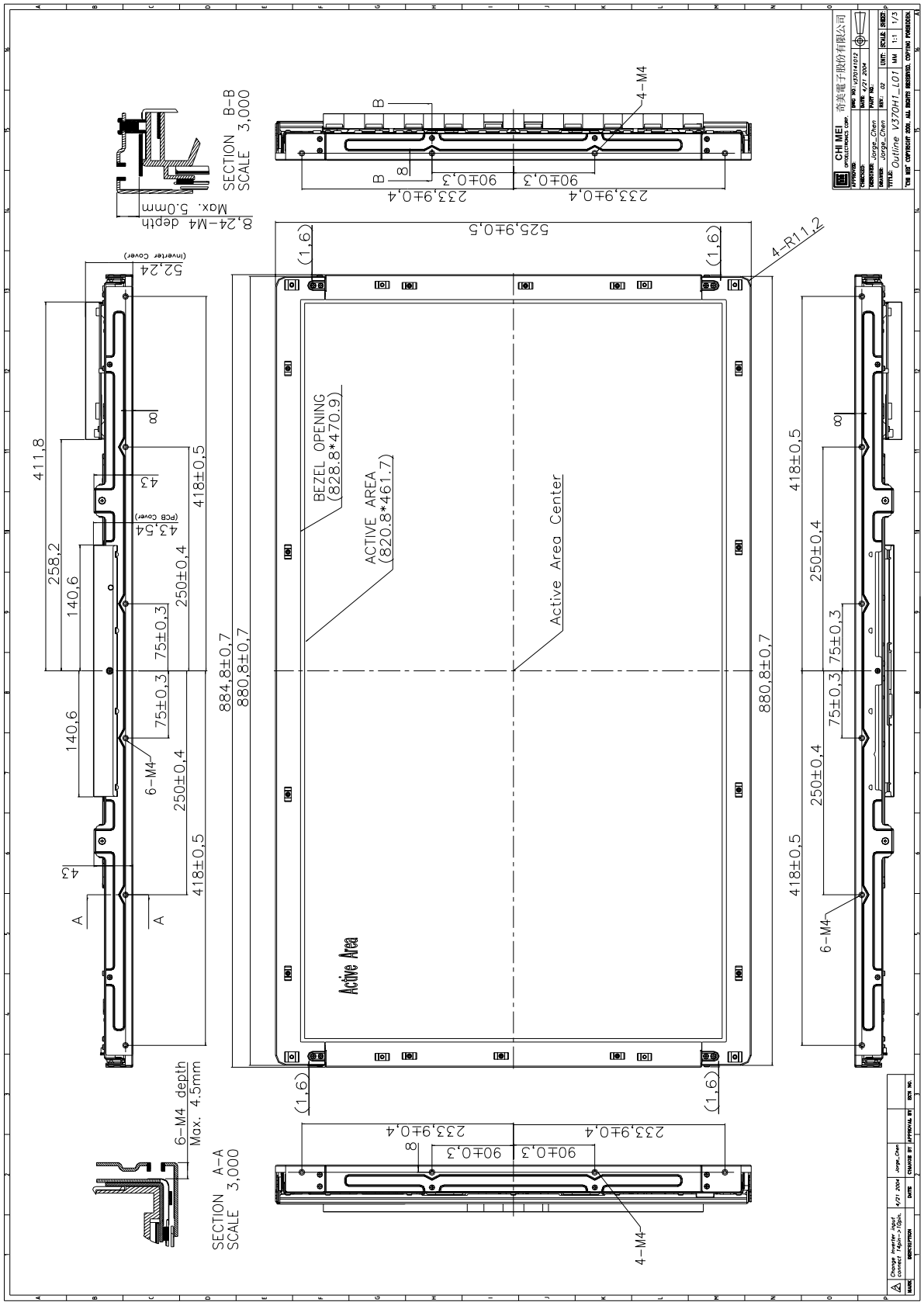
(10) When ambient temperature is lower than 10ºC may reduce the display quality. For example, the response time will become slowly, and the starting voltage of CCFL will be higher than room temperature.

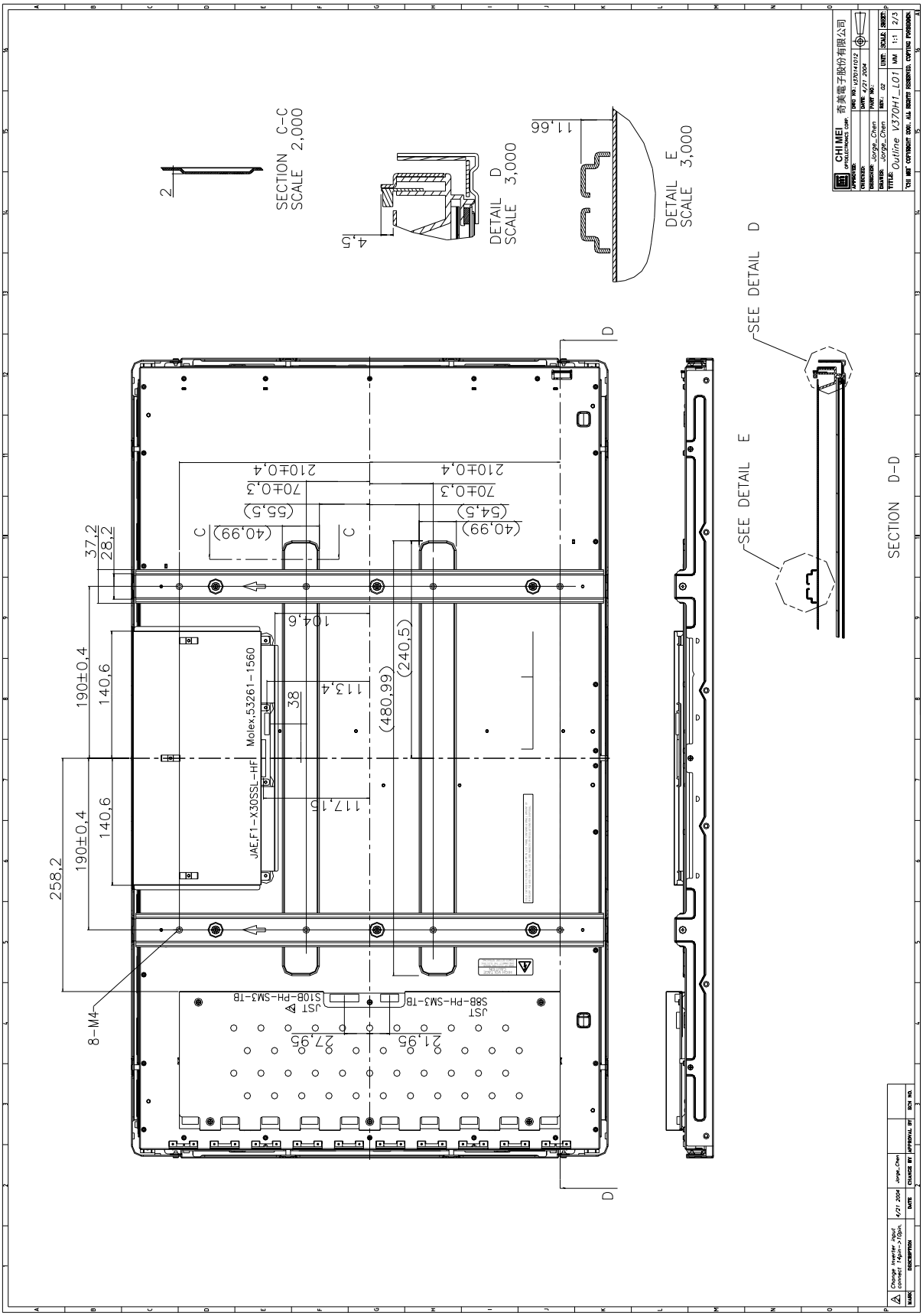
8.2 SAFETY PRECAUTIONS

(1) The startup voltage of Backlight is approximately 1700 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.





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