silicon systems®
A TDK Group Company

SSI 78P236
DS-3 Line Interface

December 1992

DESCRIPTION

The SSI 78P236 is a line interface transceiver IC intended for DS-3 (44.736 Mbit/s) applications. The receiver has a very wide dynamic range and is designed to accept B3ZS-encoded Alternate-Mark Inversion (AMI) inputs; it provides clock, positive data, negative data, and low-level signal detector logical outputs. The transmitter converts clock and data input signals into AMI pulses of the appropriate shape for transmission. A line buildout (LBO) equalizer may be selected to shape the outgoing pulses for shorter line lengths. The SSI 78P236 requires a single 5-volt supply and is available in DIP and surface mount packages.

FUNCTIONAL DESCRIPTION

The SSI 78P236 is a single chip line interface IC designed to work with 44.736 Mbit/s DS-3 signals. The receiver recovers 44.736 MHz clock, positive data and negative data from an Alternate Mark Inversion (AMI) signal which has travelled a maximum of 450 feet from a DSX3 crosspoint over 75Ω coaxial cable (cable type WECO 728A, RG-59B or equivalent). The wide dynamic range of SSI 78P236 allows for additional resistive attenuation. The input DS-3 signal should be B3ZS coded.

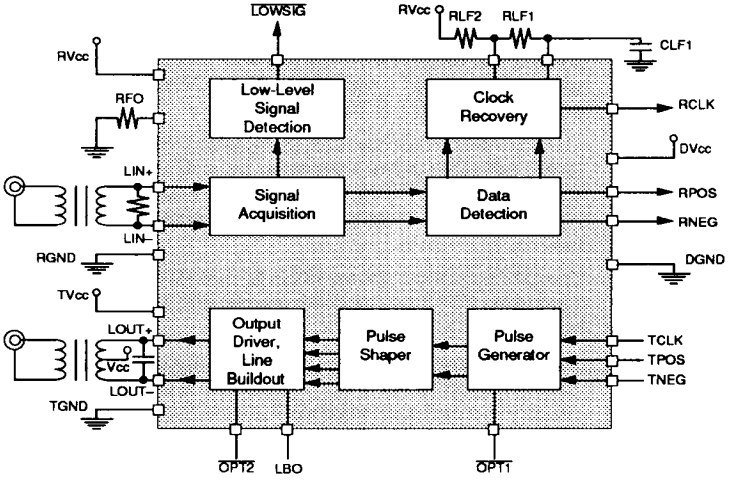
(continued)

FEATURES

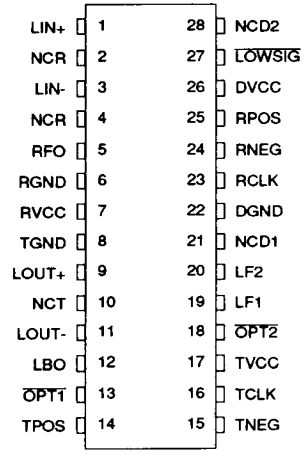
- **Single chip transmit and receive interface for DS-3 (44.736 Mbit/s) applications**
- **Unique clock recovery circuit, requires no crystals, tuned components or external clock**
- **Selectable transmit line buildout (LBO) to accommodate shorter line lengths**
- **Standard CMOS level unipolar POS and NEG data and CLK ports**
- **Compliant with ANSI T1.102 - 1987, TR-TSY-000499 and CCITT G.703**
- **Low-level input signal indication**
- **Available in DIP or surface mount packages**
- **-40°C to +85°C operating range**
- **Pin-compatible with SSI 78P2361, 78P2362 and 78P7200**

5

BLOCK DIAGRAM



PIN DIAGRAM



28-Pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION (continued)

The transmitter accepts CMOS level logical clock, positive data and negative data and converts them to the AMI signal to drive a 75Ω coaxial cable. Programmable internal Line Buildout (LBO) circuitry eliminates the need for external LBO networks. The shape of the transmitted signal through any cable length of 0 to 450 feet complies with the published templates of ANSI T.102-1987, CCITT G.703 and TR-TSY-000499. The SSI 78P236 is designed to work with a B3ZS coded signal. The B3ZS encoding and decoding functions are normally included in the DS-3 framer ICs or can easily be implemented in a PAL.

RECEIVER

The receiver input is normally transformer-coupled to the DS-3 signal. The inputs to the IC are internally referenced to RVCC so that when no transformer is used, a DC blocking capacitor of 0.01 µF should be used to isolate these pins from the DS-3 signal. Since the input impedance of the SSI 78P236 is high, the DS-3 line must be terminated in 75Ω. The input signal to the SSI 78P236 must be limited to a maximum of three consecutive zeros using a coding scheme such as B3ZS or HDB3.

The DS-3 signal is input to a variable gain differential amplifier whose output is maintained at a constant voltage level regardless of the input voltage level. The gain of this amplifier is adjusted by detecting the peak of the signal and comparing it to a fixed reference.

The output of the variable gain amplifier is compared to a threshold value which is a fixed percentage of the signal peak. In this way, even though the input signal amplitude may fall below the minimum value that can be regulated by the variable gain circuit, the proper detection threshold is maintained.

Output of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase locked loop which has an auxiliary frequency-sensitive acquisition loop which is active only when cycle-slipping occurs between the received signal rate and the internal oscillator.

This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high precision and/or adjustable oscillator or tuned circuits. The response characteristic for the phase locked loop is established by external filter components, RLF1, RLF2 and CLF1. The values of these components are specified such that the bandwidth of the phase locked loop is greater than 200 kHz.

The jitter tolerance of the SSI 78P236 exceeds the requirements of TR-TSY-000499 for the category II of equipments. The jitter transfer function is maximally flat so the IC doesn't add any jitter to the system.

Figure 2 shows the recovered clock (RCLK), positive data (RPOS) and negative data (RNEG) signals timing. The data is valid on the rising edge of the clock. The minimum setup and hold times allow easy interface to all DS-3 framer circuits. These signals are CMOS-level outputs.

Should the input signal fall below a minimum value, the $\overline{\text{LOWSIG}}$ pin goes active low. A time delay is provided before this output is active so the transient interruptions do not needlessly cause the indication.

TRANSMITTER

The transmitter accepts unipolar CMOS-level logical clock, positive data and negative data signals (TCLK, TPOS, TNEG) and generates high current drive pulses on the LOUT+ and LOUT- pins. When properly connected to a center tapped transformer, an AMI pulse is generated which can drive a 75Ω coaxial cable (type WE728A or RG59B).

Figure 3 shows the timing for the transmitter logic signals. The output pulse width is internally set and is not sensitive to input clock (TCLK) pulse width.

When a recommended transformer is used, the transmitted pulse shape at the end of a 75Ω terminated cable of 0 to 450 feet will fit the template for DSX3 pulse published in ANSI T1.102-1987, BELLCORE TR-TSY-000499 and CCITT G.703 documents.

The SSI 78P236 incorporates a selectable Line Buildout (LBO) equalizer in the transmitter path. The LBO pin should be set HIGH if the cable is shorter than 225 feet. For longer cable lengths, the LBO pin should be set low.

The $\overline{\text{OPT1}}$ pin should be set HIGH for normal operation. Setting the $\overline{\text{OPT1}}$ pin to LOW increases the transmitter power.

The $\overline{\text{OPT2}}$ pin should be set HIGH for normal operation. Setting the $\overline{\text{OPT2}}$ pin to LOW disables the transmitter circuitry and reduces the power consumption of the IC by 125 mW.

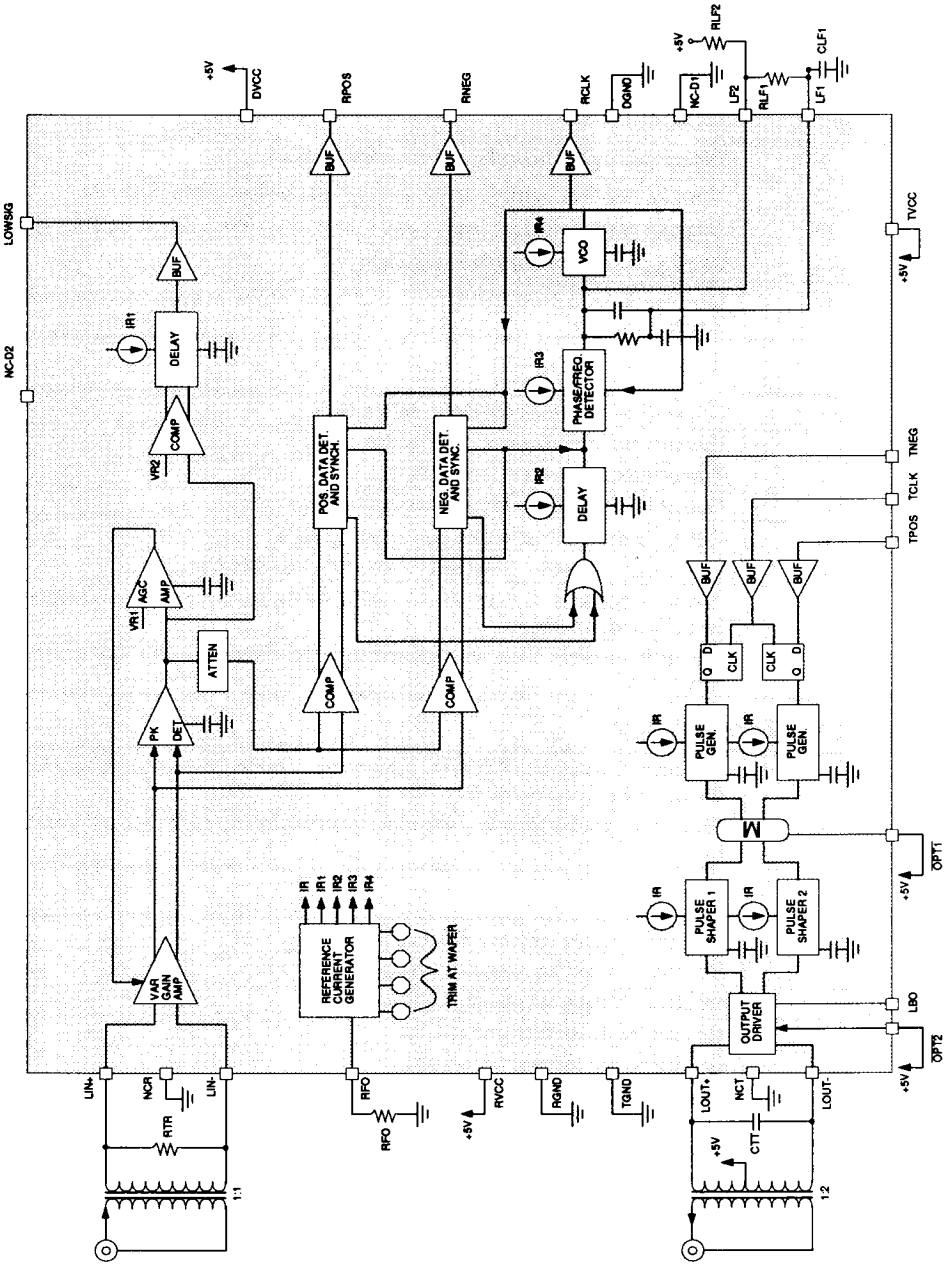


FIGURE 1: Functional Diagram

Note: NC pins should be tied to the ground pin indicated by the trailing letter.

5

PIN DESCRIPTION

RECEIVER

NAME	TYPE	DESCRIPTION
LIN+, LIN-	I	Differential inputs, transformer-coupled from line.
RPOS	O	Unipolar receiver output, active as result of positive pulse at inputs.
RNEG	O	Unipolar receiver output, active as result of negative pulse at inputs.
RCLK	O	Clock pulses recovered from line data.
$\overline{\text{LOWSIG}}$	O	Low signal logic output indicating that input signal is less than threshold value.

TRANSMITTER

TPOS	I	Unipolar transmitter data input, active high.
TNEG	I	Unipolar transmitter data input, active high.
TCLK	I	Transmitter clock input, active high.
LOUT+	O	Output to transformer for positive data pulses.
LOUT-	O	Output to transformer for negative data pulses.
LBO	I	Line buildout control. Selected for shorter cable lengths.
$\overline{\text{OPT1}}$	I	Transmit option 1. Selects faster output pulse transition time and higher amplitude when low.
$\overline{\text{OPT2}}$	I	Transmit option 2. Disables output driver and reduces output bias current when low.

EXTERNAL COMPONENT CONNECTION

RFO	I	Resistor connected to RGND to provide basic center frequency of receiver phase locked loop oscillator.
LF1, LF2	-	Resistor-capacitor loop filter network to establish bandwidth of phase locked loop.

POWER

TVcc	-	5V power supply for transmit circuits.
RVcc	-	5V power supply for receive circuits.
DVcc	-	5V power supply for receive logic circuits.
TGND	-	Ground return for transmit circuits.
RGND	-	Ground return for receive circuits.
DGND	-	Ground return for receive logic circuits.
NCR, NCT NCD1	-	No connect. These pins are not connected to the chip. They should be tied to the appropriate ground pin (see figure 1) to minimize pin-to-pin coupling capacitance.
NCD2	-	No connect. This pin is not connected for compatibility to SSI 78P7200.

ELECTRICAL SPECIFICATIONS

(TA = -40°C to 85°C, Vcc = 5V ±5%, unless otherwise noted.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value. Operation above absolute maximum ratings may permanently damage the device.

ABSOULUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive 5.0V supply: TVcc, RVcc, DVcc	6.0	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Ambient Operating Temperature, TA	-40 to +85	°C
Pin Ratings: LIN+, LIN-, TPOS, TNEG, TCLK, LOUT+, LOUT-, LBO, RFO, LF2, LF1, $\overline{OPT1}$, $\overline{OPT2}$ Pins	-0.3 to Vcc +0.3	V
Pin Ratings: RPOS, RNEG, RCLK, $\overline{LOWSIG}$ Pins	-0.3 to Vcc +0.3	V
	or +12	mA

SUPPLY CURRENTS AND POWER

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ICC	Supply Current	Outputs Unloaded, normal operation, transmit and receive all 1's pattern		142	174	mA
P	Power Dissipation	Outputs unloaded, TA = 85°C			0.93	W

EXTERNAL COMPONENTS (Refer to Figure 1 for location of components.)

RFO	Loop center frequency resistor	1% tolerance		5.23		kΩ
RLF1	Loop filter resistor	1%		20		kΩ
RLF2	Loop filter resistor	1%		100		kΩ
CLF1	Loop filter capacitor	5%		0.22		µF
RTR	Receive termination resistor	1%		75		Ω
CTT	Transmit termination capacitor	5%			20	pF

ELECTRICAL SPECIFICATIONS (Continued)

DIGITAL INPUTS AND OUTPUTS

(CMOS-compatible pins: $\overline{\text{LOWSIG}}$, RPOS, RNEG, RCLK, TPOS, TNEG, TCLK, LBO, $\overline{\text{OPT1}}$.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIL	Input low voltage		-0.3		1.5	V
VIH	Input high voltage		3.5		Vcc +0.3	V
IIL	Input low current	VIL = 1.5V	-5.0		5.0	µA
IIH	Input high current	VIH = 3.5V	-5.0		5.0	µA
VOL	Output low voltage	IOL = 0.1 mA			1.0	V
VOH	Output high voltage	IOH = -0.1 mA	4.0			V

$\overline{\text{OPT2}}$ CHARACTERISTICS

VIL	Input low voltage	IIL = 0.4 mA			0.5	V
VIH	Input high voltage		2.0			V

RECEIVER

All of the measurements for the receiver are made with the following conditions unless otherwise stated:

1. The input signal is transformer coupled as shown in Figure 1.
2. RFO = 5.25 kΩ
3. The circuit is connected as in Figure 1.
4. The maximum cable length (type 728-A or RG-59B) to DSX-3 point is 450 ft.

VIN	Input signal voltage	Input AC-Coupled	±0.045		±1.20	Vpk
RIN	Input Resistance	Input at chip's common mode voltage	15	20	30	kΩ
VDTH	Receive data detection threshold	Relative to peak amplitude for 22.37 MHz sinusoidal input		50		%
VLOW	Receive data low signal threshold	Relative to peak amplitude for 22.37 MHz sinusoidal input		±55		mV
VLOWT	Receive data low signal delay	Relative to peak amplitude for 22.37 MHz sinusoidal input		1.5		µs
TRCF	Receive clock period			22.35		ns
TRC	Receive clock pulse width			12.24		ns
TRCPT	Receive clock positive transition time	C_L = 15 pF		4.5	6	ns
TRCNT	Receive clock negative transition time	C_L = 15 pF		4.5	6	ns

RECEIVER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TRDP TRDN	Positive or negative receive data pulse width			22.35		ns
TRDPS TRDNS	Receive data set-up time		5	11.18	13.7	ns
TRDPH TRDNH	Receive data hold time		5	11.18	13.7	ns
	Receive input jitter tolerance	sine, 60 kHz	±3.35			ns
	high frequency	to 300 kHz	0.3			UIPP
	Receive input jitter tolerance	sine, 10 Hz to 2.3 kHz	±55.88			ns
	low frequency		5.0			UIPP
KD	Clock Recovery Phase Detector Gain	All 1's data pattern KD = .418/RFO	72	80	88	µA/Rad
KO	Clock Recovery Phase Locked Oscillator Gain		12	14.5	17	Mrad/ sec. -Volt

TRANSMITTER

All of the measurements for the transmitter are made with the following conditions unless otherwise stated:

1. Transmit pulse characteristics are obtained using a line transformer which has the characteristics TBD.
2. The circuit is connected as in Figure 1.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTCF	Transmit clock repetition period			22.35		ns
TTC	Transmit clock pulse width			11.18		ns
TTCNT	Transmit clock negative transition time			4.5	6	ns
TTCPT	Transmit clock positive transition time			4.5	6	ns
TTPDS TTNDS	Transmit data set-up time		3.5	11.18		ns
TTPDH TTNDH	Transmit data hold time		3.5	11.18		ns
TTPL	Transmit positive line pulse width	Measured at transformer, LBO = Low	10.62	11.18	12.0	ns

TRANSMITTER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTNL	Transmit negative line pulse width	Measured at transformer, LBO = Low	10.62	11.18	12.0	ns
	Transmit line pulse waveshape	See Note				

Note: Characteristics are in accordance with ANSI T1.102 - 1987, Table 5 and Figure 8.

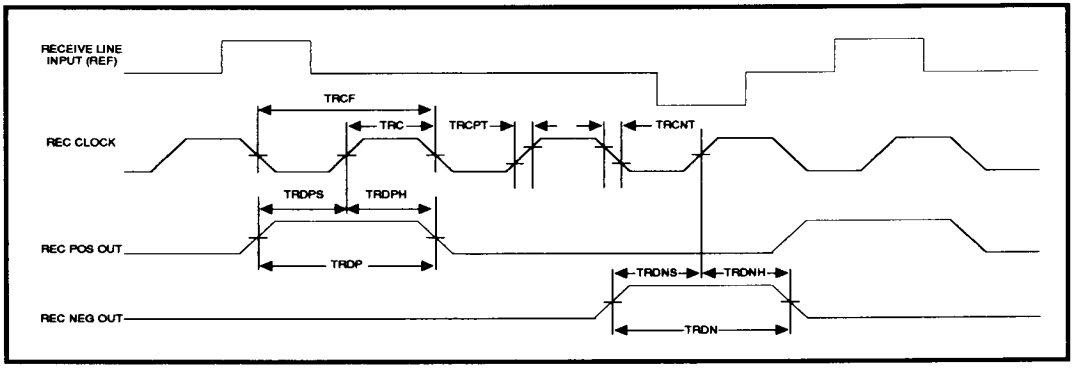


FIGURE 2: Receive Waveforms

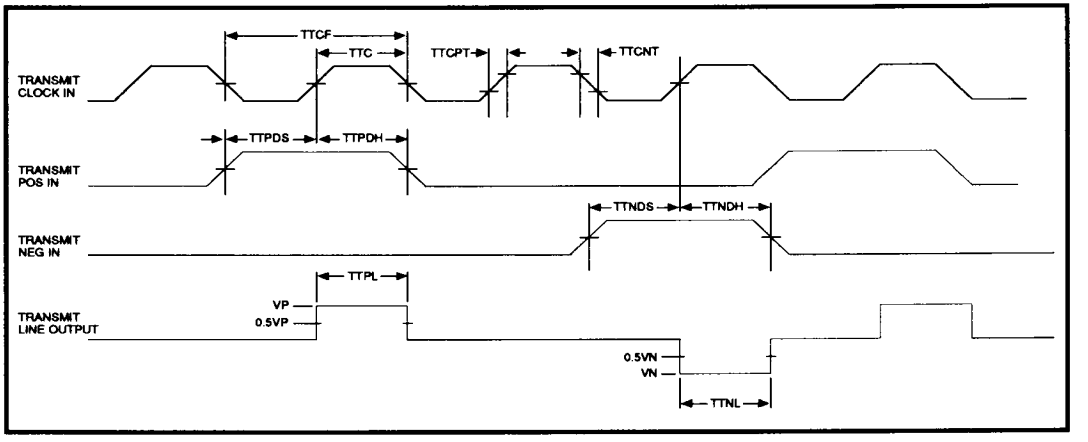
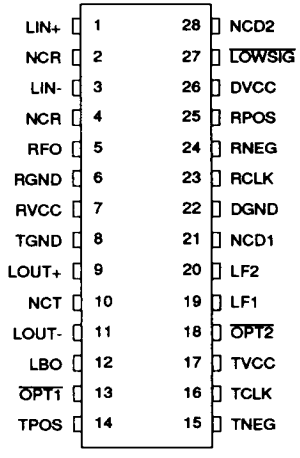


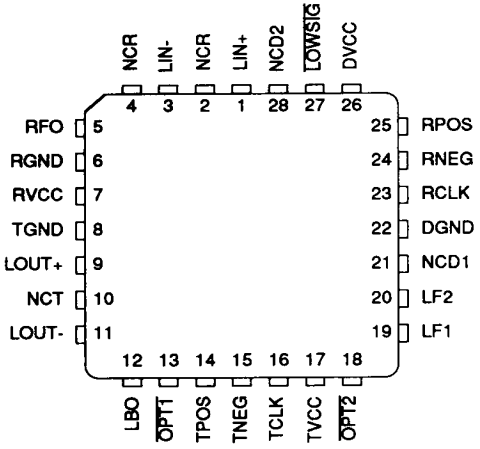
FIGURE 3: Transmit Waveforms

PACKAGE PIN DESIGNATIONS

(Top View)



28-Pin DIP



28-Pin PLCC

5

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 78P236, DS-3 Line Interface – 28-pin		
Standard Width Plastic DIP (600 mil)	78P236-IP	78P236-IP
Surface Mount 28-pin PLCC	78P236-IH	78P236-IH

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX (714) 573-6914