CYPRESS SEMICONDUCTOR

CYM1611

16K x 16 Static RAM Module

Features

- **High-density 256-kilobit SRAM module**
- **High-speed**
  - **—Access time of 12 ns**
- **16-bit-wide organization**
- **Low active power**
  - **—1.8W (max.) at 25 ns**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **—Max. height of 0.5 in.**
- **Small PCB footprint**
  - **—0.4 sq. in. (ceramic version)**
  - **—0.6 sq. in. (plastic version)**
- **2V data retention (L version)**

Functional Description

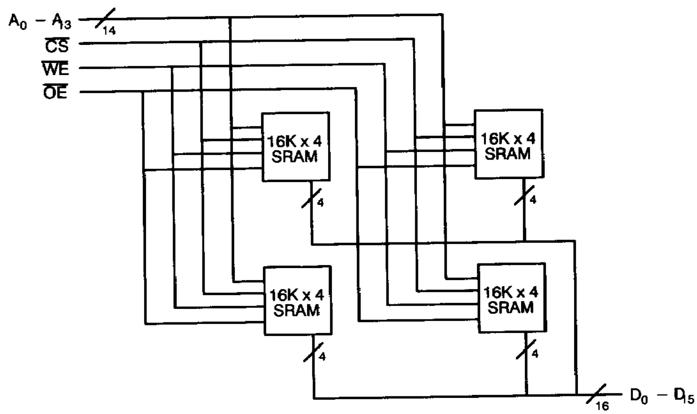
The CYM1611 is a very high performance 256-kilobit static RAM module organized as 16K words by 16 bits. The module is constructed using four 16K x 4 static RAMs mounted on a vertical substrate with pins. The vertical DIP format minimizes board space while still keeping a maximum height of 0.5 in.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the sixteen input/output pins (D_0 through D_{15}) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip select $\overline{CS}$ and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the sixteen data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



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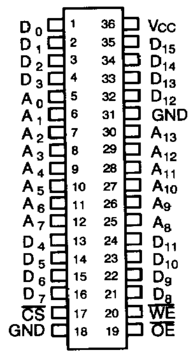
Pin Configuration

VDIP
Top View



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Selection Guide

	1611-12	1611-15	1611-20	1611-25	1611-30	1611-35	1611-45
Maximum Access Time (ns)	12	15	20	25	30	35	45
Maximum Operating Current (mA)	550	550	330	330	330	330	330
Maximum Standby Current (mA)	250	250	80	80	80	80	80

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature .... − 65°C to +125°C

Ambient Temperature with Power Applied .... −10°C to +85°C

Supply Voltage to Ground Potential .... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... − 0.5V to +7.0V

DC Input Voltage .... − 0.5V to + 7.0V

Output Current into Outputs (LOW) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	1611−12 1611−15		1611−20 1611−25 1611−30 1611−35 1611−45		Units
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = −8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	−20	+20	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	−20	+20	−20	+20	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND		−350		−350	mA
I_{CC}	V_{CC} Operating Supply	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		550		330	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		250		80	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}; $\overline{CS}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V, or V_{IN} ≤ 0.3V				80	mA

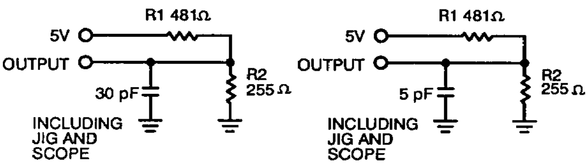
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	40	pF
C_{OUT}	Output Capacitance		15	pF

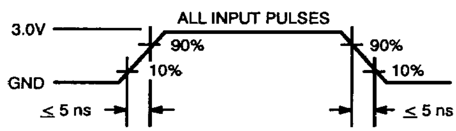
Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on a sample basis.

AC Test Loads and Waveforms



(a) (b) 1611-3



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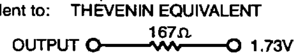
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

Parameters	Description	1611−12		1611−15		1611−20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Data Hold from Address Change	2		2		2		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[4]		8		8		8	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	3		3		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		8		8		8	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		12		15		20	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	10		12		15		ns
t_{AW}	Address Set-Up to Write End	10		12		15		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		ns
t_{SD}	Data Set-Up to Write End	10		10		10		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[4]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z	0	7	0	7	0	7	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZOE}, t_{HZCS}, and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
5. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range[3] (continued)

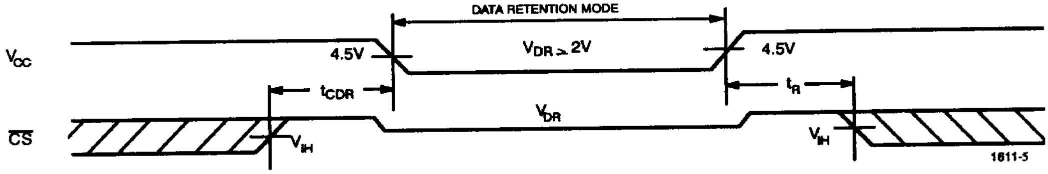
Parameters	Description	1611–25 Min.	1611–25 Max.	1611–30 Min.	1611–30 Max.	1611–35 Min.	1611–35 Max.	1611–45 Min.	1611–45 Max.	Units
READ CYCLE										
t_{RC}	Read Cycle Time	25		30		35		45		ns
t_{AA}	Address to Data Valid		25		30		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[4]		10		15		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	5		10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		10		15		15		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		20		30		35		45	ns
WRITE CYCLE[6]										
t_{WC}	Write Cycle Time	20		25		25		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		25		30		ns
t_{SD}	Data Set-Up to Write End	13		20		20		25		ns
t_{HD}	Data Hold from Write End	2		2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0	7	0	12	0	12	0	15	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z	3		5		5		5		ns

Data Retention Characteristics (L Version Only)

Parameters	Description	Test Conditions	1611 Min.	1611 Max.	Units
V_{DR}	V_{CC} for Retention of Data	$V_{CC} = 2.0V$, $\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, or $V_{IN} \leq 0.2V$	2.0		V
I_{CCDR}	Data Retention Current			4	mA
t_{CDR}	Chip Deselect to Data Retention Time		0		ns
t_R	Operation Recovery Time		t_{RC}[7]		ns
I_{LI}	Input Leakage Current			5	μA

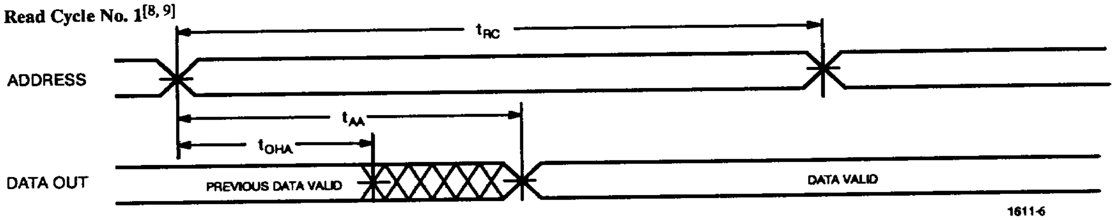
Notes:
7. t_{RC} = read cycle time.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
11. Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
12. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Data Retention Waveform

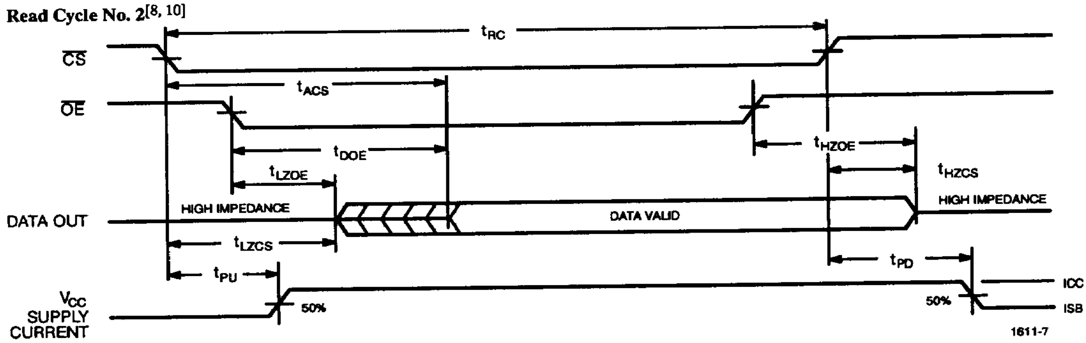


Switching Waveforms

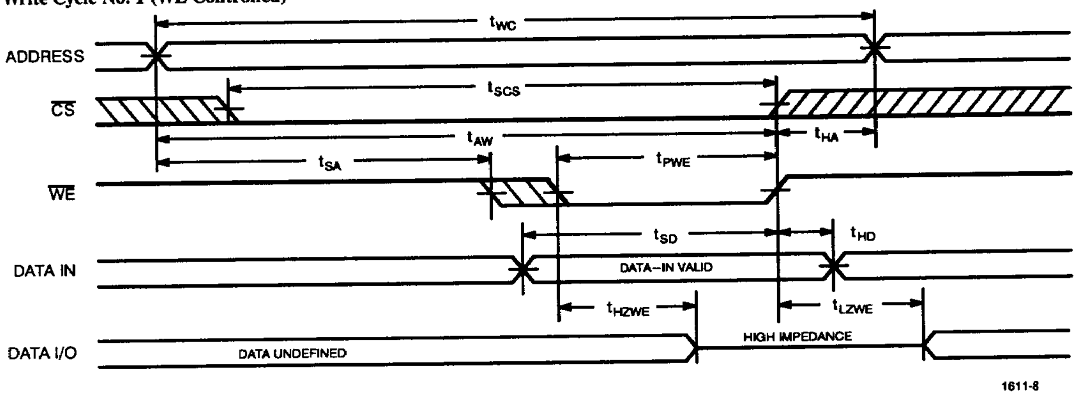
Read Cycle No. 1[8, 9]



Read Cycle No. 2[8, 10]

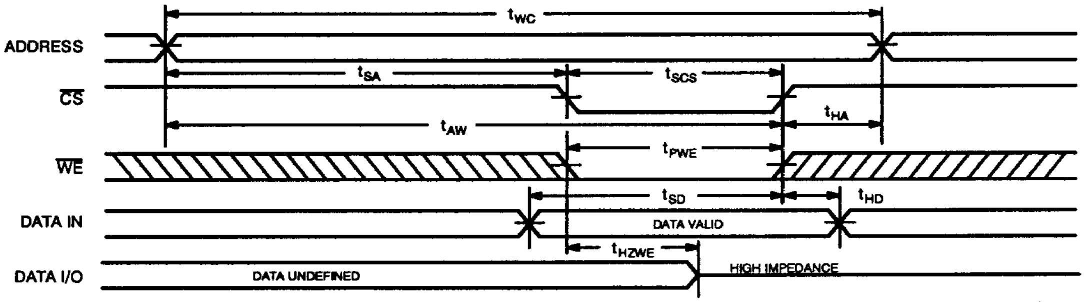


Write Cycle No. 1 ($\overline{WE}$ Controlled)[6, 11]



Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled) [6, 11, 12]



Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Inputs/ Outputs	Mode
H	X	X	High Z	Deselect/ Power-Down
L	L	H	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CYM1611HV−12C	HV01	Commercial
	CYM1611PV−12C	PV03	
15	CYM1611HV−15C	HV01	Commercial
	CYM1611PV−15C	PV03	
20	CYM1611HV−20C	HV01	Commercial
	CYM1611LHV−20C	HV01	
	CYM1611PV−20C	PV03	
	CYM1611LPV−20C	PV03	
25	CYM1611HV−25C	HV01	Commercial
	CYM1611LHV−25C	HV01	
	CYM1611PV−25C	PV03	
	CYM1611LPV−25C	PV03	
30	CYM1611HV−30C	HV01	Commercial
	CYM1611LHV−30C	HV01	
	CYM1611PV−30C	PV03	
	CYM1611LPV−30C	PV03	
35	CYM1611HV−35C	HV01	Commercial
	CYM1611LHV−35C	HV01	
	CYM1611PV−35C	PV03	
	CYM1611LPV−35C	PV03	
45	CYM1611HV−45C	HV01	Commercial
	CYM1611LHV−45C	HV01	
	CYM1611PV−45C	PV03	
	CYM1611LPV−45C	PV03	

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