HISTECH LINEAR COMPONENT DOTA SHEET

SI-Cr THIN FILM RESISTORS VALUES OF 10Ω to 100KΩ, LASER TRIMMABLE

GENERAL DESCRIPTION

HTL'S IC compatible silicon-chrome resistors are offered as an option on selected semi-custom analog arrays as well as on all custom integrated circuits. The resistors are made using a very accurate deposition process by which a thin film of high-resistivity silicon-chrome material is deposited over the field oxide surface of the chip, prior to the aluminum metalization step. This thin film resistor offers some excellent characteristics that cannot be matched by the normal IC diffused or implanted resistors. In addition to the excellent qualities of the siliconchrome resistors, they can also be laser trimmed to a very accurate matching ratio of typically $\pm 0.005\%$.

FEATURES

Wide Range of Resistor Values
Negligible Voltage Dependence
Very Low Temperature Coefficient
Very High Breakdown Voltage
Good Matching Characteristics
Very Low Temperature Drift Matching
Very Low Capacitance
Excellent Ratio of Laser Trimmed
Resistors

TYPICAL APPLICATIONS

Analog and Digital Precision Circuits
A/D and D/A Converters
Feedback Networks
Summing Amplifiers
Precision Voltage Dividers
Operational Amplifiers and Comparators
Voltage References and Regulators
Active Filters

Electrical characteristics, Prior to laser trimming, at ambient temperature $T_A = 25$ °C (Unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Sheet Resistance	Р	ν _R =5ν	800	1000	1200	Ω/Ω
Resistor-Substrate Breakdown Voltage	BV _{RS}	I _S =1μA (Note 1)	150			v
Temp. Coefficient of Resistors	ΔR/ΔΤ	V _R =5V -55°C < T _A < 125°C		-3 5	-60	PPM/°C
Matching of Equal Design Value Resistors 10 m Resistor Width 15 m Resistor Width 25 m Resistor Width 50 m Resistor Width 75 m Resistor Width 100 m Resistor Width	ΔR(1:1)	V _R =5V R ₁ = R ₂ (Note 2,3)		± 1 ± 0.5 ± 0.2 ± 0.1 ± 0.07 ± 0.05		*

Electrical characteristics, Prior to laser trimming, at ambient temperature $T_A = 25$ °C (CONTINUED)

Matching of Unequal Design Value Resistors				
10μm Resistor Width	ΔR(1:2) ΔR(1:4) ΔR(1:8)	$R_2 = 2R_1$ $R_2 = 4R_1$ $R_2 = 8R_1$ (Note 2,3)	± 2 ± 3 ± 4	
15μm Resistor Width	ΔR(1:2) ΔR(1:4) ΔR(1:8)	$R_2 = 2R_1$ $R_2 = 4R_1$ $R_2 = 8R_1$ (Note 2,3)	± 1 ± 2 ± 3	
25μm Resistor Width	ΔR(1:2) ΔR(1:4) ΔR(1:8)	$R_2 = 2R_1$ $R_2 = 4R_1$ $R_2 = 8R_1$ (Note 2,3)	± 0.5 ± 1 ± 2	
50μm Resistor Width	ΔR(1:2) ΔR(1:4) ΔR(1:8)	$R_2 = 2R_1$ $R_2 = 4R_1$ $R_2 = 8R_1$ (Note 2,3)	±0.2 ±0.5 ±1	
75μm Resistor Width	ΔR(1:2) ΔR(1:4) ΔR(1:8)	R ₂ = 2R ₁ R ₂ = 4R ₁ (Note 2,3) R ₂ = 8R ₁	± 0.15 ± 0.25 ± 0.5	
100μm Resistor Width	ΔR(1:2) ΔR(1:4) ΔR(1:8)	R ₂ = 2R ₁ R ₂ = 4R ₁ R ₂ = 8R ₁	± 0.1 ± 0.2 ± 0.3	
Temp. Coefficient of Matching Drift	ΔR(1:1)/ΔT ΔR(1:2)/ΔT ΔR(1:4)/ΔT ΔR(1:8)/ΔT	V _R =5V -55°C < TA < 125°C	± 2 ± 4 ± 8 ± 16	PPM/ ^O C
Resistor-Substrate Capacitance	C _{RS}	0 <v<sub>R<bv<sub>RS (Note 4)</bv<sub></v<sub>	0.02 3.1 •10 ⁻⁵	pF/mil ² pF/μm ²

Notes

1) Breakdown occurs through a thick layer of oxide (Field Oxide). The breakdown is destructive and non-reversible.

Resistor ratios matching is satisfied by

$$k\left(1-2\left|\frac{\Delta R_{\left(MAX\right)}}{100\lambda}\right|\right) < \frac{R_{2}}{R_{1}} < k\left(1+2\left|\frac{\Delta R_{\left(MAX\right)}}{100\lambda}\right|\right)$$

Where K is the resistor ratio of the nominal values, and $\rm R_{1}$ and $\rm R_{2}$ are any two resistors chosen from these populations on chip.

- These particular matching parameters apply to the various resistor ratios on chip, prior to laser triming. Matching of laser trimmed resistors is typically $\pm 0.005\%$.
- 4) MOS capacitance is specified. An average capacitance of 0.5pF must be added if resistor is connected to a package pin. Also included must be a capacitance of about 1pF for each bonding pad which is related to the specific resistor.

histech Linear component Datasheets

20V SMALL NPN TRANSISTOR 10ma QUAD COLLECTOR CONTACT

GENERAL DESCRIPTION

The small 10mA NPN transistor has two N+ diffusion regions in the collector area with two collector contacts in each of these diffusions. The contacts are normally connected together to reduce the series collector resistance as well as the saturation voltage. The small NPN transistor is available in two versions, with and without a deep N+ diffusion in the collector region. The deep N+ diffusion allows for an additional increase in the operating current.

FEATURES

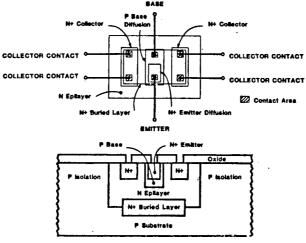
Four Collector Contacts
Matched VBE and hFE Transistor Parameters
TYPICAL, APPLICATIONS
Amplifiers
Comparators
Current Sources
Bias Circuits
Level Shifters
Emitter Followers
Diode Connected Transistors
Zener Diode Connections

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A=25^{\circ}C$ (Unless otherwise noted)

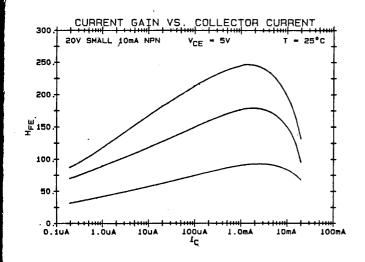
PARAMETER	SYMBOL		CONDITIONS			MIN	ТҮР	MAX	UNITS
DC Current Gain	h _{FE}	I _C =1mA	V _{CE} =5V		(Note 1)	. 80		300	
Matching of DC Current Gains	∆h _{FE}	I _C = 1mA	V _{CE} =5V		(Note 2)		±5	±10	*
Temperature Coefficient of h _{FE}	Δħ _{FE} /ΔΤ	I _C =1mA	-55°C < TA	< 125 ⁰ C			0.5		%/°(
Callanter Bass Laskage Company	,	V -20V	TA=25°C		(Note 3)		0:01	0.1	nA
Collector-Base Leakage Current	^I сво	V _{CB} =20V	TA=125°C		(Note 3)		1	10	na
Callantan Fatham Lasham Command	,	V	TA=25°C		(Note 3)		0.2	2	nA
Collector-Emitter Leakage Current	ICEO	V _{CE} =20V	TA=125°C		(Note 3)		0.2	2	μА
Collector-Emitter Breakdown Voltage	LVCEO	Ic=1mA				20			¥
Collector-Base Breakdown Voltage	вусво	1 _C =100µA				30			٧
Emitter-Base Breakdown Voltage	BV _{EBO}	IE=10hV		····		6.25		7.25	٧
Collector-Substrate Breakdown Voltage	BVCS	Ic=10µA				20			V
Base-Emitter Forward Voltage	V _{BE}	I _E = 1mA	V _{CE} =5V			0.67		0.79	٧
Matching of Base-Emitter Forward Voltages	ΔV _{BE}	I _E =1mA	VCE=5V		(Note 4)		±2	±6	m∀
Temperature Coefficient of V _{BE}	ΔV _{BE} /ΔT	I	V _{CE} =5V				-1.8		mV/°C
		I _C =lmA	(One Diffu	tor Contact sion Region)	(Note 5)		0.16	0.3	
Collector-Emitter Saturation Voltage	V _{CE} (SAT)	·	17	tor Contacts sion Regions)	(Note 5)		0.14	0.25	٧
		(I _C /I _B)=10	Four Colle (Two Diffu	sion Regions) ctor Contacts sion Regions)			0.09	0.17	
Maximum Collector Current	I _{C(MAX)}	P _{D(MAX)} =30	OmW		···			20	mА
Cutoff Frequency	f _T	I _C =5mA					500		MHz
				I _C =1mA	·		6		
Storage Time	™S	(1C/1B)=1	R _B =750Ω	I _C =10mA			100		ns
Emitter-Base Capacitance	CEB	V _{EB} =OV			(Note 6)		1		pF
Collector-Base Capacitance	ССВ	V _{CB} =0V			(Note 6)	-	1		pF
Collector-Substrate Capacitance	c _{cs}	V _{CS} =0V		***	(Note 6)		3.8		pF

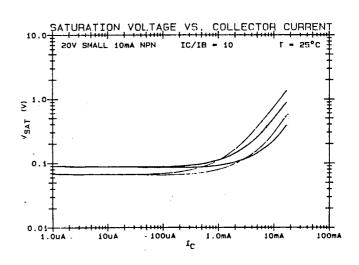
Information furnished by HI-Tech Linear is believed to be accurate and reliable. However, no responsibility is assumed by HTL for its use, nor for any infringements of pattents or other rights which may result from its use. HTL reserves the right to make changes at any time without notice.

- 1) -All collector contacts connected in parallel.
- h_{FF} matching is satisfied by 2) hFE(1) $h_{FE(1)}$ and $h_{FE(2)}$ are any two current gains chosen from a population of like transistors on chip.
- Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage. 3)
- Matching of V_{BE} is satisfied by $|V_{BE(2)} V_{BE(1)}| < 2|\Delta V_{BE(MAX)}|$ where $V_{BE(1)}$ 4) and $V_{BE(2)}$ are any two base-emitter voltages chosen from a population of like transistors on chip.
- 5) It is not recommended to operate the transistor in the saturation mode when only one collector contact or two collector contacts on the same N^+ diffusion region are used, since a high saturation voltage is inevitable, especially at increased collector currents.
- Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of lpF for each bonding pad which is related to the specific junction



Layout and Cross-Section of Small 10mA NPN Transistor (Not to Scale)





hi-tech linear component data shee

SMALL TOMA DIODE (TRANSISTOR WITH COLLECTOR AND BASE SHORTED)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A = 25^{\circ}C$ (Unless otherwise noted)

PARAMETER	SYMBOL		CONDITION		MIN	ТҮР	MAX	UNITS
,		I _F =100µA			0.61		0.73	
Forward Voltage Drop	V _F .	I _F =1mA			0.67		0.79	1 v
		I _F =10mA			0.77		0.89	1
Matching of Forward Voltages	۵۷ _F	I _F =1mA		(Note 1)		±2	±6	mV
Temperature Coefficient of V _F	ΔV _F /ΔT	I _F =1mA				-1.8		mV/°C
Leakage Current	,	V _R =20V	T _A =25°C	(Note 2)		0.1		
	I ₀	R-LOV	TA=125°C	(Note 2)		10		nA
Breakdown Voltage	BVD	I _R =10μA			6.25		7.25	٧
Maximum Diode Current	I _{F(MAX)}						20	mA
Junction Capacitance	C _J	V _n =0V		(Note 3)		1		pF

Notes:

- Matching of V_F is satisfied by $\|V_{F(2)} V_{F(1)}\| \le 2\|\Delta V_{F(MAX)}\|$ where $V_{F(1)}$ and $V_{F(2)}$ are any two forward voltages chosen from a population of like diodes on chip.
- Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.
- Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of lpF for each bonding pad which is related to the specific junction under test.

SMALL 10mA ZENER DIODE (EMITTER-BASE JUNCTION OF TRANSISTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE Ta=25°C (Unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN	ТҮР	MAX	UNITS
		I _Z =lµA		6.2	6.7	7.2	
	ļ	I _Z =10μA		6.25	6.75	7.25	1
Breakdown Voltage	v _z	I _Z =100µA	(Note 1)	6.3	6.8	7.3) v
		IZ=1mA	(Note 1)	6.4	6.9	7.4	1
•		I _Z =10mA	(Note 1)	7	7.5	8	
Dynamic Impedance (in the Breakdown Mode)	RZ	I Z=1mA			75		Ω
Temperature Coefficient of Breakdown Voltage	۵ÝZ/۵۲	I _Z =1mA			2.4		mV/ ^O C

Notes

l) Base-emitter breakdown, unlike base-collector breakdown, can be damaging to the transistor particularly for long breakdown duration at high current. Under these conditions, $h_{\rm FE}$ degradation is inevitable; therefore, $V_{\rm Z}$ is tested at $l_{\rm P}A$ and $l0_{\rm P}A$ for each transistor. Operation at higher current has been fully characterized and is guaranteed by extrapolation.

8368605 0007536 7 📗 D MISTECH LINEAR COMPONENT DATA

20V LOW NOISE NPN TRANSISTOR 10ma DUAL COLLECTOR CONTACT

GENERAL DESCRIPTION

The low noise NPN transistor is identical in size to th 10mA small NPN transistor. It has a single N+ diffusion in the collector area with two collector contacts in it. The base diffusion and the base contact are much larger than those of the small NPN transistor. This results in a much reduced base resistance and consequently in a lower level of noise. It is recommended to use the transistor at very low current levels of 10nA to 1mA to maintain the low noise characteristics.

FEATURES .

Large Base Contact for Reduced Noise **Dual Collector Contacts** Matched $v_{\mbox{\footnotesize{BE}}}$ and $h_{\mbox{\footnotesize{FE}}}$ transistor parameters TYPICAL APPLICATIONS Low Noise Amplifiers Differential Input Stages Low Level Amplifiers

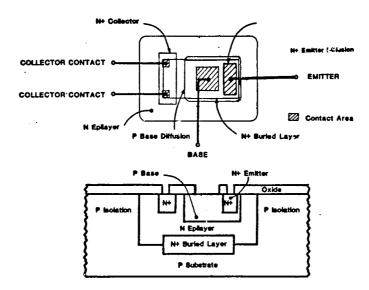
ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A=25^{\circ}C$ (Unless otherwise noted)

PARAMETER	SIMBOL		CONDITIONS			MIN	ТҮР	MAX	UNITS
DC Current Gain	h _{FE}	I _C =1mA	V _{CE} =5V		(Note 1)	80		300	
Matching of DC Current Gains	Δh _{FE}	I _C =1mA	°VcE=5V		(Note 2)		±5	±10	*
Temperature Coefficient of h _{FE}	Δh _{FE} /ΔT	I _C =1mA	-55°C < TA	< 125 ⁰ C			0.5		%/°(
			TA=25°C	····	(Note 3)		0.01	0.1	ηA
Collector-Base Leakage Current	Ісво	V _{CB} =20V	TA=1250C		(Note 3)		1	10	
			TA=25°C		(Note 3)		0.2	2	nΑ
Collector-Emitter Leakage Current	I _{CEO}	VCE=20V	TA=125°C		(Note 3)	1	0.2	2	μĄ
Collector-Emitter Breakdown Voltage	LV _{CEO}	Ic=1mA				20			٧
Collector-Base Breakdown Voltage	вусво	I _C =100µA				30			٧
Emitter-Base Breakdown Voltage	BVEBO	I _E =10µA		<u>,,</u>		6.25		7.25	V
Collector-Substrate Breakdown Voltage	BV _{CS}	1 _C =10µA				20			٧
Base-Emitter Forward Voltage	V _{BE}	1 _E =1mA	V _{CE} =5V			0.67		0.79	٧
Matching of Base-Emitter Forward Voltages	ΔVBE	I _{E-} =1mA	VCE=5V		(Note 4)		±2	±6	ψV
Temperature Coefficient of VBE	ΔV _{BE} /ΔT	I _E =1mA	V _{CE} =5V				-1.8		mV/C
Collector-Emitter Saturation	v	Ic=lmA	One Coll	ector Contac	t		0.2	0.3	V
Voltage	VCE (SAT)	(I _C /I _B)=1	Two Coll	ector Contac	ts		0.16	0.25	
Maximum Collector Current	I _C (MAX)	PD(MAX)=3	DOmW .					20	#RA
Cutoff Frequency	f _T	Ic*5mA	V _{CE} =5V				500		MHz
Storage Time	¹s	(1 _C /I _B)=1	0 R _B ≖750Ω	I _C =1mA			100		ns
Emitter-Base Capacitance	CEB	V _{EB} =OV	· · · · -	1 - 6	(Note 5)	1	1		pF
Collector-Base Capacitance	C _{CB}	V _{CB} =OV			(Note 5)		1		pF
Collector-Substrate Capacitance	c _{cs}	V _{CS} =0V	» 		(Note 5)		3.8		pF

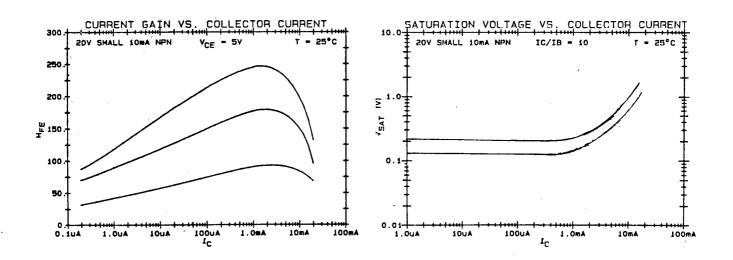
information furnished by Hi-Tech Linear is believed to be accurate and reliable. However, no responsibility is assumed by HTL for its use, nor for any infringements of pattents or other rights which may result from its use. HTL reserves the right to make changes at any time without notice.

HI-TECH LINEAR COMPONENT DATA SHEET

- All collector contacts connected in parallel.
- 2) h_{FE} matching is satisfied by $1-2\left|\frac{an_{FE}(MAX)}{100\%}\right| < \frac{n_{FE}(2)}{h_{FE}(1)} < 1+2\left|\frac{an_{FE}(MAX)}{100\%}\right|$ where $h_{FE}(1)$ and $h_{FE}(2)$ are any two current gains chosen from a population of like transistors on chip.
- Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.
- 4) Matching of V_{BE} is satisfied by $\|V_{BE(2)}^{-V}\|_{BE(1)}\| < 2\|\Delta V_{BE(MAX)}\|$ where $V_{BE(1)}$ and $V_{BE(2)}$ are any two base-emitter voltages chosen from a population of like transistors on chip.
- 5) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of lpF for each bonding pad which is related to the specific junction under test.



Layout and Cross-Section of Low Noise NFN Transistor (Not to Scale)



SMALL 10MA DIODE (TRANSISTOR WITH COLLECTOR AND BASE SHORTED)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE Ta=25°C (Unless otherwise noted)

PARAMETER	SYMBOL		CONDITION		MIN	ТҮР	MAX	UNITS
		I _F =100µA	-		0.61		0.73	
Forward Voltage Drop	V _F	I _F =1mA			0.67		0.79	1 v
		I _F =10mA			0.77		0.89	
Matching of Forward Voltages	۵۷ _F	I _F =1mA	· · · · · · · · · · · · · · · · · · ·	(Note 1)		±2	±6	m۷
Temperature Coefficient of V _F	ΔV _F /ΔT	I _F =1mA				-1.8		mV/ ^O C
	_	V -20V	TA=25°C	(Note 2)		0.1		
Leakage Current	I ₀	V _R =20V	TA=125°C	(Note 2)		10		nA
Breakdown Voltage	₿V _D	I _R =10µA		-	6.25		7.25	٧
Maximum Diode Current	I _F (MAX)						20	mA
Junction Capacitance	CJ	V _D =0V		(Note 3)		1		pF

- Matching of V_F is satisfied by $\{V_{F(2)} V_{F(1)}\}$ $\{V_{F(MAX)}\}$ where $V_{F(1)}$ and 1) V_{F(2)} are any two forward voltages chosen from a population of like diodes on chip.
- Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.
- Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of lpF for each bonding pad which is related to the specific junction under test.

SMALL 10MA ZENER DIODE (EMITTER-BASE JUNCTION OF TRANSISTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE T_A =25 $^{\rm O}$ C (Unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN	ТҮР	MAX	UNITS
		I _Z =lµA	-	6.2	6.7	7.2	
		I _Z =10µA		6.25	6.75	7.25	
Breakdown Voltage	v _z	1 _Z ≐100µA	(Note 1)	6.3	6.8	7.3	٧
		I _Z =1mA	(Note 1)	6.4	6.9	7.4]
		1 _Z =10mA	(Note 1)	7	7.5	8	
Dynamic Impedance (in the Breakdown Mode)	RZ	I _Z =lmA			75		Ω
Temperature Coefficient of Breakdown Voltage	△VZ/△T	IZ*1mA			2.4		mV/ ^O C

Notes:

Base-emitter breakdown, unlike base-collector breakdown, can be damaging to the transistor particularly for long breakdown duration at high current. Under these conditions, $h_{f\bar{t}}$ degradation is inevitable; therefore, V_{z} is tested at $1\mu A$ and $10\mu A$ for each transistor. Operation at higher current has been fully characterized and is guaranteed by extrapolation. 1)

20V SCHOTTKY NPN TRANSISTOR 100ua Guard-Banded Schottky Diode

GENERAL DESCRIPTION

The Schottky NPN transistor is identical in size to the small NPN transistor on chip. It has a single N+ collector diffusion with two collector contacts in it. These contacts are used for the ohmic connection to the transistor's collector. In addition there is also a Schottky contact which is made directly to the N-type epilayer collector. This Schottky contact forms a Schottky diode which can be connected to the base of the transistor to form a Schottky clamped transistor or

can be used independently as a Schottky diode. The Schottky diode has a p-type ring in its periphery. The ring functions as a guard-band to reduce the leakage current in the diode.

FEATURES

Matched V_{BE} and h_{FE} Transistor Parameters
Matched Schottky Diode Parameters
Transistor Can be Schottky Clamped or Unclamped
TYPICAL APPLICATIONS
Non Saturating Logic Gates
High-Speed Circuitry

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE Ta=25°C'(Unless otherwise noted)

PARAMETER	SYMBOL		CONDITION	4S	MIN	TYP	MAX	UNITS
DC Current Gain	h _{FE}	I _C =3mA	V _{CE} ±5V		80		300	
Matching of DC Current Gains	Δh _{FE}	I _C =1mA	V _{CE} =5V	(Note 1)		±5	±10	%
Temperature Coefficient of h _{FE}	Δh _{FE} /ΔT	I _C =1mA		TA < 125°C		0.5		
			~ oc0c	Transistor with Clamp (Notes 2,3)		10	100	nA
Collector-Base Leakage Current	Ī	V _{CB} =20V	7 _A =25 ⁰ C	Transistor without Clamp (Notes 2,3)		0.01	0.1	na
COFFECTOR - Base Leakage Current	I _{CBO}	CB 201	0.	Transistor with Clamp (Notes 2,3)		0.1	1	μА
			T _A =125 ⁰ C	Transistor without Clamp (Notes 2,3)		1	10	nΑ
				Transistor with Clamp (Notes 2,3)		0.5	5	μА
Callacton Emitton Lookago Cumment	1	V _{CE} =20V	TA=25°C	Transistor without Clamp (Notes 2,3)		0.2	2	nA
Collector-Emitter Leakage Current	I _{CEO}	CE		Transistor with Clamp (Notes 2,3)		10	100	
			T _A =125 ⁰ C	Transistor without Clamp (Notes 2,3)		0.2	2	μА
Collector-Emitter Breakdown Voltage	LVCEO			(Note 4)	20			٧
Collector-Base Breakdown Voltage	вусво			(Note 4)	20			٧
Emitter-Base Breakdown Voltage	BV _{EBO}	1 _E =10µA			6.25		7.25	٧
Collector-Substrate Breakdown Voltage	BVCS			(Note 4)	20			٧
Base-Emitter Forward Voltage	V _{BE}	I _E = 1mA	V _{CE} =5V	•	0.67		0.79	v
Matching of Base-Emitter Forward Voltages	ΔV _{BE}	I _E =lmA	V _{CE} =5V	(Note 5)		±2	±6	πV
Temperature Coefficient of V _{BE}	ΔV _{BE} /ΔT	I _E = 1 mA	V _{CE} =5V			-1.8		mV/ ^O
Collector-Emitter Saturation	V _{CE} (SAT)	I _C =1mA	Transist	or with Clamp(Notes 3,6)		0.45	0.55	V
Voltage	CE (SAI)	(I _C /I _B)=1	0 Transist	or without Clamp (Notes 3,6)		0.2	0.3	'
Maximum Collector Current	I _C (MAX)	P _D (MAX)=2	200mW				20	πA

Information furnished by Hi-Tech Linear is believed to be accurate and reliable. However, no responsibility is assumed by HTL for its use, nor for any infringements of pattents or other rights which may result from its use. HTL reserves the right to make changes at any time without notice.

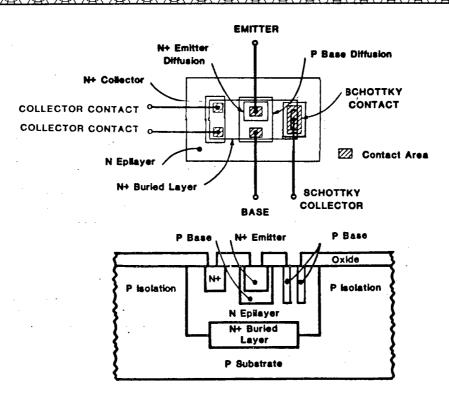
HISTECH LINEAR COMPONENT DAT

SMALL SCHOTTKY CLAMPED NPN TRANSISTOR (CONTINUED)

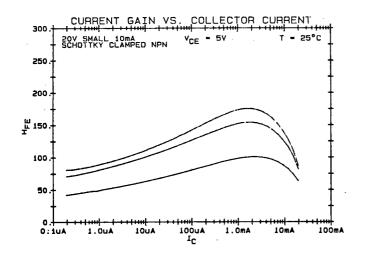
PARAMETER	SYMBOL	CONDIT	IONS	•	MIN	ТҮР	MAX	UNITS
	1.		Transist	or with Clamp		300		MHz
Cutoff Frequency	fT	IC=5mA VCE=5	Transist	or without Clamp		400		PUIZ
				Transistor with Clamp		3		
CA Time	_	$(I_C/I_B)=10 R_B=75$	1 _C =1mA	Transistor with- out Clamp		5		ns
Storage Time	¹s ·	i d'CuBiero WBeig		Transistor with Clamp		25		
	<u> </u>		I _C =10mA	Transistor with- out Clamp		80		1
Emitter-Base Capacitance	C _{EB}	V _{EB} =0V		(Note 7)		0.8		pF
		Transi	stor with	Clamp (Note 7)		1.5		pF
Collector-Base Capacitance	ССВ	V _{CB} =0V Transi	stor witho	ut Clamp(Note 7)		1		pr
Collector-Substrate Capacitance	c _{cs}	V _{CS} =0V		(Note 7)		3		pF

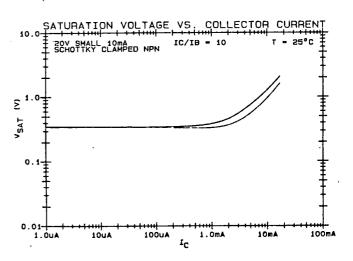
- h_{FE} matching is satisfied by $1-2 \left| \frac{h_{FE}(MAX)}{100\%} \right|$ 1) $h_{\text{FE}(1)}$ and $h_{\text{FE}(2)}$ are any two current gains chosen from a population of like transistors on chip.
- Device leakage current is specified. Mishandled packaged devices may exhibit 2) much higher leakage currents due to external surface leakage.
- In an array design, the MPN transistor can be used without the clamp, the transistor 3) and the diode can be separated.
- It is not advisable to operate Schottky transistors in the breakdown mode as 4) parameter degradation may occur.
- Matching of V_{BE} is satisfied by $|V_{BE(2)}^{-1} V_{BE(1)}| < 2|\Delta V_{BE(MAX)}|$ where $V_{BE(1)}$ 5) and $V_{BE(2)}$ are any two base-emitter voltages chosen from a population of like transistors on chip.
- The base collector Schottky clamp prevents deep saturation of the transistor. 6)
- Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of lpF for each bonding pad which is related to the specific junction 7) under test.

HI-TECH LINEAR COMPONENT DATA SHEET



Layout and Cross-Section of Small 10mA Schottky Clamped NPN Transistor (Not to Scale)



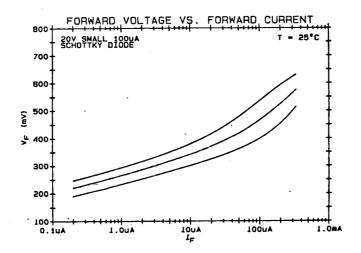


SMALL 100µA SCHOTTKY DIODE (Note 1)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE TA=25°C (Unless otherwise noted)

PARAMETER	SYMBOL		CONDITIONS		MIN	ТҮР	MAX	UNITS
		I _F =10µA			0.27		0.47	V
Forward Voltage Drop	V _F	I _F =100μA			0.42		0.62] '
Temperature Coefficient of V _F	ΔV _F /ΔT	I _F =100μA				-0.9		mV/°C
Lankana Cumant	,	V =20V	T _A =25 ⁰ C	(Note 2)		10		nΑ
Leakage Current	10	V _R =20V	T _A =125°C	(Note 2)		1		.µA
Breakdown Voltage	BVD	<u> </u>		' (Note 3)	20			٧
Maximum Usable Current	I _{F (MAX)}						0.5	mA

- In an array design, the NPN transistor can be used without the clamp, the transistor and the diode can be separated.
- Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.
- It is not advisable to operate Schottky diodes in the breakdown mode as parameter degradation may occur.



histech Linear component data sheet

20V LARGE NPN TRANSISTOR 100ma Dual Emitter

GENERAL DESCRIPTION

The large 50mA (per emitter) dual-emitter NPN transistor has two emitters in a common base region with three seperate base contacts. The collector has two seperate N+ diffusion regions with two contacts in each. Normally, all collector contacts are connected together to reduce the series collector resistance as well as the saturation voltage, unless, the collector region is used as a crossunder, or layout considerations restrict the connection of the collector contacts. Also, both emitters should be connected together unless the design calls for a dual emitter transistor, in which case each emitter is capable of

handling half of the maximum transistor current. This transistor is available in two versions, with and without a deep N+ diffusion in the collector area. The deep N+ diffusion reduces the saturation voltage and increases the current handling capability.

FEATURES

Two Seperate Emitters for Increased Emitter Area and Emitter Efficiency

Quad Collector Contacts

Three Base Contacts

TYPICAL APPLICATIONS

Motor Drivers Relay Drivers Lamp and LED Drivers Voltage Regulators Power Darlingtons

LARGE 50mA (PER EMITTER) DUAL-EMITTER NPN TRANSISTOR (EACH EMITTER)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE T_A=25.0C (Unless otherwise noted)

		Α	•					
PARAMETER	SYMBOL		CONDITION	S	MIN	ТҮР	MAX	UNIT
DC Current Gain	h _{FE}	I _C =50mA	V _{CE} =5V	(Note 1)	80		300	
Matching of DC Current Gains	۵ħ _{FE}	1 _C =50mA	V _{CE} =5V	(Note 2)		±5	±10	*
Temperature Coefficient of h _{FE}	Δh _{FE} /ΔT	I _C =50mA	-55°C < T	A < 125°C		0.5		%/
Collector-Base Leakage Current	,	V -20V	T _A =25°C	(Note 3)		0.05	0.5	
Collector-base Leakage Current	^I CBO	V _{CB} =20V	T _A =125°C	· (Note 3)		5	50	nA
Callantan Faitten Laukan Command	•	V -20V	T _A =25 ⁰ C	(Note 3)		0.5	5	nA
Collector-Emitter Leakage Current	ICEO	V _{CE} =20V	TA=125°C	(Note 3)		0.5	5	μA
Collector-Emitter Breakdown Voltage	LVCEO	I _C ≐1mA			20			٧
Collector-Base Breakdown Voltage	BA ^{CBO}	I _C =100µA		 	30			V
Emitter-Base Breakdown Voltage	BV _{EBO}	I _E =10μΑ			6.25		7.25	V
Collector-Substrate Breakdown Voltage	BV _{CS}	I _C =10µA			20			٧
			I _F =5mA	One Emitter	0.68		0.8	
Base-Emitter Forward Voltage	v	V ~6V	٠	Two Emitters Connected in Parallel	0.66		0.78] ,
sase-Emitter Forward Voltage	V _{BE}	V _{CE} =5V	I _F =50mA	One Emitter	0.8		0.92] '
		-		Two Emitters Connected in Parallel	0.74		0.86	
datching of Base-Emitter Forward Voltages	ΔV _{BE}	I _E =5mA	V _{CE} =5V	(Note 4)		±2	±6	mV
Temperature Coefficient of V _{BE}	ΔV _{BE} /ΔT	I _F =5mA	V _{CE} =5V			-1.8		mV/

Information furnished by Hi-Tech Linear is believed to be accurate and reliable. However, no responsibility is assumed by HTL for its use, nor for any infringements of pattents or other rights which may result from its use. HTL reserves the right to make changes at any time without notice.

hi etech Linear Component Data

LARGE NPN TRANSISTOR (CONTINUED)

PARAMETER	SYMBOL		CONDITIONS		MIN	ТҮР	MAX	UNITS
	·			One Collector Contact (One Diffusion Region) (Note 5)	·	0.42	0.6	
			One Emitter	Two Collector Contacts (Two Diffusion Regions) (Note 5)		0.2	0.4	
	·	I _C =5mA	. •	Four Collector Contacts (Two Diffusion Regions)		0.17	0.22	
•	-	(Ĭ _C /I _B)=10	·	One Collector Contact (One Diffusion Region) (Note 5)		0.25	0.35	
Collector-Emitter Saturation Voltage	V _{CE} (SAT)		Two Emitters Connected in Parallel	Two Collector Contacts (Two Diffusion Regions) (Note 5)		0.12	0.22	٧
				Four Collector Contacts (Two Diffusion Regions)		0.11	0.15	
				One Collector Contact (One Diffusion Region) (Note 5)		2.4		·
	-	I _C =50mA (I _C /I _B)=10	Two Emitters Connected in Parallel	Two Collector Contacts (Two Diffusion Regions) (Note 5)		1	1.4	
.3				Four Collector Contacts (Two Diffusion Regions)		0.9	1.3	
Maximum Collector Current	I _C (MAX)	PD(MAX)=50	OmW Two Emitt	ers Connected			200	mA .
Cutoff Frequency	f _T	I _C =50mA	V _{CE} =5V Two E	imitters Connected arallel (Note 1)		500		MHz
Storage Time	₹S	(I _C /I _B)=10 R _B =75Ω	Two Emitters Connected in Parallel	I _C =5mA I _C =50mA		15 120		ns
Emitter-Ba - Capacitance	- C _{EB}	V _{EB} =OV		(Note 6)		2		pF
Collector-Base Capacitance	ССВ	V _{CB} =OV		(Note 6)		3		pF
Collector-Substrate Capacitance	c _{cs}	V _{CS} =0V		(Note 6)		6		pF

Notes:

All collector contacts connected in parallel. 1)

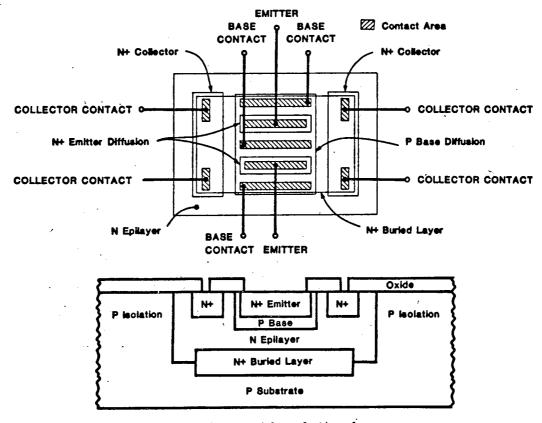
h_{FE} matching is satisfied by 2)

 $^{h}_{\text{FE(1)}}$ and $^{h}_{\text{FE(2)}}$ are any two current gains chosen from a population of like transistors on chip.

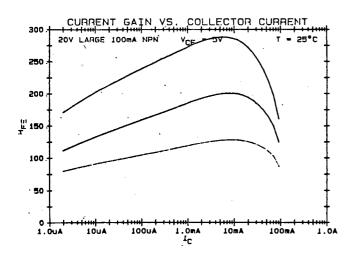
- Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.
- Matching of V_{BE} is satisfied by $|V_{BE(2)} V_{BE(1)}| < 2|\Delta V_{BE(MAX)}|$ where $V_{BE(1)}$ and VBE(2) are any two base-emitter voltages chosen from a population of like transistors on chip.

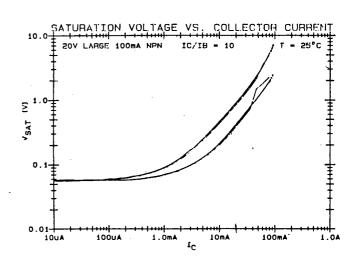
tech linear component data shee

- It is not recommended to operate the transistor in the saturation mode when only one collector contact or two collector contacts on the same N+ diffusion region are used, since a high saturation voltage is inevitable, especially at increased collector currents. 5)
- 6) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of lpF for each bonding pad which is related to the specific junction under test.



Layout and Cross-Section of Large 50mA (Per Emitter) Dual-Emitter NPN Transistor (Not to Scale)





20V LARGE NPN TRANSISTOR 200mA HEX EMITTER

GENERAL DESCRIPTION

The large 200mA NPN Transistor has a large emitter constructed with six fingers, in a double-comb shape, placed in a single base region. The base region has two base contacts in it and is serounded with a wrap-around N+ collector diffusion which also includes two collector contacts. This multiple contact structive permits a degree of flexibility in the layout process. However, best results are obtained when all collector contacts are connected together and all base contacts connected together respectively. This transistor is available in two versions, with and without a deep N+ diffusion in the collector region. The N+ diffusion reduces the saturation voltage and increases the current handling capability.

FEATURES

Six-finger Emitter Structure **Dual Base Contacts Dual Collector Contacts** TYPICAL APPLICATIONS Motor Drivers Relay Drivers Lamp and LED Drivers Voltage Regulators **Power Darlingtons**

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE T_x=25°C (Unless otherwise noted)

PARAMETEŔ	SYMBOL		CONDITIO	NS .		MIN	ТҮР	MAX	UNITS
DC Current Gain	h _{FE}	1 _C =100mA	V _{CE} =5V		(Note 1)	80		300	
Matching of DC Current Gains	Δħ _{FE}	I _C =100mA	V _{CE} =5V		(Note 2)		±5	±10	2
			-55 ⁰ C <	T _A < 25 ⁰ C			0.5		
Temperature Coefficient of h _{FE}	Δħ _{FE} /ΔΤ	I _C =100mA	25 ⁰ C < T				±0.3		%/ ⁰ (
			75 ⁰ C < T	4 < 125 ⁰ C			-0.5		<u> </u>
		V - 20V	TA=25°C		(Note 3)		0.05	0.5	nA.
Collector-Base Leakage Current	I CBO	V _{CB} =20V	T _A =125°C		(Note 3)		5	50] IIA
			TA=25°C		(Note 3)		0.5	5	nA
Collector-Emitter Leakage Current	I _{CEO}	V _{CE} =20V	T _Á =125 ⁰ C		(Note 3)		1	10	μA
Collector-Emitter Breakdown Voltage	LVCEO	I _C =1mA				20			٧
Collector-Base Breakdown Voltage	вусво	I _C =100µA	•	· .		30			٧
Emitter-Base Breakdown Voltage	BV _{EBO}	I_E=10μA	•			6.25		7.25	٧
Collector-Substrate Breakdown Voltage	BVCS	1 _C =10μA				20			٧
			I _E =10m/	4		0.65		0.77	V
Base-Emitter Forward Voltage	V _{BE}	V _{CE} =5V	I _E = 100r	πA		0.73		0.85] "
Matching of Base-Emitter Forward Voltages	ΔVBE	I _E = 10mA	V _{CE} =5V		(Note 4)		±2	±6	mV
Temperature Coefficient of V _{RF}	ΔV _{BE} /ΔT	!I _E	V _{CE} =5V				-1.8		my/º
				One Collector			0.16	0.24	
			I _C =10mA	Two Collector (One Diffusion	Contacts		0.12	0.17	1
Collector-Emitter Saturation Voltage	V _{CE} (SAT)	(I _C /I _B)=10		One Collector (One Diffusion	Contact		1.4	2	7 "
			I _C =100mA	Two Collector (One Diffusion	Contacts		0.9	1.2	
Maximum Collector Current	I _{C(MAX)}	P _{D(MAX)} =70	OmW					300	mА
Cutoff Frequency	f _T	I _C =50mA	V _{CE} =5V	· · · · · · · · · · · · · · · · · · ·		·	500		MHz

Information furnished by HI-Tech Linear is believed to be accurate and reliable. However, no responsibility is assumed by HTL for its use, nor for any infringements of pattents or other rights which may result from its use. HTL reserves the right to make changes at any time without notice.

ECH LINEAR SCOMPONENT DATAS SHEETS

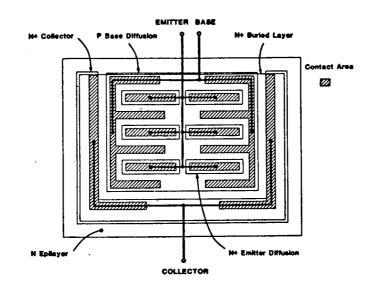
LARGE NPN TRANSISTOR (CONTINUED)

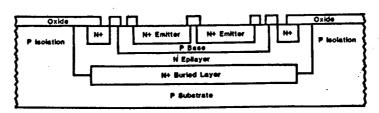
PARAMETER	SYMBOL	CI	OITIDMO	NS		:	MIN	ТҮР	MAX	UNITS
		/ / / / / / /	0 75-	I _C =10mA	, ·	-		30		
Storage Time	¹s s	(I _C /I _B)=10	KB=/51	I _C =100mA				150		ns
Emitter-Base Capacitance	CEB	V _{EB} *0V			(Note	5)		13.5		pF
Collector-Base Capacitance	ССВ	V _{CB} =0V	.,		(Note	5)		9		рF
Collector-Substrate Capacitance	c _{ćs}	V _{CS} =0V			(Note	5)		16.5		pF

Notes:

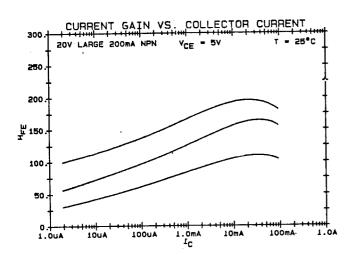
All collector contacts connected in parallel.

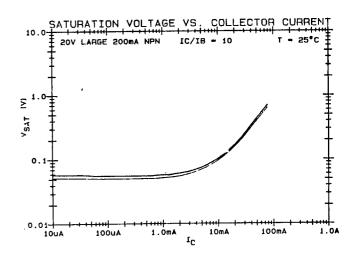
- $1-2\left|\frac{^{\Delta h}FE\,(MAX)}{100\%}\right| < \frac{^{h}FE\,(2)}{^{h}FE\,(1)} < 1+2\left|\frac{^{\Delta h}FE\,(MAX)}{100\%}\right| \text{ where}$ h_{FE} matching is satisfied by 2) $h_{\text{FE}(1)}$ and $h_{\text{FE}(2)}$ are any two current gains chosen from a population of like transistors on chip.
- Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.
- Matching of V_{BE} is satisfied by $\|V_{BE(2)}^{-V}\|_{BE(1)}\| < 2\|\Delta V_{BE(MAX)}\|$ where $V_{BE(1)}$ and $V_{BE(2)}$ are any two mase-emitter voltages chosen from a population of like transistors on chip.
- Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.





Layout and Cross-Section of Large 200mA NPN Transistor (Not to Scale)





20V LATERAL PNP TRANSISTOR 1mA QUAD COLLECTOR

GENERAL DESCRIPTION

The lateral PNP transistor has an oval-shaped, P-type emitter, surrounded by four P-type collector diffusions in a single epi base region. The base is made with an N+ diffusion with two base contacts in it. All four collectors should be connected together when a single collector transistor is required. When current ratios are important, such as for multiple current sources, the collectors can be used individually. Unused collectors must be connected to the substrate or any other potential that will ensure that the transistor does not saturate.

FEATURES

Quad Collectors Matched $v_{\mbox{\footnotesize{BE}}}$ and $h_{\mbox{\footnotesize{FE}}}$ Transistor Parameters TYPICAL APPLICATIONS **Current Sources Active Loads** Level Shifters Biasing Stages **Amplifiers**

O.25mA (PER COLLECTOR) QUAD-COLLECTOR LATERAL PNP TRANSISTOR (EACH COLLECTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE TA=25°C (Unless otherwise noted)

PARAMETER	SYMBOL	1	CONDITIONS -		MIN	ТҮР	MAX	UNITS
FARANCIER	311000		T CONDITIONS		FILM	111	FIAA	01113
			I _C =-25μA	One Collector (Note 1)	5		37.5	
DC Current Gain	h _{FE}	V _{CE} =-5V	Ic(TOTAL)*-50µA	Two Collectors Connected in Parallel (Note 1)	10		75	
			I _{C(TOTAL)} =-100µA	Four Collectors Connected in Parallel	20	-	150	
Matching of DC Current Gains	۵h _{FE}	1 _C =-100µA	V _{CE} =-5V	(Note 2)		±5	±15	*
Temperature Coefficient of h _{FE}	Δh _{FE} /ΔT	I _C =-100μA	-55°C < T _A < 125	°c		-0.1		1/°C
Collector-Base Leakage Current	1 =	V _{CB} =-20V	TA=25°C	(Note 3)		-0.01	-0.1	nA
	I CBO	CB204	TA=125°C	(Note 3)		-1	-10	110
Collector-Emitter Leakage Current		V _{CE} =-20V	TA=25°C	(Note 3)		-0.05	-0.5	nA
Corrector - Emitter Leakage Current	ICEO	CE	TA=125°C	(Note 3)		-25	-250	''^
Collector-Emitter Breakdown Voltage	BVCEO	I _C =-100μA			-20			٧
Collector-Base Breakdown Voltage	вусво	1 _C =-100μA			-30			٧
Emitter-Base Breakdown Voltage	BV _{EBO}	1 _E =-100μA			-30			٧
Base-Substrate Breakdown Voltage	BVBS	I _B =10μA			20			٧
Base-Emitter Forward Voltage	V _{BE}	1 _E =100μA	V _{CE} =-5V		-0.61		-0.73	٧
Matching of Base-Emitter Forward Voltages	ΔV _{BE}	1 _E =100µA	V _{CE} =-5V	(Note 4)		±2	±6	mV
Temperature Coefficient of V _{BE}	ΔV _{BE} /ΔT	I _E =100µA	V _{CE} =-5V			1.8		mV/ ^O C

Information furnished by Hi-Tech Linear is believed to be accurate and reliable. However, no responsibility is assumed by HTL for its use, nor for any infringements of pattents or other rights which may result from its use. HTL reserves the right to make changes at any time without notice.

QUAD-COLLECTOR LATERAL PNP TRANSISTOR (CONTINUED)

PARAMETER	SYMBOL	CONDITION	S	MIN	ТҮР	MAX	UNITS
Collector-Emitter Saturation Voltage	V _{CE} (SAT)	(I _{C(TOTAL)} /I _B)=1	I _C =-25µA One Collector (Notes 1,5) I _C (TOTAL) =-50µA Two Collectors Connected in Parallel (Notes 1,5) I _C (TOTAL) =-100µA Four Collectors Connected in Parallel (Note 5)		-0.1	-0.18	٧
Maximum Usable Collector Current	I _{C(MAX)}	(Per Collector)				-0,5	mA
Cutoff Frequency	f _T	1 _{C(TOTAL)} =-100µA V _C	Four Collectors E=-5V Connected in Parallel		5		MHz
		(I _{C(TOTAL)} /I _B)=1	I _C (TOTAL)=-100µA Four Collectors Connected in Parallel		75		
Storage Time	[*] S	R _B ≖750Ω	IC(TOTAL)=-lmA Four Collectors Connected in Parallel		130		ns
Emitter-Base Capacitance	CEB	V _{EB} =OV	(Note 6)		0.2		pF
Collector-Base Capacitance	ССВ	V _{CB} =OV	(Note 6)		0.4		pF
Base-Substrate Capacitance	c _{BS}	V _{BS} =0V	(Note 6)		3.5		pF

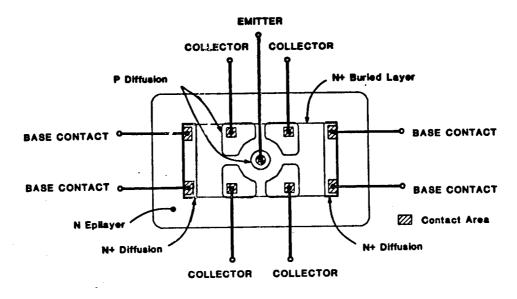
Notes:

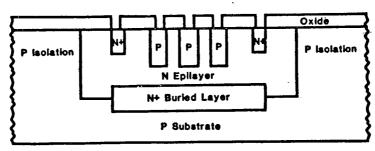
1) With the other collectors grounded.

 h_{FE} matching is satisfied by $1-2\left|\frac{\Delta h_{FE}(MAX)}{100\%}\right| < \frac{h_{FE}(2)}{h_{FE}(1)} < 1+2\left|\frac{\Delta h_{FE}(MAX)}{100\%}\right|$ where $\mathbf{h}_{\mathsf{FE}(1)}$ and $\mathbf{h}_{\mathsf{FE}(2)}$ are any two current gains chosen from a population of like transistors on chip.

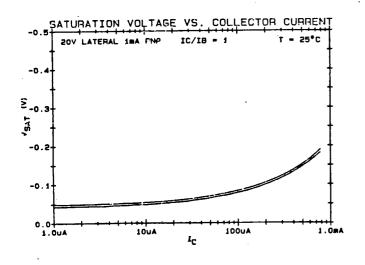
- Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.
- Matching of V_{BE} is satisfied by $\|V_{BE(2)} V_{BE(1)}\| \le 2\|\Delta V_{BE(MAX)}\|$ where $V_{BE(1)}$ and $V_{BE(2)}$ are any two base-emitter voltages chosen from a population of like transistors on chip.
- It is not advisable to operate the lateral PNP transistor in the saturation mode since the parasitic vertical substrate transistor (related to the lateral transistor) becomes heavily active.
- Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of lpF for each bonding pad which is related to the specific junction under test.

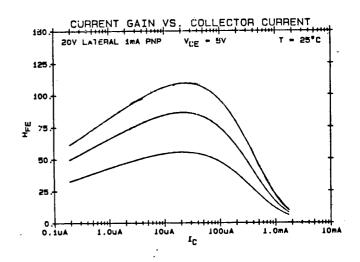
ECH LINEAR COMPONENT DATA SHEE





Layout and Cross-Section of O.25mA (Per Collector) Quad-Collector Lateral PNP Transistor (Not to Scale)





LATERAL PHP DIODE (EMITTER-BASE JUNCTION OF TRANSISTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE T_A =25 $^{\rm O}$ C (Unless otherwise noted)

PARAMETER	SYMBOL		CONDITIONS		MIN	TYP	MAX	UNITS
		I _F =100µA			0.61		0.73	
Forward Voltage Drop	٧ _F	I _F =]mA			0.73		0.85	٧
		I _F =10mA		(Note 1)		1.1		
Matching of Forward Voltages	ΔVF	I _F =1mA		(Note 2)		±2	±6	m∀
Temperature Coefficient of V _F	ΔV _F /ΔΤ	I _F =1mA				-1.8		mV/°C
			T _A =25 ⁰ C	(Note 3)		0.1		
Leakage Current	10	V _R *20V	TA=125°C	(Note 3)		10		nA
Breakdown Voltage	BVD	I _R =100µA			30			٧
Maximum Diode Current	I _{F(MAX)}			(Note 1)			10	mA
Junction Capacitance	c _J	V _D =OV		(Note 4)		0.2		pF

- The lateral PNP diode, like the lateral PNP transistor, has a parasitic vertical substrate current that becomes dominant at high operating current. This substrate loss current becomes comparable to the diode forward current at about 5mA. 1)
- Matching of V_F is satisfied by $\|V_{F(2)} V_{F(1)}\| \le 2\|\Delta V_{F(MAX)}\|$ where $V_{F(1)}$ and $V_{F(2)}$ are any two forward voltages chosen from a population of like diodes on 2)
- Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.
- Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of lpF for each bonding pad which is related to the specific junction under test.

hy tech linear component data shee

20V DUAL LATERAL PNP TRANSISTOR 1ma Quad Collector

GENERAL DESCRIPTION

The lateral PNP transistor has an oval shaped, p-type emitter surrounded by four P-type collector diffusions in a single epi base region. The two transistors are located in a common isolation tub and share the same base region. The base is made with an N + diffusion with two base contacts in it. All four collectors should be connected together when a single collector transistor is required. When current ratios are important, such as for multiple current sources, the collectors can be connected individually.

Unused collectors must be connected to the substrate or any other potential that will ensure that the transistor does not saturate.

FEATURES

Quad Collectors
Matched VBE and hFE Transistor Parameters

TYPICAL APPLICATIONS

Current Sources Active Loads Level Shifters Biasing Stages Amplifiers

0.25mA (PER COLLECTOR) QUAD-COLLECTUR LATERAL PNP TRANSISTOR (EACH COLLECTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE TA=25°C (Unless otherwise noted)

PARAMETER	SYMBOL		CONDITIONS		MIN	TYP	MAX	UN TS
			I _C =-25 µA	One Collector (Note 1)	5		37.5	
DC Current Gain	h _{FE}	V _{CE} =-5V	^I C(TOTAL)=-50μA	Two Collectors Connected in Parallel (Note 1)	10		75	
	:		IC(TOTAL)=-100µA	Four Collectors Connected in Parallel	20		150	
Matching of DC Current Gains	^{Δh} FE	1 _C =-100μA	V _{CE} =-5V	(Note 2)		±5	±15	*
Temperature Coefficient of h _{FE}	Δh _{FE} /ΔT	I _C =-100μA	-55°C < T _A < 125	°C		-0,1		%/ ⁰ C
	•	V _{CB} =-20V	TA=25°C	(Note 3)		-0,01	-0.1	nA
Collector-Base Leakage Current	^I сво	VCB=-20V	TA=125°C	(Note 3)		-1	-10	
		V - 20V	T _A =25°C T _A =125°C	(Note 3)		-0.05	-0.5	nA
Collector-Emitter Leakage Current	ICEO	VCE=-20V	TA=125°C	(Note 3)		-25	-250	
Collector-Emitter Breakdown Voltage	BVCEO	I _C =-100µA	<u> </u>		-20			٧
Collector-Base Breakdown Voltage	вусво	I _C =-100μA			-30			¥
Emitter-Base Breakdown Voltage	BV _{EBO}	I _E =-100μA		`	-30			Y
Base-Substrate Breakdown Voltage	BVBS	IB=JOhV			20			٧
Base-Emitter Forward Voltage	VBE	I _E =100µA	V _{CE} =-5V		-0.61	,	-0.73	٧
Matching of Base-Emitter Forward Voltages	ΔV _{BE}	I _E =100µA	V _{CE} =-5V	(Note 4)		±2	±6	m۷
Temperature Coefficient of V _{BE}	ΔV _{BE} /ΔT	I _E =100µA	V _{CE} =-5V		<u> </u>	1.8	<u> </u>	mV/ ^O C

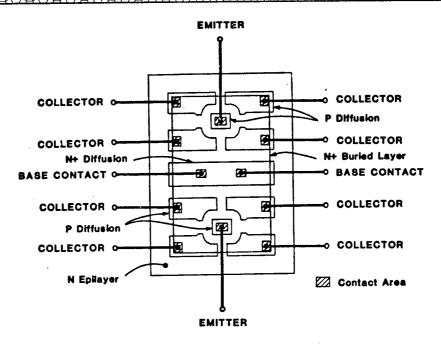
Information furnished by HI-Tech Linear is believed to be accurate and reliable. However, no responsibility is assumed by HTL for its use, nor for any infringements of patients or other rights which may result from its use. HTL reserves the right to make changes at any time without notice.

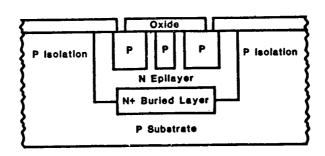
HI TECH LINEAR COMPONENT DATA SHEET

QUAD-COLLECTOR LATERAL PNP TRANSISTOR (CONTINUED)

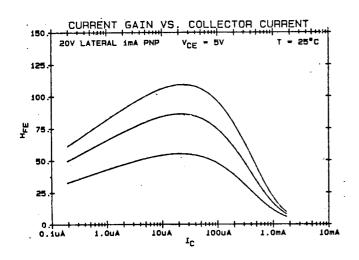
PARAMETER	SYMBOL	CONDITIONS		MIN	ТҮР	MAX	UNITS
Collector-Emitter Saturation Voltage	V _{CE} (SAT)	^{{I} C(TOTAL)/ ^I B ⁾⁼ 1	I _C =-25µA One Collector (Notes 1,5) I _C (TOTAL)=-50µA Two Collectors Connected in Parallel (Notes 1,5) I _C (TOTAL)=-100µA Four Collectors Connected in Parallel (Note 5)		-0.1	-0.18	y
Maximum Usable Collector Current	I _C (MAX)	(Per Collector)				-0.5	πA
Cutoff Frequency	f _T	¹ C(TOTAL) ^{=-100μA} V _{CE} ⁼⁻⁵	Four Collectors V Connected in Parallel		5		MHz
Channe Time		(I _{C(TOTAL)} /I _B)=1	I _C (TOTAL)=-100µA Four Collectors Connected in Parallel		75		
Storage Time	^τ S	R _B =750Ω	I _{C(TOTAL)} =-1mA Four Collectors Connected in Parallel		130	_	ns
Emitter-Base Capacitance	c _{EB}	V _{EB} =OV	(Note 6)		0.2		pF
Collector-Base Capacitance	ССВ	V _{CB} =OV	(Note 6)		0.4		pF
Base-Substrate Capacitance	C _{BS}	V _{BS} =0V	(Notes 6,7)		3.5		pF

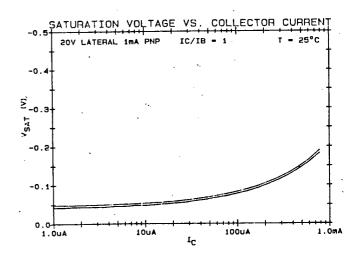
- 1) With the other collectors grounded.
- 2) h_{FE} matching is satisfied by $1-2\left|\frac{\Delta h_{FE}(MAX)}{100\%}\right| < \frac{h_{FE}(2)}{h_{FE}(1)} < 1+2\left|\frac{\Delta h_{FE}(MAX)}{100\%}\right|$ where $h_{FE}(1)$ and $h_{FE}(2)$ are any two current gains chosen from a population of like transistors on chip.
- Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.
- 4) Matching of V_{BE} is satisfied by $\|V_{BE(2)} V_{BE(1)}\| < 2\|\Delta V_{BE(MAX)}\|$ where $V_{BE(1)}$ and $V_{BE(2)}$ are any two base-emitter voltages chosen from a population of like transistors on chip.
- 5) It is not advisable to operate the lateral PNP transistor in the saturation mode since the parasitic vertical substrate transistor (related to the lateral transistor) becomes heavily active.
- 6) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of lpF for each bonding pad which is related to the specific junction under test.
- 7) On the HTL-I20L chip, two quad-collector lateral PNP transistors are placed in one isolation bucket. The total base-substrate capacitance must be considered even when only one of the transistors is being used.





Layout and Cross-Section of 9.25mA (Per Collector) Quad-Collector Lateral PNP Transistor (Not to Scale)





DE 8368602 0001756 7 7-42-21

LATERAL PNP DIODE (EMITTER-BASE JUNCTION OF TRANSISTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A=25^{\circ}C$ (Unless otherwise noted)

PARAMETER	SYMBOL		CONDITIONS		MIN	TYP	MAX	UNITS
		I _E =100µA			0.61		0.73	
Forward Voltage Drop	V _F	I _F =]mA			0.73		0.85	٧
		I _F =10mA		(Note 1)		1.1		
Matching of Forward Voltages	ΔV _F	I _F =1mA		(Note 2)		±2	±6	mV
Temperature Coefficient of V _F	ΔV _F /ΔT	I _F =1mA				-1.8		mV/ ^O C
-			T _A =25°C	(Note 3)		0.1		nA
Leakage Current	I ₀	V _Ř =20V	T _A =125°C	(Note 3)		10		110
Breakdown Voltage	BVD	I _R =100μA			30			٧
Maximum Diode Current	I _F (MAX)			(Note 1)			10	mA
Junction Capacitance	CJ	V _D =0V		(Note 4)		0.2		pF

- The lateral PNP diode, like the lateral PNP transistor, has a parasitic vertical substrate current that becomes dominant at high operating current. This substrate loss current becomes comparable to the diode forward current at about
- Matching of V_F is satisfied by $\|V_{F(2)} V_{F(1)}\| < 2\|\Delta V_{F(MAX)}\|$ where $V_{F(1)}$ and $V_{F(2)}$ are any two forward voltages chosen from a population of like diodes on 2) chip.
- Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage. 3)
- Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.

20V P-TYPE DIFFUSED RESISTORS

200Ω, **450**Ω, **900**Ω, **1.8**ΚΩ, **3.6**ΚΩ

GENERAL DESCRIPTION

The P-type diffused resistors are made during the base diffusion step in the integrated circuit process. They exhibit excellent ratio matching properties which are primerily dependent on the masking accuracy in the fabrication process. However, the obsolute values are not as accurate as they are directly related to the tolerances in the diffusion process.

FEATURES
Matched Resistor Ratios
TYPICAL APPLICATIONS
Analog and Digital Circuitry

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A = 25^{\circ}C$ (Unless otherwise noted)

PARAMETER	SYMBOL		CONDITIONS		MIN	ТҮР	MAX	UNITS
Absolute Values 200n 450n 900n 1.8Kn 3.6Kn	R	V _R =5V			337.5 675 1350 2700	200 450 900 1800 3600	250 562.5 1125 2250 4500	Ω
Epi (Vcc Terminal)- Substrate Breakdown Voltage	BV _{NS}	I _N =10µA			20			V
Epi (Vcc Terminal)- Resistor Breakdown Voltage	^{BŲ} NR	I _N =100µA			30			٧
Resistor-Substrate Breakdown Voltage	BVRS	I _R =10μA			20			V
Temperature Coefficient of R	ΔR/ΔT	V _R =5V	-55°C < T _A < -25°C -25°C < T _A < 25°C 25°C < T _A < 125°C			0.06 0.13		%/°c
Matching of Equal Design Value Resistors	ΔR(1:1)	V _R =5V	^R 2 ^{=R} 1	(Notes 1,2)			±3	2
Ratio Matching of Unequal Design Value Resistors	ΔR(1:2) ΔR(1:4) ΔR(1:8)	v _R =5V	R ₂ =2R ₁ R ₂ =4R ₁ R ₂ =8R ₁	(Notes 1,2) (Notes 1,2) (Notes 1,2)			±4 ±5 ±6	%
Maximum Power Dissipation	P _{D(MAX)}						300	mW
Epi (Vcc Terminal)- Resistor Capacitance 200α 450α 900α 1.8Κα 3.6Κα	C _{NR}	V _{NR} ≖0V		(Notes 3,4)		1.1 0.5 0.6 0.9		pF

Information furnished by Hi-Tech Linear is believed to be accurate and reliable. However, no responsibility is assumed by HTL for its use, nor for any infringements of pattents or other rights which may result from its use. HTL reserves the right to make changes at any time without notice.

DE 8368602 0001758 0 D T-42-21 hi tech linear conronent data

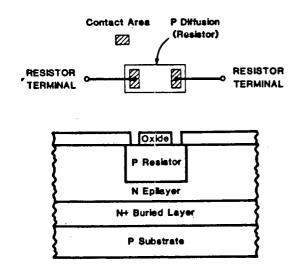
Notes:

1) Resistor ratio matching is satisfied by

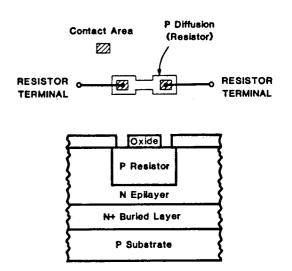
$$k \left(1-2\left|\frac{\Delta R\left(MAX\right)}{100\%}\right|\right) < \frac{R_2}{R_1} < k \left(1+2\left|\frac{\Delta R\left(MAX\right)}{100\%}\right|\right)$$

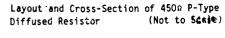
where k is the resistor ratio of the nominal values, and $\rm R_1$ and $\rm R_2$ are any two resistors chosen from these populations on chip.

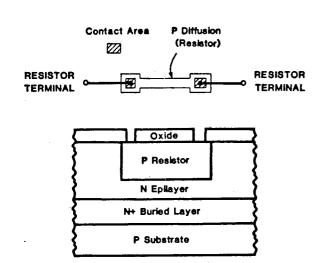
- These particular matching parameters apply to the various resistor ratios on chip. 2)
- Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test. 3)
- These capacitances refer to each individual resistor; however, most resistors on chip are strung together, thus presenting a higher total capacitance for each 4) resistor group.



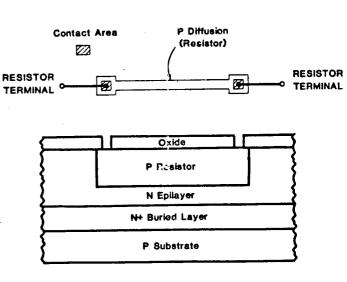
Layout and Cross-Section of 2000 P-Type Diffused Resistor (Not to Scale)





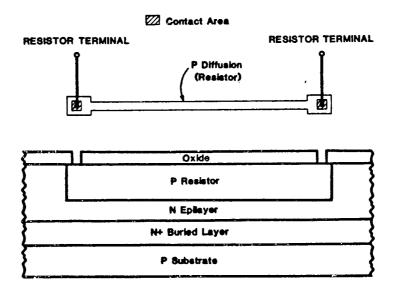


Layout and Cross-Section of 900n P-Type Diffused Resistor (Not to Scale)

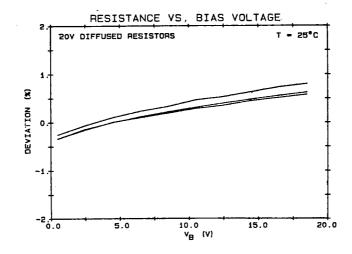


yout and Cross-Section of 1.8Km P-Type Diffused Resistor (Not to Scale)

TECH LINEAR COMPONENT DATA SHEET



Layout and Cross-Section of 3.6Kn P-Type (Not to Scale) Diffused Resistor



20V BASE PINCH RESISTORS

 $30K\Omega$, $100K\Omega$

GENERAL DESCRIPTION

The base pinch resistors have an N+ gate diffusion that overlaps the P diffusion which forms the resistor body. In most cases the gate is internally connected to one of the resistor terminals. This terminal is normally designed and layed out as the most positive node of the resistor. The layout sheets indicate this terminal with a "+" sign. The voltage drop across the resistor should not exceed 6V to prevent breakdown. Pinch resistors can be connected in series when a higher operating voltage is desired,

providing that each of the resistor does not sustain more than 6V. On some chips, the $30 \mathrm{K}\Omega$ and the $100 \mathrm{K}\Omega$ resistors are located in a single isolation tub and share a common gate connection. Each of these resistor can also sustain 6V before breakdown occures. It should be noted that the pinch resistors are non-linear and have a very strong voltage dependency.

FEATURES

High Resistor Values

TYPICAL APPLICATIONS

Current Sources

General Purpose Circuitry

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_a=25^{\circ}C$ (Unless otherwise noted)

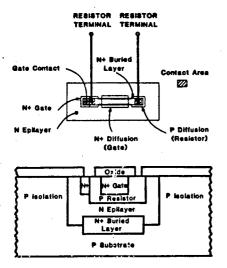
PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	мах	UNITS
Absolute Values 30Kn 100Kn	R	I _R =10µA	15 5 0	30 100	60 200	ĶΩ
Matching of Resistor Values	ΔR	I _R =10µA (Note 1)		±5		1
Breakdown Voltage	8V _R	I _R =0.5πA (For 30KΩ Resistor)	6			v
(Across Resistor Terminals)	ĸ	I _R =0.15mA (For 100KΩ Resistor)	6			•
Resistor-Substrate Breakdown Voltage	BV _{RS}	I _R =10μA	20			Á
Temperature Coefficient of R	ΔR/ΔΤ	-55°C < T _A < 125°C		0.5		%/ ⁰ C
Maximum Power Dissipation	P _{D(MAX)}				200	яW
Resistor-Substrate Capacitance 30Kn 100Kn	c _{RS}	V _{RS} =0V (Notes 2,3)		2.6 6.8		pF

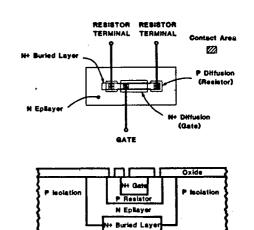
Notes:

- 1) Resistor matching is satisfied by $1-2\left|\frac{\Delta R_{(MAX)}}{100\%}\right| < \frac{R_2}{R_1} < 1+2\left|\frac{\Delta R_{(MAX)}}{100\%}\right|$ where R_1 and R_2 are any two resistors chosen from a population of the same nominal value on chip.
- 2) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of lpF for each bonding pad which is related to the specific junction
- 3) On the MCE-A20A chip, these two base pinch resistors are connected in series so that the total capacitance must be considered even when only one of the resistors is being used.

Information furnished by HI-Tech Linear is believed to be accurate and reliable. However, no responsibility is assumed by HTL for its use, nor for any infringements of pattents or other rights which may result from its use. HTL reserves the right to make changes at any time without notice.

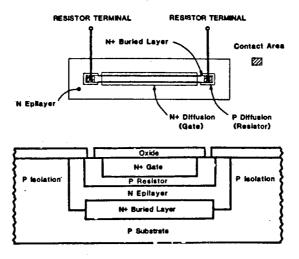
SOLITRON DEVICES INC 61 DE 8368602 0001761 0 T-42-21



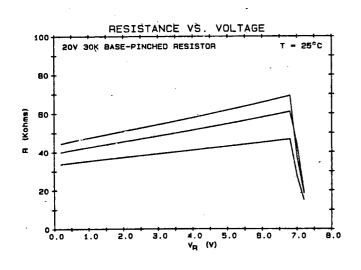


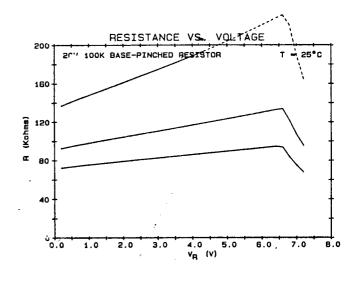
P Substrate

Layout and Cross-Section of 30Kn Base Pinch Resistor (Not to Scale)



Layout and Cross-Section of 100Km Bas.: Pinch Resistor (Not to Scale)





HISTECH LINEAR COMPONENT DATA

20V BASE PINCH RESISTORS

DUAL 60KΩ

GENERAL DESCRIPTION

The base pinch resistors have an N+ gate diffusion that overlaps the P diffusion which forms the resistor body. Both resistors are located in a single isolation tub and share a single N+ gate diffusion which has two gate contacts in it. The two resistors can be connected in series or in parallel and one of the gate contacts must be connected to the most positive node of the resistor combination. The voltage drop accross the resistor combination must never be greater than 6V to prevent breakdown. It is also possible to utilize only one of the resistors while the other resistor is left open. Since the N+ gate diffusion has two contacts in it, it can be used as a low resistance crossunder. It should be noted that the pinch resistors are nonlinear and have a very strong voltage dependency. **FEATURES**

High Resistor Values TYPICAL APPLICATIONS **Current Sources General Purpose Circuitry**

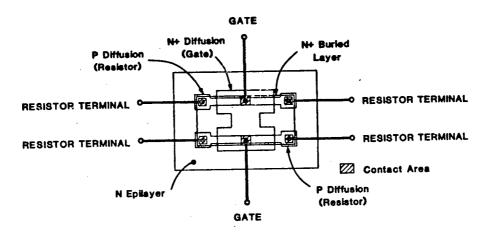
ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_a=25^{\circ}C$ (Unless otherwise noted)

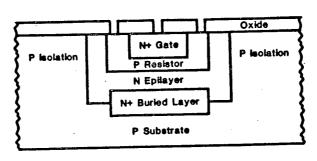
PARAMETER	SYMBQL	CONDITIO	NS ·	MIN	TYP	MAX	UNITS
Absolute Value	R	I _R ≈10µA		30	60	120	KΩ
Matching of Resistor Values	ΔR	I _R =10µA	(Note 1)		±5		%
Breakdown Voltage (Across Resistor Terminals)	^{BV} R	I _R =0.3mA		6			٧ .
Resistor-Substrate Breakdown Voltage	BV _{RS}	1 _R =10µA		20	İ		٧
Temperature Coefficient of R	ΔR/ΔT	-55°C < T _A < 125°C			0.5		%/ ⁰ 0
Maximum Power Dissipation	P _{D(MAX)}					200	mW.
Resistor Gate Capacitance	C _{RG}	V _{RG} =0V	(Notes 2,3)		1		pF
Resistor-Substrate Capacitance	C _{RS}	V _{RS} =0V	(Notes 2,4)		2.6		рF

Notes:

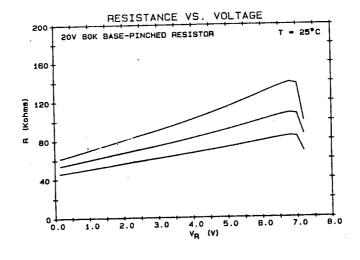
- $1-2\Big|\frac{\Delta R\left(\text{MAX}\right)}{100\%}\Big| \; < \frac{R_2}{R_1} \; < \; 1+2\Big|\frac{\Delta R\left(\text{MAX}\right)}{100\%}\Big| \; \; \text{where} \; \; R_1$ 1) and ${\bf R}_2$ are any two resistors chosen from a population of the same nominal value on chip.
- Junction capacitance is specified. An average capacitance of 0.5pF must be 2) added to include the effect of the package. Also included must be a capacitance of lpF for each bonding pad which is related to the specific junction, under test under test.
- $\mathbf{C}_{\mbox{RG}}$ is applicable only when the gate is not connected to one of the resistor
- $\mathbf{C}_{\mathbf{RS}}$ is applicable only when the gate is connected to one of the resistor terminals.

Information furnished by HI-Tech Linear is believed to be accurate and reliable. However, no responsibility is assumed by HTL for its use, nor for any infringements of pattents or other rights which may result from its use. HTL reserves the right to make changes at any time without notice.





Layout and Cross-Section of $60 \mbox{K} \mbox{\Omega}$ Base Pinch Resistor (Not to Scale)



20V N+ CROSSUNDER

TECH LINEAR

15Ω RESISTANCE

GENERAL DESCRIPTION

The 15Ω crossunder is made during the emitter diffusion step of the process. It exhibits a low sheet resistance and is primarily designed to be used as a crossunder connection to aid in the layout process. When layout permits, it is recommended to minimize the number of crossunders used to avoid possible performance degredation. Also, it is recommended not to run metal over the crossunder when metal is connected directly to a bonding pad, to prevent possible breakdown of the thin oxide layer over the crossunder.

FEATURES Low Crossunder Resistance TYPICAL APPLICATIONS

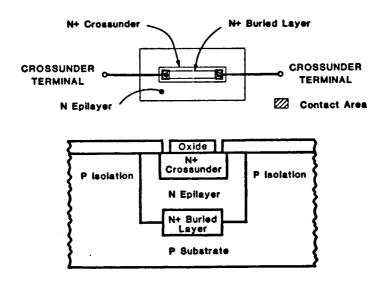
Crossunder Interconnections Low Value Resistors

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A=25^{\circ}C$ (Unless otherwise noted)

	PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
	Absolute Values	R	v _R =5v		11.25	15	18.75	ន
	Crossunder-Substrate Breakdown Voltage	BV _{RS}	I _R =10µA		20			٧
Ī	Maximum Crossunder Current	I _{R(MAX)}	·		<u></u>		40	mA
l	Crossunder-Substrate Capacitance	C _{RS} .	V _{RS} =0V	(Note 1)		1		pF

Notes:

1) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of lpF for each bonding pad which is related to the specific junction under test.



Layout and Cross-Section of 150 N+ Crossunder (Not to Scale)

Information furnished by HI-Tech Linear is believed to be accurate and reliable. However, no responsibility is assumed by HTL for its use, nor for any infringements of pattents or other rights which may result from its use. HTL reserves the right to make changes at any time without notice.

40V SMALL NPN TRANSISTOR 10ma QUAD COLLECTOR CONTACT

GENERAL DESCRIPTION

The small 10mA NPN transistor has two N+ diffusion regions in the collector area with two collector contacts in each of these diffusions. The contacts are normally connected together to reduce the series collector resistance as well as the saturation voltage. The small NPN transistor is available in two versions, with and without a deep N+ diffusion in the collector region. The deep N+ diffusion allows for an additional increase in the operating current.

FEATURES

Four Collector Contacts

Matched V_{BE} and h_{FE} Transistor Parameters

TYPICAL, APPLICATIONS

Amplifiers

Comparators

Current Sources

Bias Circuits

Level Shifters

Emitter Followers

Diode Connected Transistors

Zener Diode Connections

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A=25^{\circ}C$ (Unless otherwise noted)

PARAMETER	SYMBOL		CONDITIONS		MIN	ТҮР	MAX	UNITS
DC Current Gain	h _{FE}	I _C =1mA	V _{CE} =5V	(Note 1)	80		500	
Matching of DC Current Gains	Δh _{FE}	I _C =1mA	V _{CE} =5V	(Note 2)		±5	±10	%
Temperature Coefficient of h _{FE}	Δh _{FE} /ΔT	Ic=1mA	-55°C < TA < 125°C			0.5		%/°
		. 404	TA=25°C	(Note 3)		0.02	0.2	nA
Collector-Base Leakage Current	I _{CBO}	V _{CB} =40V	T _A =125°C	(Note 3)		1	10	I TA
			T _A =25 ⁰ C	(Note 3)		0.5	5	nΑ
Collector-Emitter Leakage Current	I _{CEO}	V _{CE} =40V	TA=125°C	(Note 3)		0.5	5	μА
Collector-Emitter Breakdown Voltage	LVCEO	I _C =1mA			40			٧
Collector-Base Breakdown Voltage	вусво	I _C =100μA			60			٧
Emitter-Base Breakdown Voltage	BV _{EBO}	I _E =10μA			6.25		7.25	٧
Collector-Substrate Breakdown Voltage	BV _{CS}	I _C =10μA			40			٧
Base-Emitter Forward Voltage	V _{BE}	I _E = 1 mA	V _{CE} =5V		0.67		0.79	V
Matching of Base-Emitter Forward Voltages	ΔVBE	I _E .[=1mA	V _{CE} =5V	(Note 4)		±2	±6	m۷
Temperature Coefficient of V _{BF}	ΔV _{BE} /ΔT	I _E =1mA	V _{CE} =5V			-1.8		mV/ ^C
			One Collector Contact (One Diffusion Region)	(Note 5)		0.2	0.3	
Collector-Emitter Saturation Voltage	V _{CE} (SAT)	IC=JWA	Two Collector Contacts (Two Diffusion Regions) (Note 5)		0.17	0.25] v
	32(3.11)	(I _C /I _B)=10	Four Collector Contact	S		0.15	0.2	
Maximum Collector Current	I _{C(MAX)}	P _{D(MAX)} =30	OmW				20	mΑ
Cutoff Frequency	f _T	I _C =5mA	V _{CE} =5V			400		MHz

information furnished by Hi-Tech Linear is believed to be accurate and reliable. However, no responsibility is assumed by HTL for its use, nor for any infringements of pattents or other rights which may result from its use. HTL reserves the right to make changes at any time without notice.

SMALL NPN TRANSISTOR (CONTINUED)

PARAMETER	SYMBOL	CONDITIONS	CONDITIONS			MAX	UNITS
Storage Time		(1 (1)-10 D -7500	I _C =1mA		7		ns
	[™] S	(I _C /I _B)=10 R _B =750Ω	I _C =10mA	12	120		113
Emitter-Base Capacitance	c _{EB}	V _{EB} =OV	(Note 6)		1.1		pF
Collector-Base Capacitance	ССВ	V _{CB} =0V	(Note 6)		1.5		pF
Collector-Substrate Capacitance	c _{cs}	V _{CS} ±0V	(Note 6)		3		pF

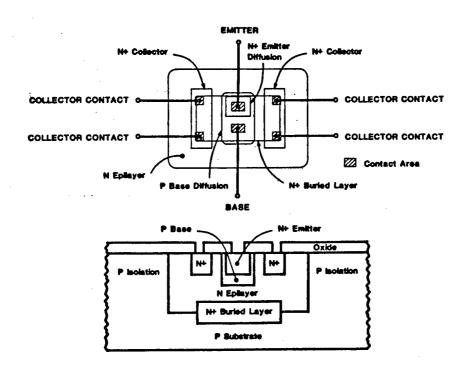
Notes:

All collector contacts connected in parallel. 1)

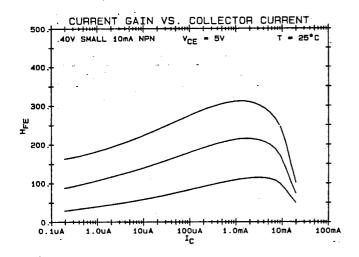
 $\left|\frac{\Delta h_{\text{FE}(\text{MAX})}}{100\%}\right| < \frac{h_{\text{FE}(2)}}{h_{\text{FE}(1)}} < 1+2\left|\frac{\Delta h_{\text{FE}(\text{MAX})}}{100\%}\right|$ \mathbf{h}_{FF} matching is satisfied by 2)

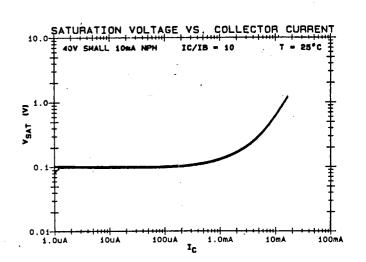
 $h_{\text{FE}(1)}$ and $h_{\text{FE}(2)}$ are any two current gains chosen from a population of like transistors on chip.

- Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage. 3)
- Matching of V_{BE} is satisfied by $|V_{BE(2)} V_{BE(1)}| < 2|\Delta V_{BE(MAX)}|$ where $V_{BE(1)}$ and $V_{BE(2)}$ are any two base-emitter voltages chosen from a population of like 4) transistors on chip.
- It is not recommended to operate the transistor in the saturation mode when 5) only one collector contact or two collector contacts on the same N+ diffusion region are used, since a high saturation voltage is inevitable, especially at increased collector currents.
- Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of lpF for each bonding pad which is related to the specific junction 6) under test.



Layout and Cross-Section of Small 10mA NPN Transistor (Not to Scale)





SMALL 10mA DIODE (TRANSISTOR WITH COLLECTOR AND BASE SHORTED)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE TA=25°C (Unless otherwise noted)

PARAMETER	SYMBOL		CONDITION			TYP	MAX	UNITS
		I _c =100μA			0.61		0.73	
Forward Voltage Drop	V _F	. I _F =1mA	f _F =1mA				0.79	٧
	, i	I _F =10mA			0.79		0.91	
Matching of Forward Voltages	۵۷F	I _F =lmA (Note 1)				±2	±6	mV
Temperature Coefficient of V _F	ΔV _F /ΔT	I _F *1mA				-1.8		mV/ ^O C
		V - 20V	TA=25°C	(Note 2)		0.2		
Leakage Current	Io	V _R =20V	TA=125°C	(Note 2)		10		nA
Breakdown Voltage	BVD	I _R =10µA			6.25		7.25	٧
Maximum Diode Current	I _{F(MAX)}						20	mA
Junction Capacitance	c,	v _D =ov		(Note 3)		1.1		pF

- Matching of V_F is satisfied by $\|V_{F(2)} V_{F(1)}\| \le 2\|\Delta V_{F(MAX)}\|$ where $V_{F(1)}$ and $V_{F(2)}$ are any two forward voltages chosen from a population of like diodes on 1) chip.
- Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage. 2)
- Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of lpF for each bonding pad which is related to the specific junction 3) under test.

SMALL 10mA ZENER DIODE (EMITTER-BASE JUNCTION OF TRANSISTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE T_A =25 $^{\rm O}$ C (Unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN	ТҮР	MAX	UNITS
Breakdown Voltage		I ₇ =1µA	•	6.2	6.5	7.2	
	v _z	I ₇ =10μA		6.25	6.55	7.25	1
		1 ₇ =100µA	(Note 1)	6.3	6.6	7.3] v
	-	I ₇ =lmA	(Note 1)	6.4	6.7	7.4	
•		I _Z =10mA	(Note 1)	7	7.3	8	
Dynamic Impedance (in the Breakdown Mode)	R _Z	I _Z =1mA			85		Ω
Temperature Coefficient of Breakdown	۵۷ _Z /۵۲	I _Z =1mA			2.4		mV/ ^O C

Notes:

Base-emitter breakdown, unlike base-collector breakdown, can be damaging to the transistor particularly for long breakdown duration at high current. Under these conditions, $h_{\rm FE}$ degradation is inevitable; therefore, $V_{\rm Z}$ is tested at lpA and lopA for each transistor. Operation at higher current has been fully characterized and is guaranteed by extrapolation.

HI-TECH LINEAR COMPONENT DATA SHEET

40V LATERAL PNP TRANSISTOR 1ma Quad Collector

GENERAL DESCRIPTION

The lateral PNP transistor has an oval-shaped, P-type emitter, surrounded by four P-type collector diffusions in a single base region. The base is made with an N+ diffusion with two base contacts in it. All four collectors should be connected together when a single collector transistor is required. When current ratios are important, such as for multiple current sources, the collectors can be used individually. Unused collectors must be connected to the substrate or any other potential that will ensure that the transistor does not saturate.

FEATURES Quad Collectors Matched V_{BE} and h_{FE} Transistor Parameters TYPICAL APPLICATIONS

Current Sources Active Loads Level Shifters Blasing Stages Amplifiers

O.25mA (PER COLLECTOR) QUAD-COLLECTOR LATERAL PNP TRANSISTOR (EACH COLLECTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A=25^{\circ}C$ (Unless otherwise noted)

PARAMETER	SYMBOL		CONDITIONS		MIN	TYP	MAX	UNITS
			I _C =-25μA	One Collector (Note 1)	5		37.5	
DC Current Gain	ħ _{FE}	V _{CE} =-5V	Ic(TOTAL)=-50µA	Two Collectors Connected in Parallel (Note 1)	10		75	
			I _{C(TOTAL)} *-100μA	Four Collectors Connected in Parallel	20		150	
Matching of DC Current Gains	Δħ _{FE}	1 _C =-100 _P A	V _{CE} =-5V	(Note 2)		±5	±15	*
Temperature Coefficient of h _{FE}	Δħ _{FE} /ΔΤ	I _C =-100µA	-55°C < T _A < 125	°c		-0.1		%/°C
	I _{CBO}	V _{CB} =-20V	TA=25°C	(Note 3)		-0.02	-0.2	nA
Collector-Base Leakage Current		CB - 204	TA=125°C	(Note 3)		-5	-50	<u> </u>
	ICEO	V _{CE} =-20V	T _A =25 ⁰ C	(Note 3)		-0.2	-2	nA
Collector-Emitter Leakage Current			TA=125°C	(Note 3)		-0.05	-0.5	
Collector-Emitter Breakdown Voltage	BVCEO	I _C =-100µA			-40			٧
Collector-Base Breakdown Voltage	вусво	1 _C =-100μA			-60			٧
Emitter-Base Breakdown Voltage	BVEBO	I _E =-100μA			-60			٧
Base-Substrate Breakdown Voltage	BVBS	I _B =10µA			40			٧
Base-Emitter Forward Voltage	V _{BE}	I _E =100µA	V _{CE} =-5V		-0.62		-0.77	٧
Matching of Base-Emitter Forward Voltages	۵۷BE	I _E =100μA	V _{CE} *-5V	(Note 4)		±2	±6	mV
Temperature Coefficient of V _{BF}	ΔV _{BE} /ΔT	I _E =100μA	V _{CE} *-5V			1.8		mV/ ^O C

information furnished by HI-Tech Linear is believed to be accurate and reliable. However, no responsibility is assumed by HTL for its use, nor for any infringements of pattents or other rights which may result from its use. HTL reserves the right to make changes at any time without notice.

tech linear conronen

QUAD-COLLECTOR LATERAL PHP TRANSISTOR (CONTINUED)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Collector-Emitter Saturation Voltage	V _{CE} (SAT)	(I _{C(TOTAL)} /I _B)=1	I _C =-25µA One Collector (Notes 1,5) I _C (TOTAL)=-50µA Two Collectors Connected in Parallel (Notes 1,5) I _C (TOTAL)=-100µA Four Collectors Connected in Parallel (Notes 5)		-0.12	-0.2	٧
Maximum Usable Collector Current	I _{C(MAX)}	(Per Collector)				-0.5	mA
Cutoff Frequency	fŢ	1C(TOTAL)=-100µA VCE=-5	Four Collectors / Connected in Parallel		3.5		MHz
		(I _{C(TOTAL)} /I _B)-1	1C(TOTAL)=-100µA Four Collectors Connected in Parallel		100		
Storage Time	*5	R _B =750Ω	IC(TOTAL)=-lmA Four Collectors Connected in Parallel		140		ns
Emitter-Base Capacitance	C _{EB}	V _{EB} =0V	(Note 6)		0.2		pF
Collector-Base Capacitance	ССВ	V _{CB} =0V	(Note 6)		0.5		pF
Base-Substrate Capacitance	C _{BS}	V _{BS} *OV	(Note 6)		5		рF

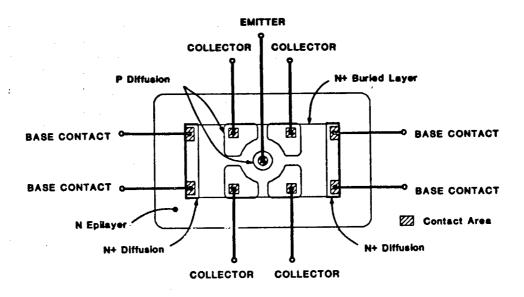
Notes:

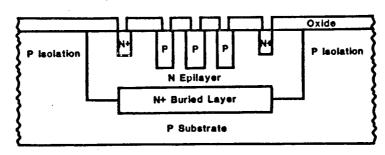
With the other collectors grounded. 1)

 $\left|\frac{^{\Delta h}_{FE(MAX)}}{100\%}\right| < \frac{^{11}_{FE(2)}}{^{h}_{FE(1)}}$ $h_{\mbox{\it FE}}$ matching is satisfied by 2) $\mathbf{h}_{\mathsf{FE}(1)}$ and $\mathbf{h}_{\mathsf{FE}(2)}$ are any two current gains chosen from a population of like transistors on chip.

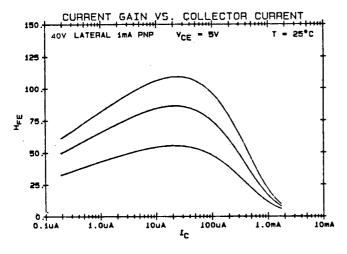
- Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage. 3)
- Matching of V_{BE} is satisfied by $|V_{BE(2)} V_{BE(1)}| < 2|\Delta V_{BE(MAX)}|$ where $V_{BE(1)}$ 4) and VBE(2) are any two base-emitter voltages chosen from a population of like transistors on chip.
- It is not advisable to operate the lateral PNP transistor in the saturation 5) mode since the parasitic vertical substrate transistor (related to the lateral transistor) becomes heavily active.
- Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.

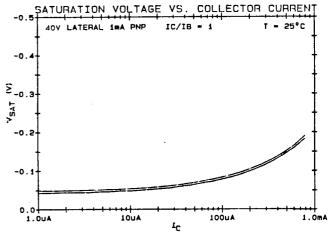
HI-TECH LINEAR COMPONENT DATA SHEET





Lay out and Cross-Section of O.25mA (Per Collector) Quad-Collector Lateral PNP Transistor (Not to Scale)







LATERAL PNP DIODE (EMITTER-BASE JUNCTION OF TRANSISTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A = 25^{\circ}C$ (Unless otherwise noted)

PARAMETER	SYMBOL		CONDITIONS		MIN	TYP.	MAX	UNITS
		I _F =100μA		, 	0.61		0.73	
Forward Voltage Drop	v _F	I _F =1mA			0.74		0.86	٧
		I _F =10mA (Note		(Note 1)		1.15		
Matching of Forward Voltages	ΔV _F	I _F =lmA		(Note 2)		±2	±6	mV
Temperature Coefficient of V _F	ΔV _F /ΔT	I _F =1mA				-1.8		mV/ ^O C
-	_	V _R =40V	TA=25°C	(Note 3)		0.5		nA
Leakage Current	¹ o		TA=125°C	(Note 3)		50		"^
Breakdown Voltage	BVD	I _R =100uA		 	60			٧
Maximum Diode Current	I _F (MAX)			(Note 1)			10	mA
Junction Capacitance	c _J	ν _D =0ν		(Note 4)		0.2		pF

- The lateral PNP diode, like the lateral PNP transistor, has a parasitic vertical substrate current that becomes dominant at high operating current. This substrate loss current becomes comparable to the diode forward current at about Ema 1) 5mA.
- Matching of V_F is satisfied by $\|V_{F(2)} V_{F(1)}\| \le 2\|\Delta V_{F(MAX)}\|$ where $V_{F(1)}$ and $V_{F(2)}$ are any two forward voltages chosen from a population of like diodes on
- Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.
- Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.

HI-TECH LINEAR COMPONENT DATA SHEET

40V P-TYPE DIFFUSED RESISTORS

200Ω, **450**Ω, **900**Ω, **1.8**ΚΩ, **3.6**ΚΩ

GENERAL DESCRIPTION

The P-type diffused resistors are made during the base diffusion step in the integrated circuit process. They exhibit excellent ratio matching properties which are primerlly dependent on the masking accuracy in the fabrication process. However, the obsolute values are not as accurate as they are directly related to the tolerances in the diffusion process.

FEATURES
Matched Resistor Ratios
TYPICAL APPLICATIONS
Analog and Digital Circuitry

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A=25^{\circ}C$ (Unless otherwise noted)

PARAMETER	SYMBOL		CONDITIONS		MIN	ТҮР	MAX	UNIT:
Absolute Values 2000 4500 9000 1.8Kn 3.6Kn	R	V _R =5V			150 337.5 675 1350 2700	200 450 900 1800 3600	250 562.5 1125 2250 4500	Ω
Epi (Vcc Terminal)- Substrate Breakdown Voltage	BV _{NS}	Au0f= <mark>N_</mark> I			40			٧
Epi (Vcc Terminal)- Resistor Breakdown Voltage	BV _{NR}	I _N =100μA	1		60			٧
Resistor-Substrate Breakdown Voltage	BV _{RS}	I _R =10µA			40			٧
		V _R =5V	-55°C < TA	< -25 ⁰ C		-0.02		
Temperature Coefficient of R	ΔR/ΔΤ		-25°C < TA	< 25 ⁰ C		0.06		%/ ⁰ 0
			25°C < TA	125 ⁰ C		0.13		
Matching of Equal Design Value Resistors	ΔR(1:1)	V _R =5V	^R 2* ^R 1	(Notes 1,2)			±3	*
	ΔR(1:2)		R2=2R1	(Notes 1,2)			±4	
Ratio Matching of Unequal Design Value Resistors	ΔR(1:4)	V _R =5V	R2=4R1	(Notes 1,2)			±5	*
	ΔR(1:8)		R ₂ =8R ₁	(Notes 1,2)			±6	
Maximum Power Dissipation	P _{D(MAX)}		_				300	mW
Epi (Vcc Terminal)- Resistor Capacitance 2000 4500 9000 1.8K0 3.6K0	C _{NR}	V _{NR} =OV		(Notes 3,4)		0.7 0.4 0.6 0.8 1.7		pF

Information furnished by HI-Tech Linear is believed to be accurate and reliable. However, no responsibility is assumed by HTL for its use, nor for any infringements of pattents or other rights which may result from its use. HTL reserves the right to make changes at any time without notice.

HISTERN LINEAR COMPONENT DATA

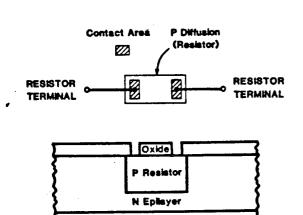
Notes:

1) Resistor ratio matching is satisfied by

$$k\left(1-2\left|\frac{\Delta R_{\left(MAX\right)}}{100x}\right|\right) < \frac{R_{2}}{R_{1}} < k\left(1+2\left|\frac{\Delta R_{\left(MAX\right)}}{100x}\right|\right)$$

where k is the resistor ratio of the nominal values, and ${\rm R}_1$ and ${\rm R}_2$ are any two resistors chosen from these populations on chip.

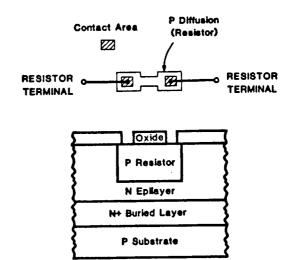
- These particular matching parameters apply to the various resistor ratios on chip.
- Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of lpF for each bonding pad which is related to the specific junction under test. 3)
- These capacitances refer to each individual resistor; however, most resistors on chip are strung together, thus presenting a higher total capacitance for each resistor group.



Layout and Cross-Section of 200n P-Type Diffused Resistor (Not to Scale)

N+ Buried Layer

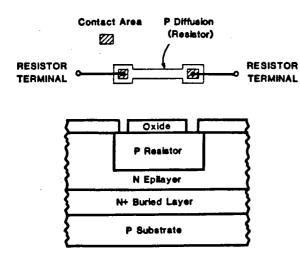
P Substrate



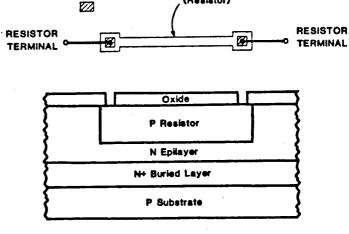
Layout and Cross-Section of 450n P-Type Diffused Resistor (Not to Scale)

P Diffusion

(Resistor)



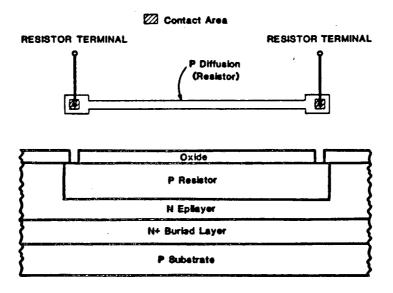
Layout and Cross-Section of 900n P-Type Diffused Resistor (Not to Scale)



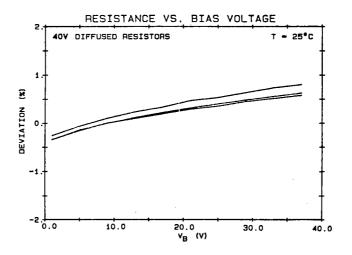
Contact Area

Layout and Cross-Section of 1.8Kn P-Type (Not to Scale) Diffused Resistor

HI-TECH LINEAR COMPONENT DATA SHEET



Layout and Cross-Section of 3.6Kn P-Type Diffused Resistor (Not to Scale)



40V EPI PINCH RESISTOR

 $60K\Omega$

GENERAL DESCRIPTION

The epi pinch resistor is made with a donut-shaped epilayer region that defines its size and shape. Two small N+ diffusion regions in the epilayer provide the ohmic contacts to the resistor terminals. The P-type substrate and isolation regions act as the resistor gate. The gate is therefore permanently biased at the most negative potential in the circuit. Unlike the base pinch resistor, the epi pinch resistor can sustain at least 40V before breakdown occures.

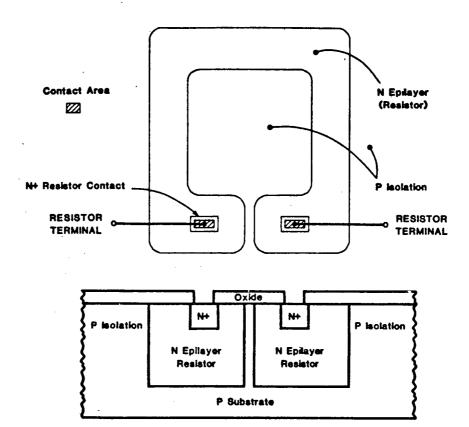
FEATURES Matched Resistor Values TYPICAL APPLICATIONS **Current Sources** General Purpose Cirultry

上面积10年20日4月 日村

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A = 25^{\circ}C$ (Unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	man mining	MIN	TYP	MAX	UNITS
Absolute Value	R	I _R =10μΑ	i Interest	30	60	120	KΩ
Matching of Resistor Values	ΔR	I _R =10µA	(Note 1)		±5		*
Breakdown Voltage (Across Resistor Terminals)	BV _R	· I _R =2mA] in actions		40			٧
Resistor-Substrate Breakdown Voltage	BVRS	I _R =10µA	:.	40			٧
Temperature Coefficient of R	ΔR/ΔT	-55°C < T _A < 125°C			0.5		%/ ⁰ C
Maximum Power Dissipation	P _{D(MAX)}					200	m₩
Resistor-Substrate Capacitance	¢ _{RS}	Y _{RS} =0Y	(Note 2)		6.5		pF

- Resistor matching is satisfied by $1-2\left|\frac{\Delta R_{(MAX)}}{100x}\right| < \frac{R_2}{R_1} < 1+2\left|\frac{\Delta R_{(MAX)}}{100x}\right|$ where R_1 1) and ${\bf R_2}$ are any two resistors chosen from a population of the same nominal value on chip.
- Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction 2)



Layout and Cross-Section of $60\mbox{K}\Omega$ Epi Pinch Resistor (Not to Scale)

