# Si-Cr THIN FILM RESISTORS

## VALUES OF 10Ω to 100KΩ, LASER TRIMMABLE

### GENERAL DESCRIPTION

HTL'S IC compatible silicon-chrome resistors are offered as an option on selected semi-custom analog arrays as well as on all custom integrated circuits. The resistors are made using a very accurate deposition process by which a thin film of high-resistivity silicon-chrome material is deposited over the field oxide surface of the chip, prior to the aluminum metalization step. This thin film resistor offers some excellent characteristics that cannot be matched by the normal IC diffused or implanted resistors. In addition to the excellent qualities of the silicon-chrome resistors, they can also be laser trimmed to a very accurate matching ratio of typically ±0.005%.

### FEATURES

Wide Range of Resistor Values
Negligible Voltage Dependence
Very Low Temperature Coefficient
Very High Breakdown Voltage
Good Matching Characteristics
Very Low Temperature Drift Matching
Very Low Capacitance
Excellent Ratio of Laser Trimmed Resistors

### TYPICAL APPLICATIONS

Analog and Digital Precision Circuits
A/D and D/A Converters
Feedback Networks
Summing Amplifiers
Precision Voltage Dividers
Operational Amplifiers and Comparators
Voltage References and Regulators
Active Filters

Electrical characteristics, Prior to laser trimming, at ambient temperature $T_A = 25°C$ (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Absolute Sheet Resistance | $\rho$ | $V_R$=5V | 800 | 1000 | 1200 | Ω/□ |
| Resistor-Substrate Breakdown Voltage | $BV_{RS}$ | $I_S$=1μA (Note 1) | 150 | | | V |
| Temp. Coefficient of Resistors | $\Delta R/\Delta T$ | $V_R$=5V $-55°C < T_A < 125°C$ | | -35 | -60 | PPM/°C |
| Matching of Equal Design Value Resistors | $\Delta R(1:1)$ | $V_R$=5V $R_1 = R_2$ (Note 2,3) | | | | % |
| 10μm Resistor Width | | | | ±1 | | |
| 15μm Resistor Width | | | | ±0.5 | | |
| 25μm Resistor Width | | | | ±0.2 | | |
| 50μm Resistor Width | | | | ±0.1 | | |
| 75μm Resistor Width | | | | ±0.07 | | |
| 100μm Resistor Width | | | | ±0.05 | | |

Electrical characteristics, Prior to laser trimming, at ambient temperature $T_A = 25°C$ (CONTINUED)

| | | | | | | |
|---|---|---|---|---|---|---|
| Matching of Unequal Design Value Resistors<br>10μm Resistor Width | $\Delta R(1:2)$<br>$\Delta R(1:4)$<br>$\Delta R(1:8)$ | $R_2 = 2R_1$<br>$R_2 = 4R_1$<br>$R_2 = 8R_1$ (Note 2,3) | | $\pm 2$<br>$\pm 3$<br>$\pm 4$ | | |
| 15μm Resistor Width | $\Delta R(1:2)$<br>$\Delta R(1:4)$<br>$\Delta R(1:8)$ | $R_2 = 2R_1$<br>$R_2 = 4R_1$<br>$R_2 = 8R_1$ (Note 2,3) | | $\pm 1$<br>$\pm 2$<br>$\pm 3$ | | |
| 25μm Resistor Width | $\Delta R(1:2)$<br>$\Delta R(1:4)$<br>$\Delta R(1:8)$ | $R_2 = 2R_1$<br>$R_2 = 4R_1$<br>$R_2 = 8R_1$ (Note 2,3) | | $\pm 0.5$<br>$\pm 1$<br>$\pm 2$ | | |
| 50μm Resistor Width | $\Delta R(1:2)$<br>$\Delta R(1:4)$<br>$\Delta R(1:8)$ | $R_2 = 2R_1$<br>$R_2 = 4R_1$<br>$R_2 = 8R_1$ (Note 2,3) | | $\pm 0.2$<br>$\pm 0.5$<br>$\pm 1$ | | |
| 75μm Resistor Width | $\Delta R(1:2)$<br>$\Delta R(1:4)$<br>$\Delta R(1:8)$ | $R_2 = 2R_1$<br>$R_2 = 4R_1$<br>$R_2 = 8R_1$ (Note 2,3) | | $\pm 0.15$<br>$\pm 0.25$<br>$\pm 0.5$ | | |
| 100μm Resistor Width | $\Delta R(1:2)$<br>$\Delta R(1:4)$<br>$\Delta R(1:8)$ | $R_2 = 2R_1$<br>$R_2 = 4R_1$<br>$R_2 = 8R_1$ | | $\pm 0.1$<br>$\pm 0.2$<br>$\pm 0.3$ | | |
| Temp. Coefficient of Matching Drift | $\Delta R(1:1)/\Delta T$<br>$\Delta R(1:2)/\Delta T$<br>$\Delta R(1:4)/\Delta T$<br>$\Delta R(1:8)/\Delta T$ | $V_R = 5V$ $-55°C < T_A < 125°C$ | | $\pm 2$<br>$\pm 4$<br>$\pm 8$<br>$\pm 16$ | | PPM/°C |
| Resistor-Substrate Capacitance | $C_{RS}$ | $0 < V_R < BV_{RS}$ (Note 4) | | 0.02 | | $pF/mil^2$ |
| | | | | $3.1 \cdot 10^{-5}$ | | $pF/\mu m^2$ |

Notes

1) Breakdown occurs through a thick layer of oxide (Field Oxide). The breakdown is destructive and non-reversible.
2) Resistor ratios matching is satisfied by

$$k\left(1-2\left|\frac{\Delta R(MAX)}{100\%}\right|\right) < \frac{R_2}{R_1} < k\left(1+2\left|\frac{\Delta R(MAX)}{100\%}\right|\right)$$

Where K is the resistor ratio of the nominal values, and $R_1$ and $R_2$ are any two resistors chosen from these populations on chip.

3) These particular matching parameters apply to the various resistor ratios on chip, prior to laser triming. Matching of laser trimmed resistors is typically $\pm 0.005\%$.

4) MOS capacitance is specified. An average capacitance of 0.5pF must be added if resistor is connected to a package pin. Also included must be a capacitance of about 1pF for each bonding pad which is related to the specific resistor.

# 20V SMALL NPN TRANSISTOR

## 10mA QUAD COLLECTOR CONTACT

### GENERAL DESCRIPTION

The small 10mA NPN transistor has two N+ diffusion regions in the collector area with two collector contacts in each of these diffusions. The contacts are normally connected together to reduce the series collector resistance as well as the saturation voltage. The small NPN transistor is available in two versions, with and without a deep N+ diffusion in the collector region. The deep N+ diffusion allows for an additional increase in the operating current.

### FEATURES

Four Collector Contacts
Matched $V_{BE}$ and $h_{FE}$ Transistor Parameters

### TYPICAL, APPLICATIONS

Amplifiers
Comparators
Current Sources
Bias Circuits
Level Shifters
Emitter Followers
Diode Connected Transistors
Zener Diode Connections

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| DC Current Gain | $h_{FE}$ | $I_C$=1mA | $V_{CE}$=5V | (Note 1) | 80 | | 300 | |
| Matching of DC Current Gains | $\Delta h_{FE}$ | $I_C$=1mA | $V_{CE}$=5V | (Note 2) | | ±5 | ±10 | % |
| Temperature Coefficient of $h_{FE}$ | $\Delta h_{FE}/\Delta T$ | $I_C$=1mA | -55°C < $T_A$ < 125°C | | | 0.5 | | %/°C |
| Collector-Base Leakage Current | $I_{CBO}$ | $V_{CB}$=20V | $T_A$=25°C | (Note 3) | | 0.01 | 0.1 | nA |
| | | | $T_A$=125°C | (Note 3) | | 1 | 10 | |
| Collector-Emitter Leakage Current | $I_{CEO}$ | $V_{CE}$=20V | $T_A$=25°C | (Note 3) | | 0.2 | 2 | nA |
| | | | $T_A$=125°C | (Note 3) | | 0.2 | 2 | µA |
| Collector-Emitter Breakdown Voltage | $LV_{CEO}$ | $I_C$=1mA | | | 20 | | | V |
| Collector-Base Breakdown Voltage | $BV_{CBO}$ | $I_C$=100µA | | | 30 | | | V |
| Emitter-Base Breakdown Voltage | $BV_{EBO}$ | $I_E$=10µA | | | 6.25 | | 7.25 | V |
| Collector-Substrate Breakdown Voltage | $BV_{CS}$ | $I_C$=10µA | | | 20 | | | V |
| Base-Emitter Forward Voltage | $V_{BE}$ | $\|I_E\|$=1mA | $V_{CE}$=5V | | 0.67 | | 0.79 | V |
| Matching of Base-Emitter Forward Voltages | $\Delta V_{BE}$ | $\|I_E\|$=1mA | $V_{CE}$=5V | (Note 4) | | ±2 | ±6 | mV |
| Temperature Coefficient of $V_{BE}$ | $\Delta V_{BE}/\Delta T$ | $\|I_E\|$=1mA | $V_{CE}$=5V | | | -1.8 | | mV/°C |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_C$=1mA, $(I_C/I_B)$=10 | One Collector Contact (One Diffusion Region) | (Note 5) | | 0.16 | 0.3 | V |
| | | | Two Collector Contacts (Two Diffusion Regions) | (Note 5) | | 0.14 | 0.25 | |
| | | | Four Collector Contacts (Two Diffusion Regions) | | | 0.09 | 0.17 | |
| Maximum Collector Current | $I_{C(MAX)}$ | $P_{D(MAX)}$=300mW | | | | | 20 | mA |
| Cutoff Frequency | $f_T$ | $I_C$=5mA | $V_{CE}$=5V | | | 500 | | MHz |
| Storage Time | $t_S$ | $(I_C/I_B)$=10 | $R_B$=750Ω | $I_C$=1mA | | 6 | | ns |
| | | | | $I_C$=10mA | | 100 | | |
| Emitter-Base Capacitance | $C_{EB}$ | $V_{EB}$=0V | | (Note 6) | | 1 | | pF |
| Collector-Base Capacitance | $C_{CB}$ | $V_{CB}$=0V | | (Note 6) | | 1 | | pF |
| Collector-Substrate Capacitance | $C_{CS}$ | $V_{CS}$=0V | | (Note 6) | | 3.8 | | pF |

Notes:

1) All collector contacts connected in parallel.

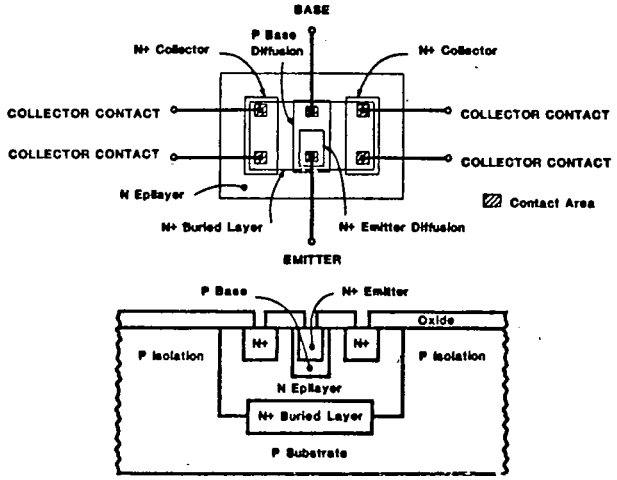
2) $h_{FE}$ matching is satisfied by $1-2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right| < \frac{h_{FE(2)}}{h_{FE(1)}} < 1+2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right|$ where $h_{FE(1)}$ and $h_{FE(2)}$ are any two current gains chosen from a population of like transistors on chip.

3) Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.

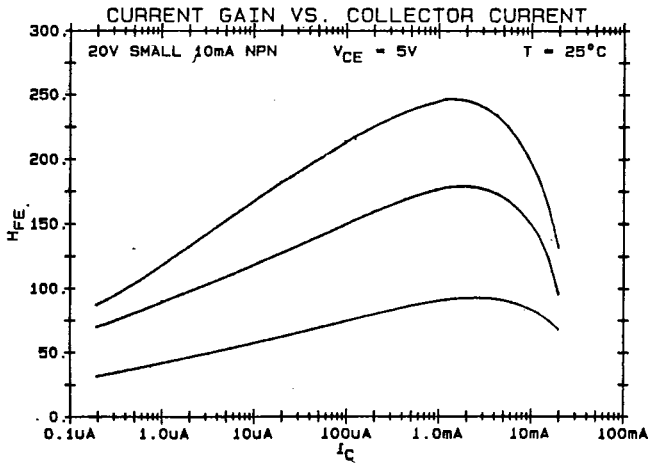
4) Matching of $V_{BE}$ is satisfied by $|V_{BE(2)}-V_{BE(1)}| < 2|\Delta V_{BE(MAX)}|$ where $V_{BE(1)}$ and $V_{BE(2)}$ are any two base-emitter voltages chosen from a population of like transistors on chip.

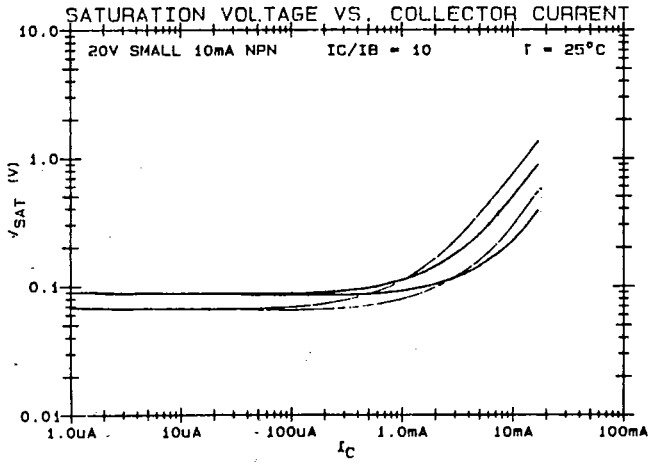
5) It is not recommended to operate the transistor in the saturation mode when only one collector contact or two collector contacts on the same N+ diffusion region are used, since a high saturation voltage is inevitable, especially at increased collector currents.

6) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.




Layout and Cross-Section of Small 10mA NPN Transistor
(Not to Scale)



## SMALL 10mA DIODE (TRANSISTOR WITH COLLECTOR AND BASE SHORTED)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITION | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Forward Voltage Drop | $V_F$ | $I_F$=100μA | | 0.61 | | 0.73 | V |
| | | $I_F$=1mA | | 0.67 | | 0.79 | |
| | | $I_F$=10mA | | 0.77 | | 0.89 | |
| Matching of Forward Voltages | $\Delta V_F$ | $I_F$=1mA | (Note 1) | | ±2 | ±6 | mV |
| Temperature Coefficient of $V_F$ | $\Delta V_F/\Delta T$ | $I_F$=1mA | | | -1.8 | | mV/°C |
| Leakage Current | $I_O$ | $V_R$=20V | $T_A$=25°C (Note 2) | | 0.1 | | nA |
| | | | $T_A$=125°C (Note 2) | | 10 | | |
| Breakdown Voltage | $BV_D$ | $I_R$=10μA | | 6.25 | | 7.25 | V |
| Maximum Diode Current | $I_{F(MAX)}$ | | | | | 20 | mA |
| Junction Capacitance | $C_J$ | $V_D$=0V | (Note 3) | | 1 | | pF |

Notes:

1) Matching of $V_F$ is satisfied by $|V_{F(2)}-V_{F(1)}| < 2|\Delta V_{F(MAX)}|$ where $V_{F(1)}$ and $V_{F(2)}$ are any two forward voltages chosen from a population of like diodes on chip.

2) Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.

3) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.

## SMALL 10mA ZENER DIODE (EMITTER-BASE JUNCTION OF TRANSISTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Breakdown Voltage | $V_Z$ | $I_Z$=1μA | | 6.2 | 6.7 | 7.2 | V |
| | | $I_Z$=10μA | | 6.25 | 6.75 | 7.25 | |
| | | $I_Z$=100μA | (Note 1) | 6.3 | 6.8 | 7.3 | |
| | | $I_Z$=1mA | (Note 1) | 6.4 | 6.9 | 7.4 | |
| | | $I_Z$=10mA | (Note 1) | 7 | 7.5 | 8 | |
| Dynamic Impedance (in the Breakdown Mode) | $R_Z$ | $I_Z$=1mA | | | 75 | | Ω |
| Temperature Coefficient of Breakdown Voltage | $\Delta V_Z/\Delta T$ | $I_Z$=1mA | | | 2.4 | | mV/°C |

Notes

1) Base-emitter breakdown, unlike base-collector breakdown, can be damaging to the transistor particularly for long breakdown duration at high current. Under these conditions, $h_{FE}$ degradation is inevitable; therefore, $V_Z$ is tested at 1μA and 10μA for each transistor. Operation at higher current has been fully characterized and is guaranteed by extrapolation.

# 20V LOW NOISE NPN TRANSISTOR

## 10mA DUAL COLLECTOR CONTACT

### GENERAL DESCRIPTION

The low noise NPN transistor is identical in size to th 10mA small NPN transistor. It has a single N+ diffusion in the collector area with two collector contacts in it. The base diffusion and the base contact are much larger than those of the small NPN transistor. This results in a much reduced base resistance and consequently in a lower level of noise. It is recommended to use the transistor at very low current levels of 10nA to 1mA to maintain the low noise characteristics.

### FEATURES

Large Base Contact for Reduced Noise
Dual Collector Contacts
Matched $V_{BE}$ and $h_{FE}$ transistor parameters

### TYPICAL APPLICATIONS

Low Noise Amplifiers
Differential Input Stages
Low Level Amplifiers

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| DC Current Gain | $h_{FE}$ | $I_C$=1mA $V_{CE}$=5V | | (Note 1) | 80 | | 300 | |
| Matching of DC Current Gains | $\Delta h_{FE}$ | $I_C$=1mA $V_{CE}$=5V | | (Note 2) | | ±5 | ±10 | % |
| Temperature Coefficient of $h_{FE}$ | $\Delta h_{FE}/\Delta T$ | $I_C$=1mA -55°C < $T_A$ < 125°C | | | | 0.5 | | %/°C |
| Collector-Base Leakage Current | $I_{CBO}$ | $V_{CB}$=20V | $T_A$=25°C | (Note 3) | | 0.01 | 0.1 | nA |
| | | | $T_A$=125°C | (Note 3) | | 1 | 10 | |
| Collector-Emitter Leakage Current | $I_{CEO}$ | $V_{CE}$=20V | $T_A$=25°C | (Note 3) | | 0.2 | 2 | nA |
| | | | $T_A$=125°C | (Note 3) | | 0.2 | 2 | µA |
| Collector-Emitter Breakdown Voltage | $LV_{CEO}$ | $I_C$=1mA | | | 20 | | | V |
| Collector-Base Breakdown Voltage | $BV_{CBO}$ | $I_C$=100µA | | | 30 | | | V |
| Emitter-Base Breakdown Voltage | $BV_{EBO}$ | $I_E$=10µA | | | 6.25 | | 7.25 | V |
| Collector-Substrate Breakdown Voltage | $BV_{CS}$ | $I_C$=10µA | | | 20 | | | V |
| Base-Emitter Forward Voltage | $V_{BE}$ | $\|I_E\|$=1mA $V_{CE}$=5V | | | 0.67 | | 0.79 | V |
| Matching of Base-Emitter Forward Voltages | $\Delta V_{BE}$ | $\|I_E\|$=1mA $V_{CE}$=5V | | (Note 4) | | ±2 | ±6 | mV |
| Temperature Coefficient of $V_{BE}$ | $\Delta V_{BE}/\Delta T$ | $\|I_E\|$=1mA $V_{CE}$=5V | | | | -1.8 | | mV/°C |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_C$=1mA $(I_C/I_B)$=10 | One Collector Contact | | | 0.2 | 0.3 | V |
| | | | Two Collector Contacts | | | 0.16 | 0.25 | |
| Maximum Collector Current | $I_{C(MAX)}$ | $P_{D(MAX)}$=300mW | | | | | 20 | mA |
| Cutoff Frequency | $f_T$ | $I_C$=5mA $V_{CE}$=5V | | | | 500 | | MHz |
| Storage Time | $t_S$ | $(I_C/I_B)$=10 $R_B$=750Ω | $I_C$=1mA | | | 6 | | ns |
| | | | $I_C$=10mA | | | 100 | | |
| Emitter-Base Capacitance | $C_{EB}$ | $V_{EB}$=0V | | (Note 5) | | 1 | | pF |
| Collector-Base Capacitance | $C_{CB}$ | $V_{CB}$=0V | | (Note 5) | | 1 | | pF |
| Collector-Substrate Capacitance | $C_{CS}$ | $V_{CS}$=0V | | (Note 5) | | 3.8 | | pF |

Notes:

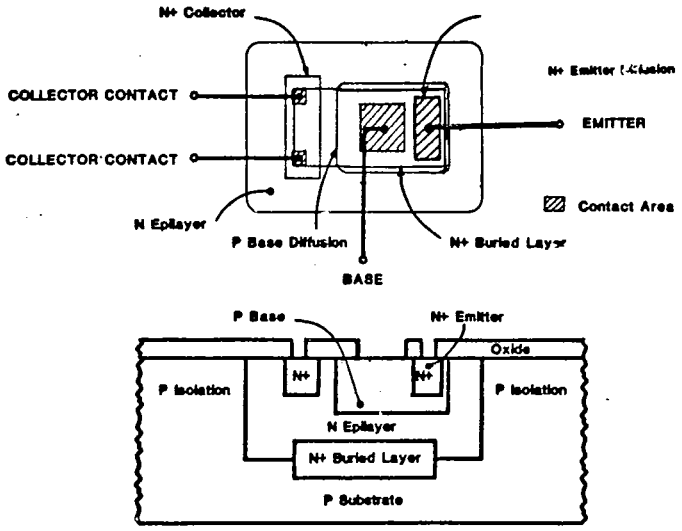
1) All collector contacts connected in parallel.

2) $h_{FE}$ matching is satisfied by $1-2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right| < \frac{h_{FE(2)}}{h_{FE(1)}} < 1+2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right|$ where $h_{FE(1)}$ and $h_{FE(2)}$ are any two current gains chosen from a population of like transistors on chip.

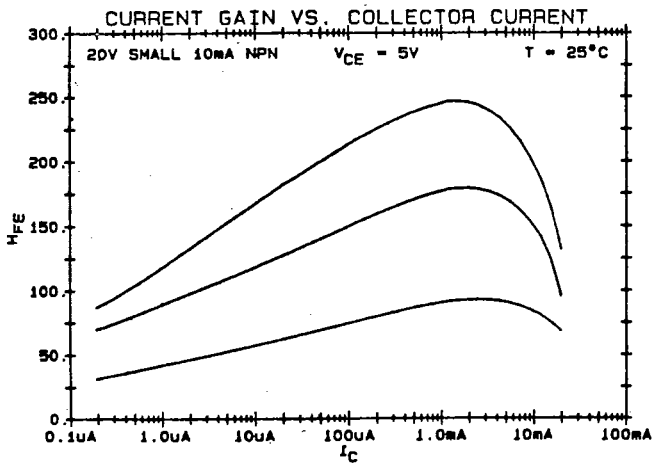
3) Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.

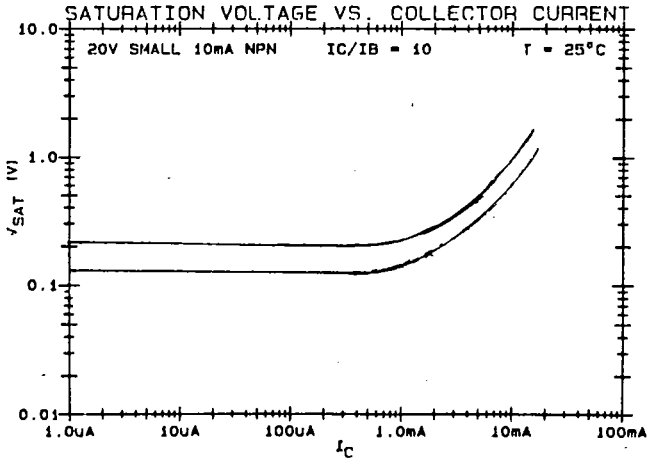
4) Matching of $V_{BE}$ is satisfied by $|V_{BE(2)}-V_{BE(1)}| < 2|\Delta V_{BE(MAX)}|$ where $V_{BE(1)}$ and $V_{BE(2)}$ are any two base-emitter voltages chosen from a population of like transistors on chip.

5) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.




Layout and Cross-Section of Low Noise NPN Transistor
(Not to Scale)



## SMALL 10mA DIODE (TRANSISTOR WITH COLLECTOR AND BASE SHORTED)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITION | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Forward Voltage Drop | $V_F$ | $I_F$=100µA | | 0.61 | | 0.73 | V |
| | | $I_F$=1mA | | 0.67 | | 0.79 | |
| | | $I_F$=10mA | | 0.77 | | 0.89 | |
| Matching of Forward Voltages | $\Delta V_F$ | $I_F$=1mA | (Note 1) | | ±2 | ±6 | mV |
| Temperature Coefficient of $V_F$ | $\Delta V_F/\Delta T$ | $I_F$=1mA | | | -1.8 | | mV/°C |
| Leakage Current | $I_O$ | $V_R$=20V | $T_A$=25°C (Note 2) | | 0.1 | | nA |
| | | | $T_A$=125°C (Note 2) | | 10 | | |
| Breakdown Voltage | $BV_D$ | $I_R$=10µA | | 6.25 | | 7.25 | V |
| Maximum Diode Current | $I_{F(MAX)}$ | | | | | 20 | mA |
| Junction Capacitance | $C_J$ | $V_D$=0V | (Note 3) | | 1 | | pF |

Notes:

1) Matching of $V_F$ is satisfied by $|V_{F(2)}-V_{F(1)}| < 2|\Delta V_{F(MAX)}|$ where $V_{F(1)}$ and $V_{F(2)}$ are any two forward voltages chosen from a population of like diodes on chip.

2) Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.

3) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.

## SMALL 10mA ZENER DIODE (EMITTER-BASE JUNCTION OF TRANSISTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Breakdown Voltage | $V_Z$ | $I_Z$=1µA | | 6.2 | 6.7 | 7.2 | V |
| | | $I_Z$=10µA | | 6.25 | 6.75 | 7.25 | |
| | | $I_Z$=100µA | (Note 1) | 6.3 | 6.8 | 7.3 | |
| | | $I_Z$=1mA | (Note 1) | 6.4 | 6.9 | 7.4 | |
| | | $I_Z$=10mA | (Note 1) | 7 | 7.5 | 8 | |
| Dynamic Impedance (in the Breakdown Mode) | $R_Z$ | $I_Z$=1mA | | | 75 | | Ω |
| Temperature Coefficient of Breakdown Voltage | $\Delta V_Z/\Delta T$ | $I_Z$=1mA | | | 2.4 | | mV/°C |

Notes:

1) Base-emitter breakdown, unlike base-collector breakdown, can be damaging to the transistor particularly for long breakdown duration at high current. Under these conditions, $h_{FE}$ degradation is inevitable; therefore, $V_Z$ is tested at 1µA and 10µA for each transistor. Operation at higher current has been fully characterized and is guaranteed by extrapolation.

# 20V SCHOTTKY NPN TRANSISTOR
## 100uA GUARD-BANDED SCHOTTKY DIODE

**GENERAL DESCRIPTION**

The Schottky NPN transistor is identical in size to the small NPN transistor on chip. It has a single N+ collector diffusion with two collector contacts in it. These contacts are used for the ohmic connection to the transistor's collector. In addition there is also a Schottky contact which is made directly to the N-type epilayer collector. This Schottky contact forms a Schottky diode which can be connected to the base of the transistor to form a Schottky clamped transistor or can be used independently as a Schottky diode. The Schottky diode has a p-type ring in its periphery. The ring functions as a guard-band to reduce the leakage current in the diode.

**FEATURES**

Matched $V_{BE}$ and $h_{FE}$ Transistor Parameters
Matched Schottky Diode Parameters
Transistor Can be Schottky Clamped or Unclamped

**TYPICAL APPLICATIONS**

Non Saturating Logic Gates
High-Speed Circuitry

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| DC Current Gain | $h_{FE}$ | $I_C$=1mA $V_{CE}$=5V | | | 80 | | 300 | |
| Matching of DC Current Gains | $\Delta h_{FE}$ | $I_C$=1mA $V_{CE}$=5V (Note 1) | | | | ±5 | ±10 | % |
| Temperature Coefficient of $h_{FE}$ | $\Delta h_{FE}/\Delta T$ | $I_C$=1mA -55°C < $T_A$ < 125°C | | | | 0.5 | | |
| Collector-Base Leakage Current | $I_{CBO}$ | $V_{CB}$=20V | $T_A$=25°C | Transistor with Clamp (Notes 2,3) | | 10 | 100 | nA |
| | | | | Transistor without Clamp (Notes 2,3) | | 0.01 | 0.1 | |
| | | | $T_A$=125°C | Transistor with Clamp (Notes 2,3) | | 0.1 | 1 | µA |
| | | | | Transistor without Clamp (Notes 2,3) | | 1 | 10 | nA |
| Collector-Emitter Leakage Current | $I_{CEO}$ | $V_{CE}$=20V | $T_A$=25°C | Transistor with Clamp (Notes 2,3) | | 0.5 | 5 | µA |
| | | | | Transistor without Clamp (Notes 2,3) | | 0.2 | 2 | nA |
| | | | $T_A$=125°C | Transistor with Clamp (Notes 2,3) | | 10 | 100 | µA |
| | | | | Transistor without Clamp (Notes 2,3) | | 0.2 | 2 | |
| Collector-Emitter Breakdown Voltage | $LV_{CEO}$ | (Note 4) | | | 20 | | | V |
| Collector-Base Breakdown Voltage | $BV_{CBO}$ | (Note 4) | | | 20 | | | V |
| Emitter-Base Breakdown Voltage | $BV_{EBO}$ | $I_E$=10µA | | | 6.25 | | 7.25 | V |
| Collector-Substrate Breakdown Voltage | $BV_{CS}$ | (Note 4) | | | 20 | | | V |
| Base-Emitter Forward Voltage | $V_{BE}$ | $\|I_E\|$=1mA $V_{CE}$=5V | | | 0.67 | | 0.79 | V |
| Matching of Base-Emitter Forward Voltages | $\Delta V_{BE}$ | $\|I_E\|$=1mA $V_{CE}$=5V (Note 5) | | | | ±2 | ±6 | mV |
| Temperature Coefficient of $V_{BE}$ | $\Delta V_{BE}/\Delta T$ | $\|I_E\|$=1mA $V_{CE}$=5V | | | | -1.8 | | mV/°C |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_C$=1mA | Transistor with Clamp (Notes 3,6) | | | 0.45 | 0.55 | V |
| | | $(I_C/I_B)$=10 | Transistor without Clamp (Notes 3,6) | | | 0.2 | 0.3 | |
| Maximum Collector Current | $I_{C(MAX)}$ | $P_{D(MAX)}$=200mW | | | | | 20 | mA |

SMALL SCHOTTKY CLAMPED NPN TRANSISTOR (CONTINUED)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Cutoff Frequency | $f_T$ | $I_C$=5mA $V_{CE}$=5V | Transistor with Clamp | | | 300 | | MHz |
| | | | Transistor without Clamp | | | 400 | | |
| Storage Time | $t_S$ | $(I_C/I_B)$=10 $R_B$=750Ω | $I_C$=1mA | Transistor with Clamp | | 3 | | ns |
| | | | | Transistor without Clamp | | 5 | | |
| | | | $I_C$=10mA | Transistor with Clamp | | 25 | | |
| | | | | Transistor without Clamp | | 80 | | |
| Emitter-Base Capacitance | $C_{EB}$ | $V_{EB}$=0V (Note 7) | | | | 0.8 | | pF |
| Collector-Base Capacitance | $C_{CB}$ | $V_{CB}$=0V | Transistor with Clamp (Note 7) | | | 1.5 | | pF |
| | | | Transistor without Clamp (Note 7) | | | 1 | | |
| Collector-Substrate Capacitance | $C_{CS}$ | $V_{CS}$=0V (Note 7) | | | | 3 | | pF |

Notes:

1) $h_{FE}$ matching is satisfied by $1-2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right| < \frac{h_{FE(2)}}{h_{FE(1)}} < 1+2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right|$ where $h_{FE(1)}$ and $h_{FE(2)}$ are any two current gains chosen from a population of like transistors on chip.

2) Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.

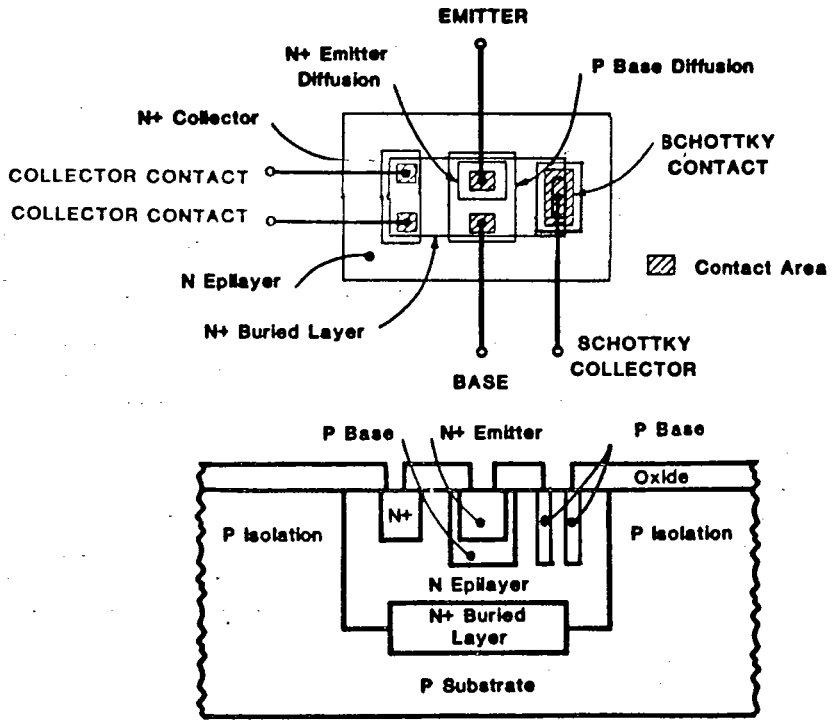
3) In an array design, the NPN transistor can be used without the clamp, the transistor and the diode can be separated.

4) It is not advisable to operate Schottky transistors in the breakdown mode as parameter degradation may occur.

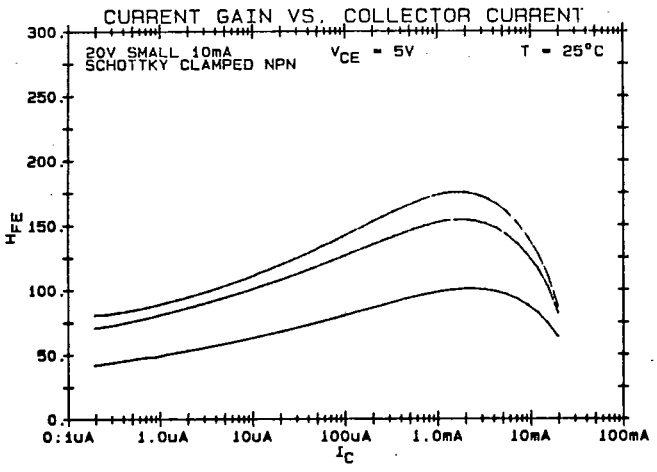
5) Matching of $V_{BE}$ is satisfied by $|V_{BE(2)}-V_{BE(1)}| < 2|\Delta V_{BE(MAX)}|$ where $V_{BE(1)}$ and $V_{BE(2)}$ are any two base-emitter voltages chosen from a population of like transistors on chip.

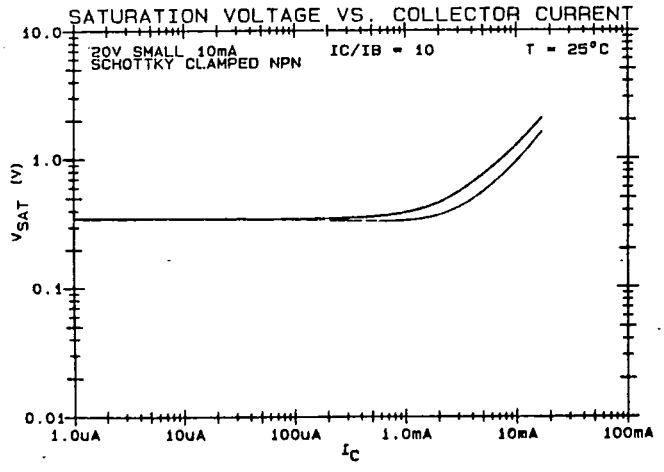
6) The base collector Schottky clamp prevents deep saturation of the transistor.

7) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.




Layout and Cross-Section of Small 10mA Schottky Clamped NPN Transistor
(Not to Scale)



## SMALL 100μA SCHOTTKY DIODE

(Note 1)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

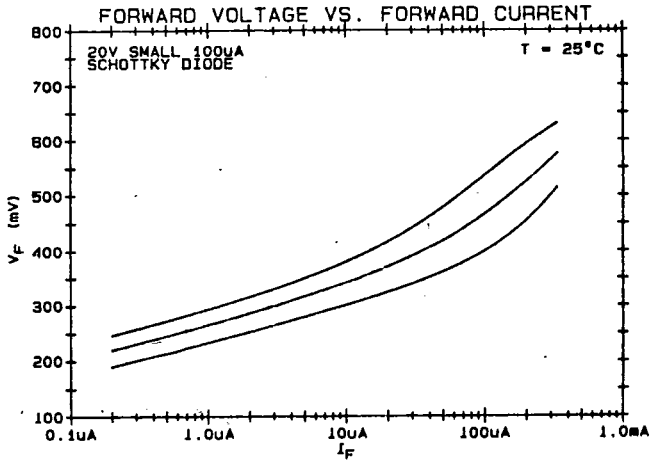
| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Forward Voltage Drop | $V_F$ | $I_F$=10μA | | | 0.27 | | 0.47 | V |
| | | $I_F$=100μA | | | 0.42 | | 0.62 | |
| Temperature Coefficient of $V_F$ | $\Delta V_F/\Delta T$ | $I_F$=100μA | | | | -0.9 | | mV/°C |
| Leakage Current | $I_O$ | $V_R$=20V | $T_A$=25°C | (Note 2) | | 10 | | nA |
| | | | $T_A$=125°C | (Note 2) | | 1 | | μA |
| Breakdown Voltage | $BV_D$ | | | (Note 3) | 20 | | | V |
| Maximum Usable Current | $I_{F(MAX)}$ | | | | | | 0.5 | mA |

Notes:

1) In an array design, the NPN transistor can be used without the clamp, the transistor and the diode can be separated.

2) Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.

3) It is not advisable to operate Schottky diodes in the breakdown mode as parameter degradation may occur.



# 20V LARGE NPN TRANSISTOR
## 100mA DUAL EMITTER

**GENERAL DESCRIPTION**

The large 50mA (per emitter) dual-emitter NPN transistor has two emitters in a common base region with three seperate base contacts. The collector has two seperate N+ diffusion regions with two contacts in each. Normally, all collector contacts are connected together to reduce the series collector resistance as well as the saturation voltage, unless, the collector region is used as a crossunder, or layout considerations restrict the connection of the collector contacts. Also, both emitters should be connected together unless the design calls for a dual emitter transistor, in which case each emitter is capable of handling half of the maximum transistor current. This transistor is available in two versions, with and without a deep N+ diffusion in the collector area. The deep N+ diffusion reduces the saturation voltage and increases the current handling capability.

**FEATURES**

Two Seperate Emitters for Increased Emitter Area and Emitter Efficiency
Quad Collector Contacts
Three Base Contacts

**TYPICAL APPLICATIONS**

Motor Drivers
Relay Drivers
Lamp and LED Drivers
Voltage Regulators
Power Darlingtons

LARGE 50mA (PER EMITTER) DUAL-EMITTER NPN TRANSISTOR

(EACH EMITTER)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| DC Current Gain | $h_{FE}$ | $I_C$=50mA | $V_{CE}$=5V | (Note 1) | 80 | | 300 | |
| Matching of DC Current Gains | $\Delta h_{FE}$ | $I_C$=50mA | $V_{CE}$=5V | (Note 2) | | ±5 | ±10 | % |
| Temperature Coefficient of $h_{FE}$ | $\Delta h_{FE}/\Delta T$ | $I_C$=50mA | -55°C < $T_A$ < 125°C | | | 0.5 | | %/°C |
| Collector-Base Leakage Current | $I_{CBO}$ | $V_{CB}$=20V | $T_A$=25°C | (Note 3) | | 0.05 | 0.5 | nA |
| | | | $T_A$=125°C | (Note 3) | | 5 | 50 | |
| Collector-Emitter Leakage Current | $I_{CEO}$ | $V_{CE}$=20V | $T_A$=25°C | (Note 3) | | 0.5 | 5 | nA |
| | | | $T_A$=125°C | (Note 3) | | 0.5 | 5 | µA |
| Collector-Emitter Breakdown Voltage | $LV_{CEO}$ | $I_C$=1mA | | | 20 | | | V |
| Collector-Base Breakdown Voltage | $BV_{CBO}$ | $I_C$=100µA | | | 30 | | | V |
| Emitter-Base Breakdown Voltage | $BV_{EBO}$ | $I_E$=10µA | | | 6.25 | | 7.25 | V |
| Collector-Substrate Breakdown Voltage | $BV_{CS}$ | $I_C$=10µA | | | 20 | | | V |
| Base-Emitter Forward Voltage | $V_{BE}$ | $V_{CE}$=5V | $\|I_E\|$=5mA | One Emitter | 0.68 | | 0.8 | V |
| | | | | Two Emitters Connected in Parallel | 0.66 | | 0.78 | |
| | | | $\|I_E\|$=50mA | One Emitter | 0.8 | | 0.92 | |
| | | | | Two Emitters Connected in Parallel | 0.74 | | 0.86 | |
| Matching of Base-Emitter Forward Voltages | $\Delta V_{BE}$ | $\|I_E\|$=5mA | $V_{CE}$=5V | (Note 4) | | ±2 | ±6 | mV |
| Temperature Coefficient of $V_{BE}$ | $\Delta V_{BE}/\Delta T$ | $\|I_E\|$=5mA | $V_{CE}$=5V | | | -1.8 | | mV/°C |

LARGE NPN TRANSISTOR (CONTINUED)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_C$=5mA ($I_C/I_B$)=10 | One Emitter | One Collector Contact (One Diffusion Region) (Note 5) | | 0.42 | 0.6 | V |
| | | | | Two Collector Contacts (Two Diffusion Regions) (Note 5) | | 0.2 | 0.4 | |
| | | | | Four Collector Contacts (Two Diffusion Regions) | | 0.17 | 0.22 | |
| | | | Two Emitters Connected in Parallel | One Collector Contact (One Diffusion Region) (Note 5) | | 0.25 | 0.35 | |
| | | | | Two Collector Contacts (Two Diffusion Regions) (Note 5) | | 0.12 | 0.22 | |
| | | | | Four Collector Contacts (Two Diffusion Regions) | | 0.11 | 0.15 | |
| | | $I_C$=50mA ($I_C/I_B$)=10 | Two Emitters Connected in Parallel | One Collector Contact (One Diffusion Region) (Note 5) | | 2.4 | | |
| | | | | Two Collector Contacts (Two Diffusion Regions) (Note 5) | | 1 | 1.4 | |
| | | | | Four Collector Contacts (Two Diffusion Regions) | | 0.9 | 1.3 | |
| Maximum Collector Current | $I_{C(MAX)}$ | $P_{D(MAX)}$=500mW Two Emitters Connected in Parallel (Note 1) | | | | | 200 | mA |
| Cutoff Frequency | $f_T$ | $I_C$=50mA $V_{CE}$=5V Two Emitters Connected in Parallel (Note 1) | | | | 500 | | MHz |
| Storage Time | $t_S$ | ($I_C/I_B$)=10 $R_B$=75Ω Two Emitters Connected in Parallel | | $I_C$=5mA | | 15 | | ns |
| | | | | $I_C$=50mA | | 120 | | |
| Emitter-Base Capacitance | $C_{EB}$ | $V_{EB}$=0V (Note 6) | | | | 2 | | pF |
| Collector-Base Capacitance | $C_{CB}$ | $V_{CB}$=0V (Note 6) | | | | 3 | | pF |
| Collector-Substrate Capacitance | $C_{CS}$ | $V_{CS}$=0V (Note 6) | | | | 6 | | pF |

Notes:

1) All collector contacts connected in parallel.

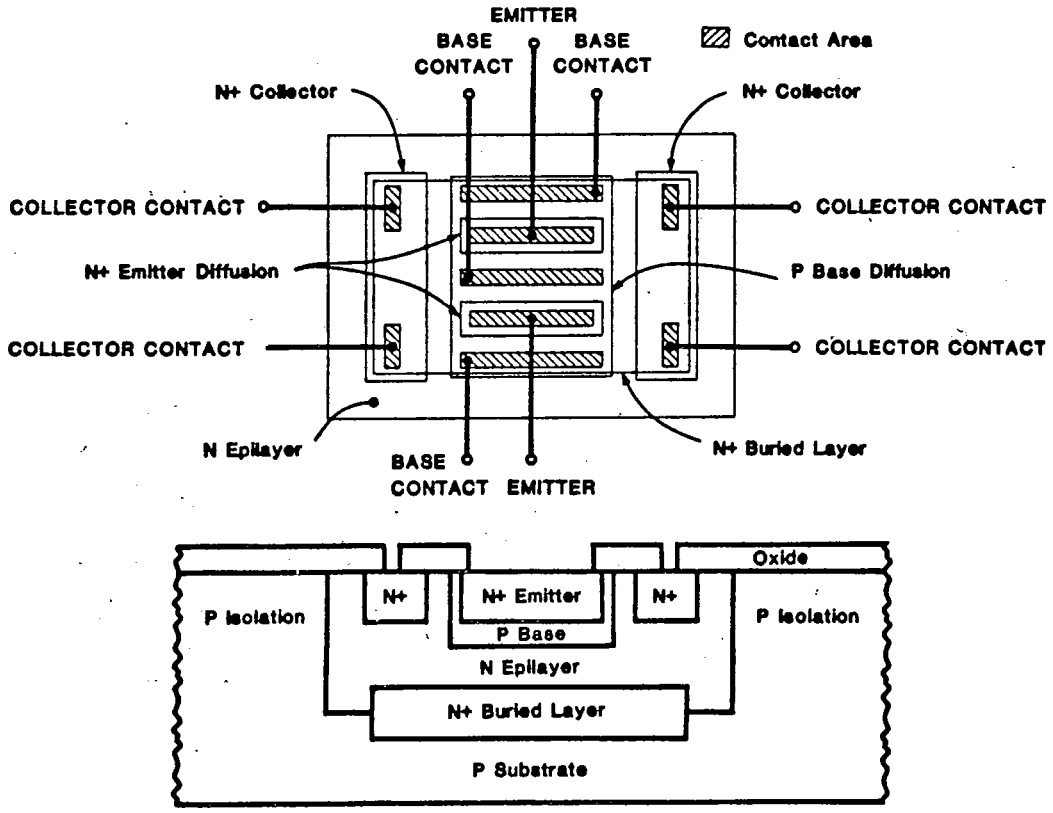
2) $h_{FE}$ matching is satisfied by $1-2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right| < \frac{h_{FE(2)}}{h_{FE(1)}} < 1+2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right|$ where $h_{FE(1)}$ and $h_{FE(2)}$ are any two current gains chosen from a population of like transistors on chip.

3) Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.

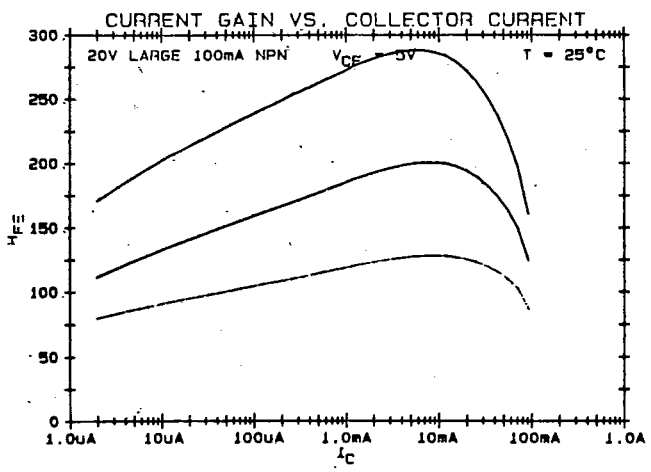
4) Matching of $V_{BE}$ is satisfied by $|V_{BE(2)}-V_{BE(1)}| < 2|\Delta V_{BE(MAX)}|$ where $V_{BE(1)}$ and $V_{BE(2)}$ are any two base-emitter voltages chosen from a population of like transistors on chip.

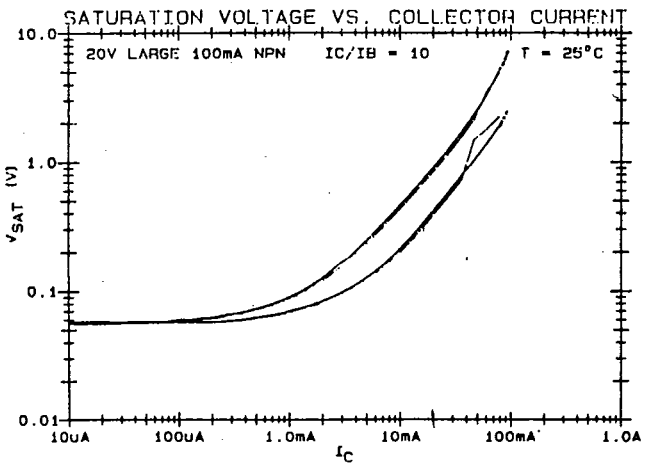
5) It is not recommended to operate the transistor in the saturation mode when only one collector contact or two collector contacts on the same N+ diffusion region are used, since a high saturation voltage is inevitable, especially at increased collector currents.

6) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.




Layout and Cross-Section of
Large 50mA (Per Emitter) Dual-Emitter NPN Transistor
(Not to Scale)



# 20V LARGE NPN TRANSISTOR

## 200mA HEX EMITTER

### GENERAL DESCRIPTION

The large 200mA NPN Transistor has a large emitter constructed with six fingers, in a double-comb shape, placed in a single base region. The base region has two base contacts in it and is serounded with a wrap-around N+ collector diffusion which also includes two collector contacts. This multiple contact structive permits a degree of flexibility in the layout process. However, best results are obtained when all collector contacts are connected together and all base contacts connected together respectively. This transistor is available in two versions, with and without a deep N+ diffusion in the collector region. The N+ diffusion reduces the saturation voltage and increases the current handling capability.

### FEATURES

Six-finger Emitter Structure
Dual Base Contacts
Dual Collector Contacts

### TYPICAL APPLICATIONS

Motor Drivers
Relay Drivers
Lamp and LED Drivers
Voltage Regulators
Power Darlingtons

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| DC Current Gain | $h_{FE}$ | $I_C$=100mA | $V_{CE}$=5V | (Note 1) | 80 | | 300 | |
| Matching of DC Current Gains | $\Delta h_{FE}$ | $I_C$=100mA | $V_{CE}$=5V | (Note 2) | | ±5 | ±10 | % |
| Temperature Coefficient of $h_{FE}$ | $\Delta h_{FE}/\Delta T$ | $I_C$=100mA | -55°C < $T_A$ < 25°C | | | 0.5 | | %/°C |
| | | | 25°C < $T_A$ < 75°C | | | ±0.3 | | |
| | | | 75°C < $T_A$ < 125°C | | | -0.5 | | |
| Collector-Base Leakage Current | $I_{CBO}$ | $V_{CB}$=20V | $T_A$=25°C | (Note 3) | | 0.05 | 0.5 | nA |
| | | | $T_A$=125°C | (Note 3) | | 5 | 50 | |
| Collector-Emitter Leakage Current | $I_{CEO}$ | $V_{CE}$=20V | $T_A$=25°C | (Note 3) | | 0.5 | 5 | nA |
| | | | $T_A$=125°C | (Note 3) | | 1 | 10 | µA |
| Collector-Emitter Breakdown Voltage | $LV_{CEO}$ | $I_C$=1mA | | | 20 | | | V |
| Collector-Base Breakdown Voltage | $BV_{CBO}$ | $I_C$=100µA | | | 30 | | | V |
| Emitter-Base Breakdown Voltage | $BV_{EBO}$ | $I_E$=10µA | | | 6.25 | | 7.25 | V |
| Collector-Substrate Breakdown Voltage | $BV_{CS}$ | $I_C$=10µA | | | 20 | | | V |
| Base-Emitter Forward Voltage | $V_{BE}$ | $V_{CE}$=5V | $\|I_E\|$=10mA | | 0.65 | | 0.77 | V |
| | | | $\|I_E\|$=100mA | | 0.73 | | 0.85 | |
| Matching of Base-Emitter Forward Voltages | $\Delta V_{BE}$ | $\|I_E\|$=10mA | $V_{CE}$=5V | (Note 4) | | ±2 | ±6 | mV |
| Temperature Coefficient of $V_{BE}$ | $\Delta V_{BE}/\Delta T$ | $\|I_E\|$=10mA | $V_{CE}$=5V | | | -1.8 | | mV/°C |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $(I_C/I_B)$=10 | $I_C$=10mA | One Collector Contact (One Diffusion Region) | | 0.16 | 0.24 | V |
| | | | | Two Collector Contacts (One Diffusion Region) | | 0.12 | 0.17 | |
| | | | $I_C$=100mA | One Collector Contact (One Diffusion Region) | | 1.4 | 2 | |
| | | | | Two Collector Contacts (One Diffusion Region) | | 0.9 | 1.2 | |
| Maximum Collector Current | $I_{C(MAX)}$ | $P_{D(MAX)}$=700mW | | | | | 300 | mA |
| Cutoff Frequency | $f_T$ | $I_C$=50mA | $V_{CE}$=5V | | | 500 | | MHz |

LARGE NPN TRANSISTOR (CONTINUED)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Storage Time | $t_S$ | $(I_C/I_B)=10$ $R_B=75\Omega$ | $I_C$=10mA | | 30 | | ns |
| | | | $I_C$=100mA | | 150 | | |
| Emitter-Base Capacitance | $C_{EB}$ | $V_{EB}$=0V | (Note 5) | | 13.5 | | pF |
| Collector-Base Capacitance | $C_{CB}$ | $V_{CB}$=0V | (Note 5) | | 9 | | pF |
| Collector-Substrate Capacitance | $C_{CS}$ | $V_{CS}$=0V | (Note 5) | | 16.5 | | pF |

Notes:

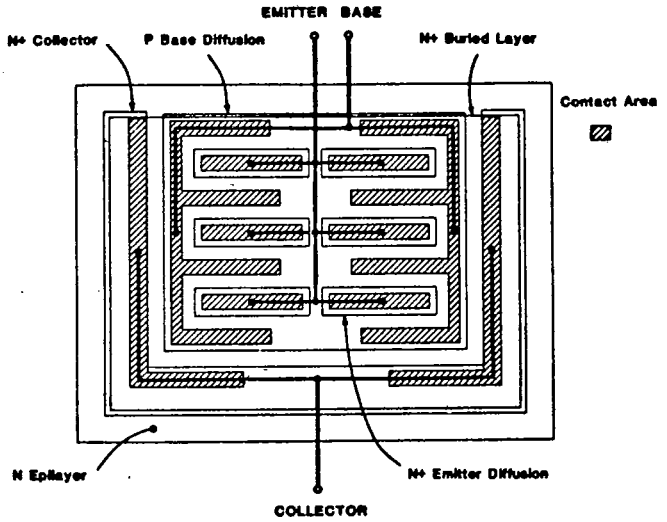
1) All collector contacts connected in parallel.

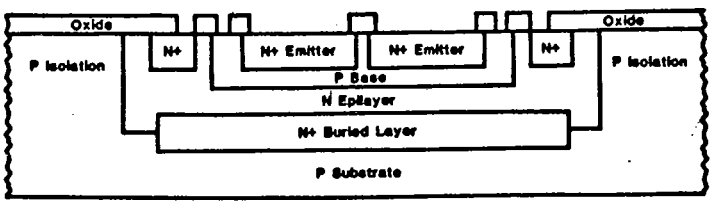
2) $h_{FE}$ matching is satisfied by $1-2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right| < \frac{h_{FE(2)}}{h_{FE(1)}} < 1+2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right|$ where $h_{FE(1)}$ and $h_{FE(2)}$ are any two current gains chosen from a population of like transistors on chip.

3) Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.

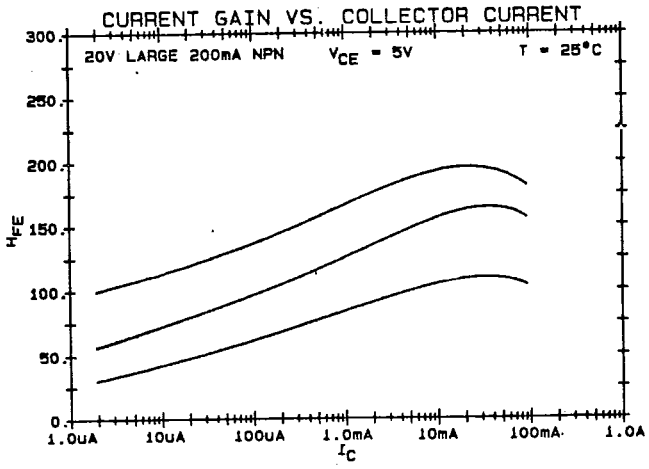
4) Matching of $V_{BE}$ is satisfied by $|V_{BE(2)}-V_{BE(1)}| < 2|\Delta V_{BE(MAX)}|$ where $V_{BE(1)}$ and $V_{BE(2)}$ are any two base-emitter voltages chosen from a population of like transistors on chip.

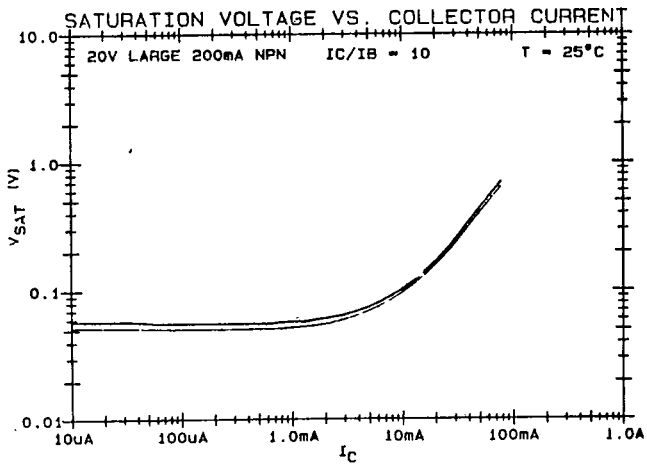
5) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.




Layout and Cross-Section of Large 200mA NPN Transistor
(Not to Scale)


CURRENT GAIN VS. COLLECTOR CURRENT
20V LARGE 200mA NPN
$V_{CE}$ = 5V
T = 25°C
300
250
200
150
100
50
0
$H_{FE}$
1.0uA
10uA
100uA
1.0mA
10mA
100mA
1.0A
$I_C$


SATURATION VOLTAGE VS. COLLECTOR CURRENT
20V LARGE 200mA NPN
IC/IB = 10
T = 25°C
10.0
1.0
0.1
0.01
$V_{SAT}$ (V)
10uA
100uA
1.0mA
10mA
100mA
1.0A
$I_C$

# 20V LATERAL PNP TRANSISTOR
## 1mA QUAD COLLECTOR

**GENERAL DESCRIPTION**

The lateral PNP transistor has an oval-shaped, P-type emitter, surrounded by four P-type collector diffusions in a single epi base region. The base is made with an N+ diffusion with two base contacts in it. All four collectors should be connected together when a single collector transistor is required. When current ratios are important, such as for multiple current sources, the collectors can be used individually. Unused collectors must be connected to the substrate or any other potential that will ensure that the transistor does not saturate.

**FEATURES**

Quad Collectors
Matched $V_{BE}$ and $h_{FE}$ Transistor Parameters

**TYPICAL APPLICATIONS**

Current Sources
Active Loads
Level Shifters
Biasing Stages
Amplifiers

0.25mA (PER COLLECTOR) QUAD-COLLECTOR LATERAL PNP TRANSISTOR
(EACH COLLECTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| DC Current Gain | $h_{FE}$ | $V_{CE}$=-5V | $I_C$=-25μA One Collector (Note 1) | 5 | | 37.5 | |
| | | | $I_{C(TOTAL)}$=-50μA Two Collectors Connected in Parallel (Note 1) | 10 | | 75 | |
| | | | $I_{C(TOTAL)}$=-100μA Four Collectors Connected in Parallel | 20 | | 150 | |
| Matching of DC Current Gains | $\Delta h_{FE}$ | $I_C$=-100μA $V_{CE}$=-5V (Note 2) | | | ±5 | ±15 | % |
| Temperature Coefficient of $h_{FE}$ | $\Delta h_{FE}/\Delta T$ | $I_C$=-100μA -55°C < $T_A$ < 125°C | | | -0.1 | | %/°C |
| Collector-Base Leakage Current | $I_{CBO}$ | $V_{CB}$=-20V | $T_A$=25°C (Note 3) | | -0.01 | -0.1 | nA |
| | | | $T_A$=125°C (Note 3) | | -1 | -10 | |
| Collector-Emitter Leakage Current | $I_{CEO}$ | $V_{CE}$=-20V | $T_A$=25°C (Note 3) | | -0.05 | -0.5 | nA |
| | | | $T_A$=125°C (Note 3) | | -25 | -250 | |
| Collector-Emitter Breakdown Voltage | $BV_{CEO}$ | $I_C$=-100μA | | -20 | | | V |
| Collector-Base Breakdown Voltage | $BV_{CBO}$ | $I_C$=-100μA | | -30 | | | V |
| Emitter-Base Breakdown Voltage | $BV_{EBO}$ | $I_E$=-100μA | | -30 | | | V |
| Base-Substrate Breakdown Voltage | $BV_{BS}$ | $I_B$=10μA | | 20 | | | V |
| Base-Emitter Forward Voltage | $V_{BE}$ | $I_E$=100μA $V_{CE}$=-5V | | -0.61 | | -0.73 | V |
| Matching of Base-Emitter Forward Voltages | $\Delta V_{BE}$ | $I_E$=100μA $V_{CE}$=-5V (Note 4) | | | ±2 | ±6 | mV |
| Temperature Coefficient of $V_{BE}$ | $\Delta V_{BE}/\Delta T$ | $I_E$=100μA $V_{CE}$=-5V | | | 1.8 | | mV/°C |

QUAD-COLLECTOR LATERAL PNP TRANSISTOR (CONTINUED)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $(I_{C(TOTAL)}/I_B)=1$ | $I_C=-25\mu A$ One Collector (Notes 1,5) | | -0.1 | -0.18 | V |
| | | | $I_{C(TOTAL)}=-50\mu A$ Two Collectors Connected in Parallel (Notes 1,5) | | | | |
| | | | $I_{C(TOTAL)}=-100\mu A$ Four Collectors Connected in Parallel (Note 5) | | | | |
| Maximum Usable Collector Current | $I_{C(MAX)}$ | (Per Collector) | | | | -0.5 | mA |
| Cutoff Frequency | $f_T$ | $I_{C(TOTAL)}=-100\mu A$ $V_{CE}=-5V$ | Four Collectors Connected in Parallel | | 5 | | MHz |
| Storage Time | $\tau_S$ | $(I_{C(TOTAL)}/I_B)=1$ | $I_{C(TOTAL)}=-100\mu A$ Four Collectors Connected in Parallel | | 75 | | ns |
| | | $R_B=750\Omega$ | $I_{C(TOTAL)}=-1mA$ Four Collectors Connected in Parallel | | 130 | | |
| Emitter-Base Capacitance | $C_{EB}$ | $V_{EB}=0V$ | (Note 6) | | 0.2 | | pF |
| Collector-Base Capacitance | $C_{CB}$ | $V_{CB}=0V$ | (Note 6) | | 0.4 | | pF |
| Base-Substrate Capacitance | $C_{BS}$ | $V_{BS}=0V$ | (Note 6) | | 3.5 | | pF |

Notes:

1) With the other collectors grounded.

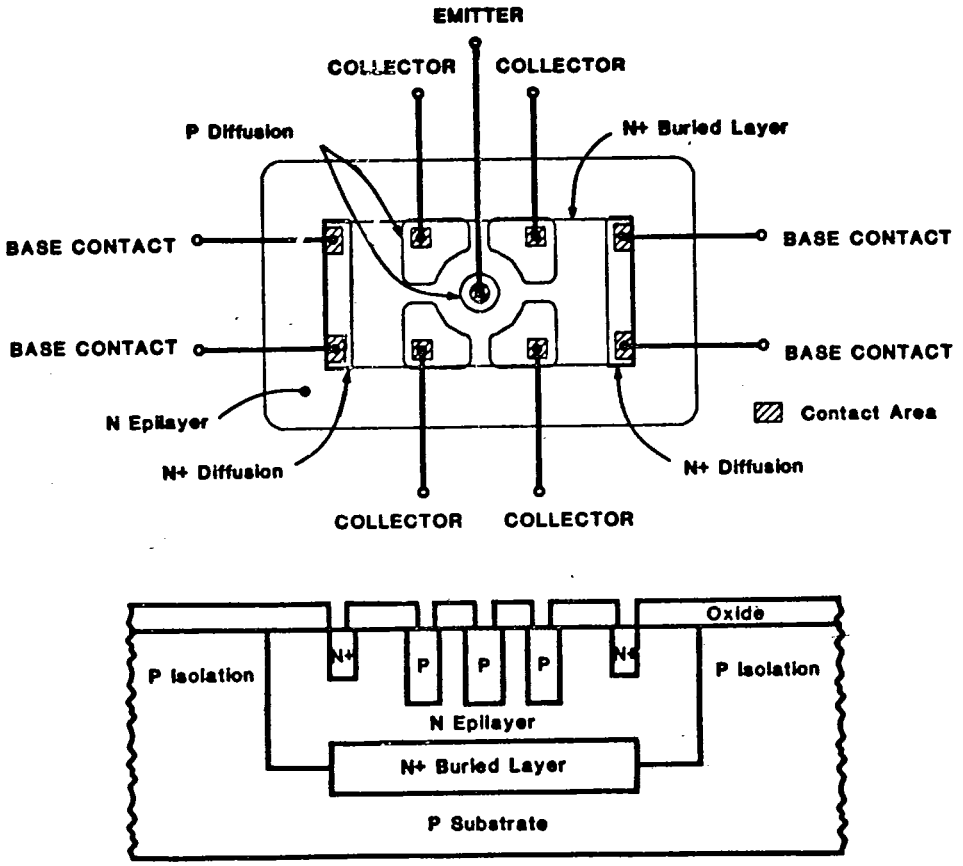
2) $h_{FE}$ matching is satisfied by $1-2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right| < \frac{h_{FE(2)}}{h_{FE(1)}} < 1+2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right|$ where $h_{FE(1)}$ and $h_{FE(2)}$ are any two current gains chosen from a population of like transistors on chip.

3) Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.

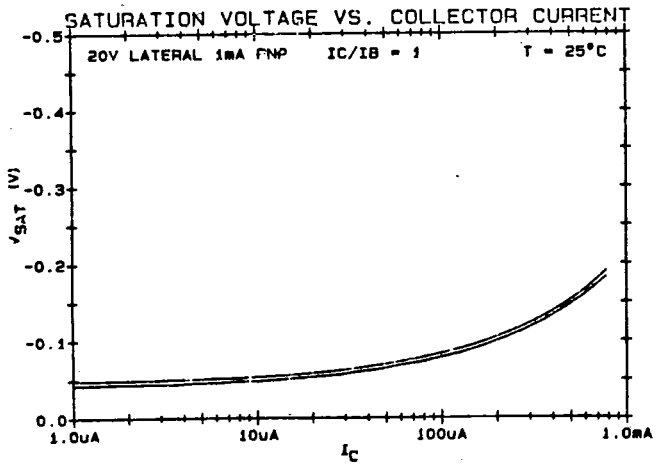
4) Matching of $V_{BE}$ is satisfied by $|V_{BE(2)}-V_{BE(1)}| < 2|\Delta V_{BE(MAX)}|$ where $V_{BE(1)}$ and $V_{BE(2)}$ are any two base-emitter voltages chosen from a population of like transistors on chip.

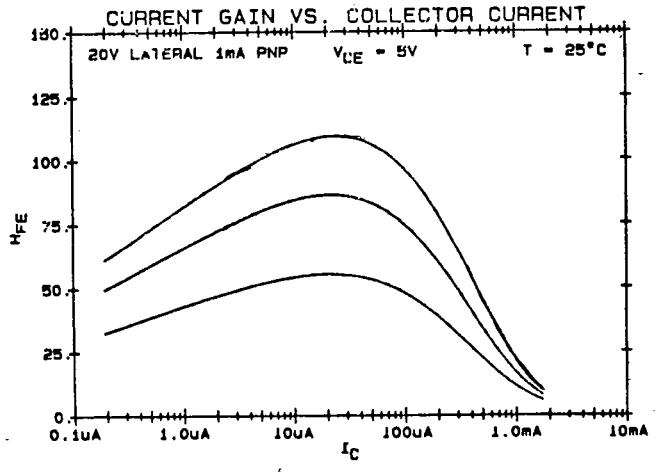
5) It is not advisable to operate the lateral PNP transistor in the saturation mode since the parasitic vertical substrate transistor (related to the lateral transistor) becomes heavily active.

6) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.




Layout and Cross-Section of
0.25mA (Per Collector) Quad-Collector Lateral PNP Transistor
(Not to Scale)



## LATERAL PNP DIODE (EMITTER-BASE JUNCTION OF TRANSISTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Forward Voltage Drop | $V_F$ | $I_F$=100µA | | | 0.61 | | 0.73 | V |
| | | $I_F$=1mA | | | 0.73 | | 0.85 | |
| | | $I_F$=10mA | | (Note 1) | | 1.1 | | |
| Matching of Forward Voltages | $\Delta V_F$ | $I_F$=1mA | | (Note 2) | | ±2 | ±6 | mV |
| Temperature Coefficient of $V_F$ | $\Delta V_F/\Delta T$ | $I_F$=1mA | | | | -1.8 | | mV/°C |
| Leakage Current | $I_O$ | $V_R$=20V | $T_A$=25°C | (Note 3) | | 0.1 | | nA |
| | | | $T_A$=125°C | (Note 3) | | 10 | | |
| Breakdown Voltage | $BV_D$ | $I_R$=100µA | | | 30 | | | V |
| Maximum Diode Current | $I_{F(MAX)}$ | | | (Note 1) | | | 10 | mA |
| Junction Capacitance | $C_J$ | $V_D$=0V | | (Note 4) | | 0.2 | | pF |

Notes:

1) The lateral PNP diode, like the lateral PNP transistor, has a parasitic vertical substrate current that becomes dominant at high operating current. This substrate loss current becomes comparable to the diode forward current at about 5mA.

2) Matching of $V_F$ is satisfied by $|V_{F(2)}-V_{F(1)}| < 2|\Delta V_{F(MAX)}|$ where $V_{F(1)}$ and $V_{F(2)}$ are any two forward voltages chosen from a population of like diodes on chip.

3) Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.

4) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.

# 20V DUAL LATERAL PNP TRANSISTOR

## 1mA QUAD COLLECTOR

**GENERAL DESCRIPTION**

The lateral PNP transistor has an oval shaped, p-type emitter surrounded by four P-type collector diffusions in a single epi base region. The two transistors are located in a common isolation tub and share the same base region. The base is made with an N+ diffusion with two base contacts in it. All four collectors should be connected together when a single collector transistor is required. When current ratios are important, such as for multiple current sources, the collectors can be connected individually.

Unused collectors must be connected to the substrate or any other potential that will ensure that the transistor does not saturate.

**FEATURES**

Quad Collectors
Matched $V_{BE}$ and $h_{FE}$ Transistor Parameters

**TYPICAL APPLICATIONS**

Current Sources
Active Loads
Level Shifters
Biasing Stages
Amplifiers

0.25mA (PER COLLECTOR) QUAD-COLLECTOR LATERAL PNP TRANSISTOR

(EACH COLLECTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UN TS |
|---|---|---|---|---|---|---|---|
| DC Current Gain | $h_{FE}$ | $V_{CE}$=-5V | $I_C$=-25μA One Collector (Note 1) | 5 | | 37.5 | |
| | | | $I_{C(TOTAL)}$=-50μA Two Collectors Connected in Parallel (Note 1) | 10 | | 75 | |
| | | | $I_{C(TOTAL)}$=-100μA Four Collectors Connected in Parallel | 20 | | 150 | |
| Matching of DC Current Gains | $\Delta h_{FE}$ | $I_C$=-100μA $V_{CE}$=-5V (Note 2) | | | ±5 | ±15 | % |
| Temperature Coefficient of $h_{FE}$ | $\Delta h_{FE}/\Delta T$ | $I_C$=-100μA -55°C < $T_A$ < 125°C | | | -0.1 | | %/°C |
| Collector-Base Leakage Current | $I_{CBO}$ | $V_{CB}$=-20V | $T_A$=25°C (Note 3) | | -0.01 | -0.1 | nA |
| | | | $T_A$=125°C (Note 3) | | -1 | -10 | |
| Collector-Emitter Leakage Current | $I_{CEO}$ | $V_{CE}$=-20V | $T_A$=25°C (Note 3) | | -0.05 | -0.5 | nA |
| | | | $T_A$=125°C (Note 3) | | -25 | -250 | |
| Collector-Emitter Breakdown Voltage | $BV_{CEO}$ | $I_C$=-100μA | | -20 | | | V |
| Collector-Base Breakdown Voltage | $BV_{CBO}$ | $I_C$=-100μA | | -30 | | | V |
| Emitter-Base Breakdown Voltage | $BV_{EBO}$ | $I_E$=-100μA | | -30 | | | V |
| Base-Substrate Breakdown Voltage | $BV_{BS}$ | $I_B$=10μA | | 20 | | | V |
| Base-Emitter Forward Voltage | $V_{BE}$ | $I_E$=100μA $V_{CE}$=-5V | | -0.61 | | -0.73 | V |
| Matching of Base-Emitter Forward Voltages | $\Delta V_{BE}$ | $I_E$=100μA $V_{CE}$=-5V (Note 4) | | | ±2 | ±6 | mV |
| Temperature Coefficient of $V_{BE}$ | $\Delta V_{BE}/\Delta T$ | $I_E$=100μA $V_{CE}$=-5V | | | 1.8 | | mV/°C |

QUAD-COLLECTOR LATERAL PNP TRANSISTOR (CONTINUED)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $(I_{C(TOTAL)}/I_B)=1$ | $I_C=-25\mu A$ One Collector (Notes 1,5) | | -0.1 | -0.18 | V |
| | | | $I_{C(TOTAL)}=-50\mu A$ Two Collectors Connected in Parallel (Notes 1,5) | | | | |
| | | | $I_{C(TOTAL)}=-100\mu A$ Four Collectors Connected in Parallel (Note 5) | | | | |
| Maximum Usable Collector Current | $I_{C(MAX)}$ | (Per Collector) | | | | -0.5 | mA |
| Cutoff Frequency | $f_T$ | $I_{C(TOTAL)}=-100\mu A$ $V_{CE}=-5V$ | Four Collectors Connected in Parallel | | 5 | | MHz |
| Storage Time | $t_S$ | $(I_{C(TOTAL)}/I_B)=1$ | $I_{C(TOTAL)}=-100\mu A$ Four Collectors Connected in Parallel | | 75 | | ns |
| | | $R_B=750\Omega$ | $I_{C(TOTAL)}=-1mA$ Four Collectors Connected in Parallel | | 130 | | |
| Emitter-Base Capacitance | $C_{EB}$ | $V_{EB}=0V$ | (Note 6) | | 0.2 | | pF |
| Collector-Base Capacitance | $C_{CB}$ | $V_{CB}=0V$ | (Note 6) | | 0.4 | | pF |
| Base-Substrate Capacitance | $C_{BS}$ | $V_{BS}=0V$ | (Notes 6,7) | | 3.5 | | pF |

Notes:

1) With the other collectors grounded.

2) $h_{FE}$ matching is satisfied by $1-2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right| < \frac{h_{FE(2)}}{h_{FE(1)}} < 1+2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right|$ where $h_{FE(1)}$ and $h_{FE(2)}$ are any two current gains chosen from a population of like transistors on chip.

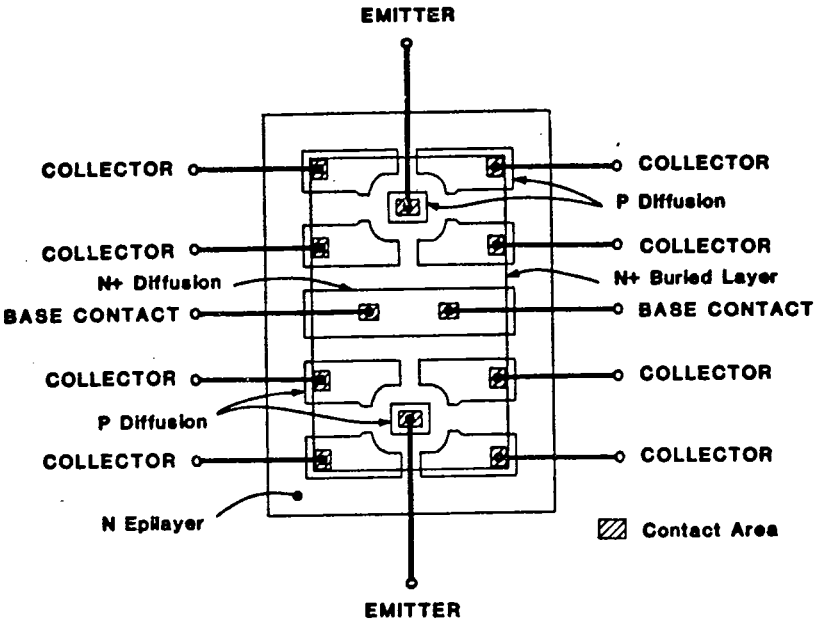
3) Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.

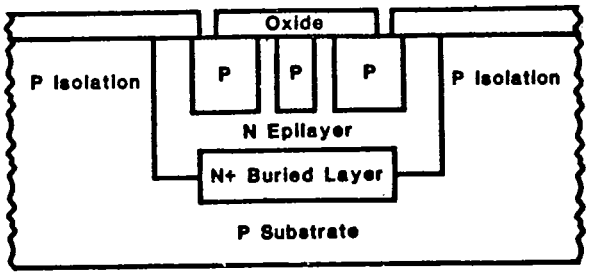
4) Matching of $V_{BE}$ is satisfied by $|V_{BE(2)}-V_{BE(1)}| < 2|\Delta V_{BE(MAX)}|$ where $V_{BE(1)}$ and $V_{BE(2)}$ are any two base-emitter voltages chosen from a population of like transistors on chip.

5) It is not advisable to operate the lateral PNP transistor in the saturation mode since the parasitic vertical substrate transistor (related to the lateral transistor) becomes heavily active.

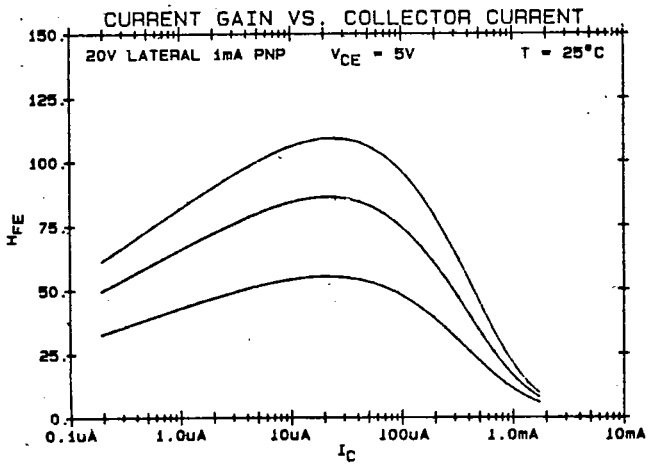
6) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.

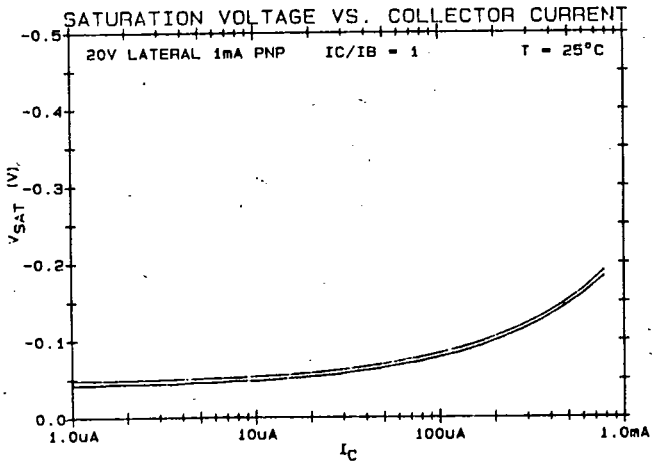
7) On the HTL-I2OL chip, two quad-collector lateral PNP transistors are placed in one isolation bucket. The total base-substrate capacitance must be considered even when only one of the transistors is being used.




Layout and Cross-Section of
0.25mA (Per Collector) Quad-Collector Lateral PNP Transistor
(Not to Scale)



## LATERAL PNP DIODE (EMITTER-BASE JUNCTION OF TRANSISTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Forward Voltage Drop | $V_F$ | $I_F$=100µA | | | 0.61 | | 0.73 | V |
| | | $I_F$=1mA | | | 0.73 | | 0.85 | |
| | | $I_F$=10mA | | (Note 1) | | 1.1 | | |
| Matching of Forward Voltages | $\Delta V_F$ | $I_F$=1mA | | (Note 2) | | ±2 | ±6 | mV |
| Temperature Coefficient of $V_F$ | $\Delta V_F/\Delta T$ | $I_F$=1mA | | | | -1.8 | | mV/°C |
| Leakage Current | $I_O$ | $V_R$=20V | $T_A$=25°C | (Note 3) | | 0.1 | | nA |
| | | | $T_A$=125°C | (Note 3) | | 10 | | |
| Breakdown Voltage | $BV_D$ | $I_R$=100µA | | | 30 | | | V |
| Maximum Diode Current | $I_{F(MAX)}$ | | | (Note 1) | | | 10 | mA |
| Junction Capacitance | $C_J$ | $V_D$=0V | | (Note 4) | | 0.2 | | pF |

Notes:

1) The lateral PNP diode, like the lateral PNP transistor, has a parasitic vertical substrate current that becomes dominant at high operating current. This substrate loss current becomes comparable to the diode forward current at about 5mA.

2) Matching of $V_F$ is satisfied by $|V_{F(2)}-V_{F(1)}| < 2|\Delta V_{F(MAX)}|$ where $V_{F(1)}$ and $V_{F(2)}$ are any two forward voltages chosen from a population of like diodes on chip.

3) Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.

4) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.

# 20V P-TYPE DIFFUSED RESISTORS

## 200Ω, 450Ω, 900Ω, 1.8KΩ, 3.6KΩ

**GENERAL DESCRIPTION**

The P-type diffused resistors are made during the base diffusion step in the integrated circuit process. They exhibit excellent ratio matching properties which are primerily dependent on the masking accuracy in the fabrication process. However, the obsolute values are not as accurate as they are directly related to the tolerances in the diffusion process.

**FEATURES**

Matched Resistor Ratios

**TYPICAL APPLICATIONS**

Analog and Digital Circuitry

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Absolute Values | R | $V_R$=5V | | | | Ω |
| 200Ω | | | | 200 | 250 | |
| 450Ω | | | 337.5 | 450 | 562.5 | |
| 900Ω | | | 675 | 900 | 1125 | |
| 1.8KΩ | | | 1350 | 1800 | 2250 | |
| 3.6KΩ | | | 2700 | 3600 | 4500 | |
| Epi (Vcc Terminal)-Substrate Breakdown Voltage | $BV_{NS}$ | $I_N$=10μA | 20 | | | V |
| Epi (Vcc Terminal)-Resistor Breakdown Voltage | $BV_{NR}$ | $I_N$=100μA | 30 | | | V |
| Resistor-Substrate Breakdown Voltage | $BV_{RS}$ | $I_R$=10μA | 20 | | | V |
| Temperature Coefficient of R | ΔR/ΔT | $V_R$=5V, -55°C < $T_A$ < -25°C | | -0.02 | | %/°C |
| | | $V_R$=5V, -25°C < $T_A$ < 25°C | | 0.06 | | |
| | | $V_R$=5V, 25°C < $T_A$ < 125°C | | 0.13 | | |
| Matching of Equal Design Value Resistors | ΔR(1:1) | $V_R$=5V, $R_2$=$R_1$ (Notes 1,2) | | | ±3 | % |
| Ratio Matching of Unequal Design Value Resistors | ΔR(1:2) | $V_R$=5V, $R_2$=2$R_1$ (Notes 1,2) | | | ±4 | % |
| | ΔR(1:4) | $V_R$=5V, $R_2$=4$R_1$ (Notes 1,2) | | | ±5 | |
| | ΔR(1:8) | $V_R$=5V, $R_2$=8$R_1$ (Notes 1,2) | | | ±6 | |
| Maximum Power Dissipation | $P_{D(MAX)}$ | | | | 300 | mW |
| Epi (Vcc Terminal)-Resistor Capacitance | $C_{NR}$ | $V_{NR}$=0V (Notes 3,4) | | | | pF |
| 200Ω | | | | 1.1 | | |
| 450Ω | | | | 0.5 | | |
| 900Ω | | | | 0.6 | | |
| 1.8KΩ | | | | 0.9 | | |
| 3.6KΩ | | | | 1.8 | | |

Notes:

1) Resistor ratio matching is satisfied by

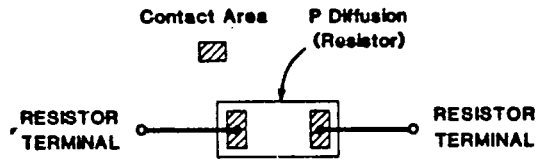
$$k\left(1-2\left|\frac{\Delta R(MAX)}{100\%}\right|\right) < \frac{R_2}{R_1} < k\left(1+2\left|\frac{\Delta R(MAX)}{100\%}\right|\right)$$

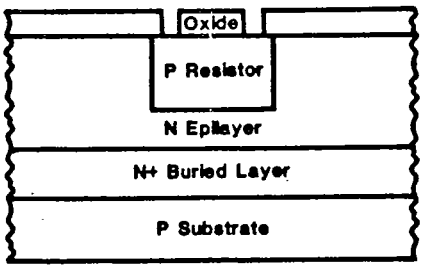
where k is the resistor ratio of the nominal values, and $R_1$ and $R_2$ are any two resistors chosen from these populations on chip.

2) These particular matching parameters apply to the various resistor ratios on chip.

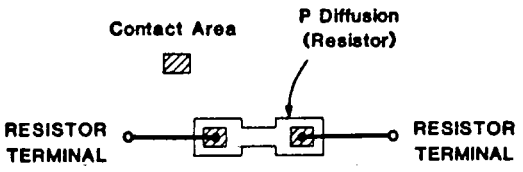
3) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.

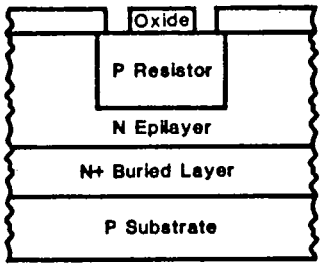
4) These capacitances refer to each individual resistor; however, most resistors on chip are strung together, thus presenting a higher total capacitance for each resistor group.



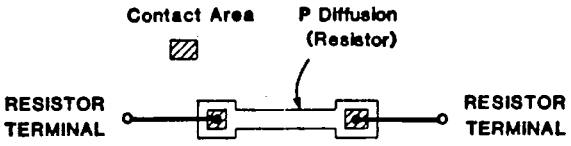



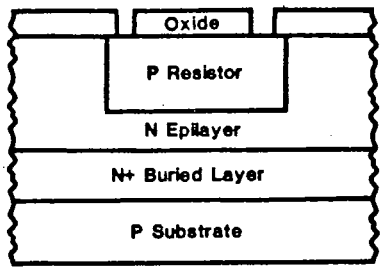

Layout and Cross-Section of 200Ω P-Type Diffused Resistor (Not to Scale)



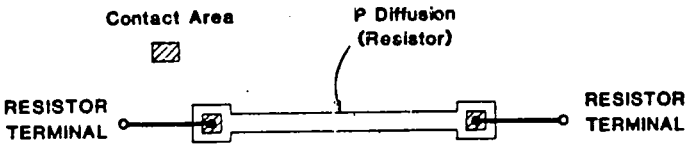



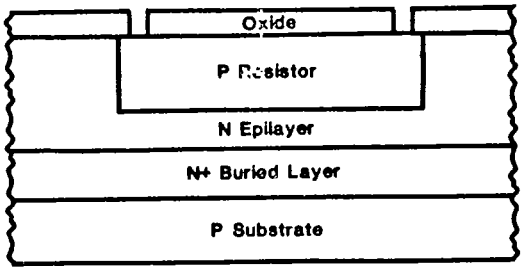

Layout and Cross-Section of 450Ω P-Type Diffused Resistor (Not to Scale)



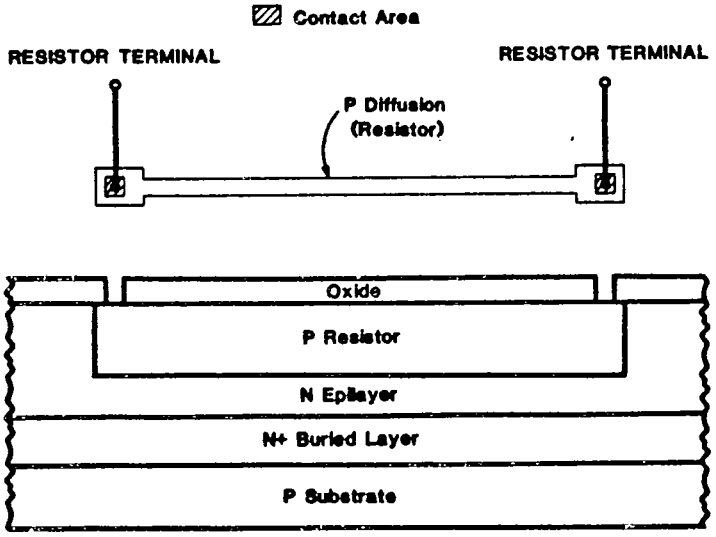




Layout and Cross-Section of 900Ω P-Type Diffused Resistor (Not to Scale)

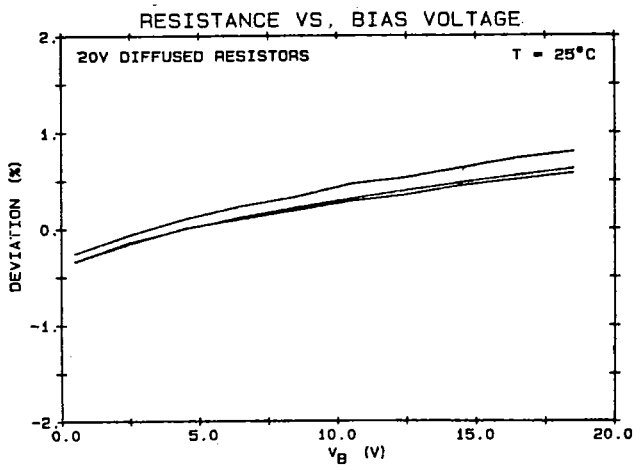



Layout and Cross-Section of 1.8KΩ P-Type Diffused Resistor (Not to Scale)




Layout and Cross-Section of 3.6KΩ P-Type
Diffused Resistor (Not to Scale)



# 20V BASE PINCH RESISTORS

## 30KΩ, 100KΩ

**GENERAL DESCRIPTION**

The base pinch resistors have an N+ gate diffusion that overlaps the P diffusion which forms the resistor body. In most cases the gate is internally connected to one of the resistor terminals. This terminal is normally designed and layed out as the most positive node of the resistor. The layout sheets indicate this terminal with a "+" sign. The voltage drop across the resistor should not exceed 6V to prevent breakdown. Pinch resistors can be connected in series when a higher operating voltage is desired, providing that each of the resistor does not sustain more than 6V. On some chips, the 30KΩ and the 100KΩ resistors are located in a single isolation tub and share a common gate connection. Each of these resistor can also sustain 6V before breakdown occures. It should be noted that the pinch resistors are non-linear and have a very strong voltage dependency.

**FEATURES**

High Resistor Values

**TYPICAL APPLICATIONS**

Current Sources
General Purpose Circuitry

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

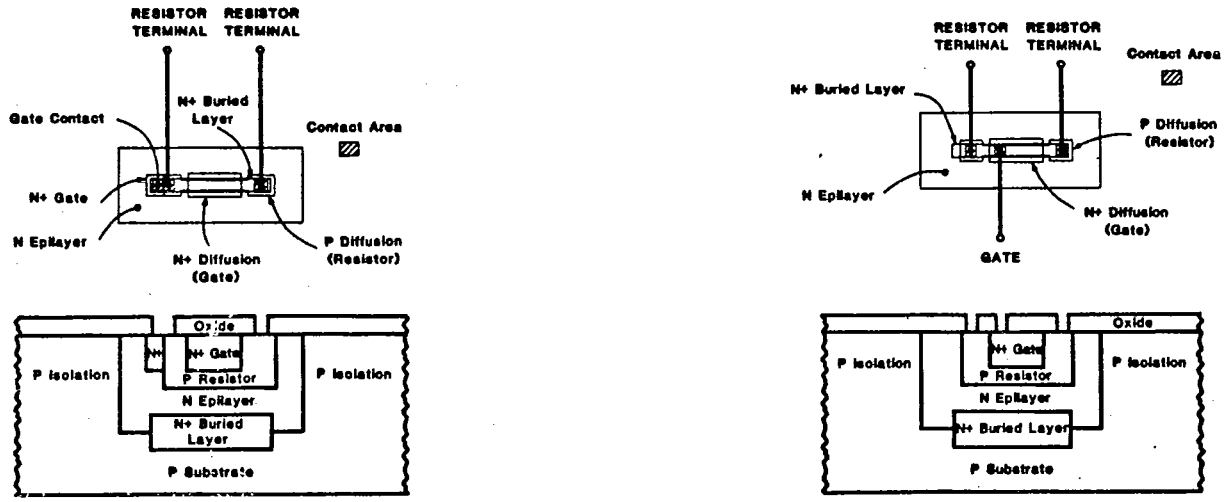
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Absolute Values<br>30KΩ<br>100KΩ | R | $I_R$=10μA | <br>15<br>50 | <br>30<br>100 | <br>60<br>200 | KΩ |
| Matching of Resistor Values | ΔR | $I_R$=10μA (Note 1) | | ±5 | | % |
| Breakdown Voltage (Across Resistor Terminals) | $BV_R$ | $I_R$=0.5mA (For 30KΩ Resistor) | 6 | | | V |
| | | $I_R$=0.15mA (For 100KΩ Resistor) | 6 | | | |
| Resistor-Substrate Breakdown Voltage | $BV_{RS}$ | $I_R$=10μA | 20 | | | V |
| Temperature Coefficient of R | ΔR/ΔT | -55°C < $T_A$ < 125°C | | 0.5 | | %/°C |
| Maximum Power Dissipation | $P_{D(MAX)}$ | | | | 200 | mW |
| Resistor-Substrate Capacitance<br>30KΩ<br>100KΩ | $C_{RS}$ | $V_{RS}$=0V (Notes 2,3) | | <br>2.6<br>6.8 | | pF |

Notes:

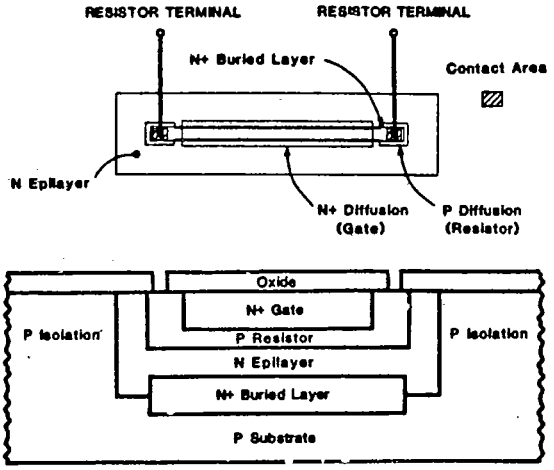
1) Resistor matching is satisfied by $1-2\left|\frac{\Delta R(MAX)}{100\%}\right| < \frac{R_2}{R_1} < 1+2\left|\frac{\Delta R(MAX)}{100\%}\right|$ where $R_1$ and $R_2$ are any two resistors chosen from a population of the same nominal value on chip.

2) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.

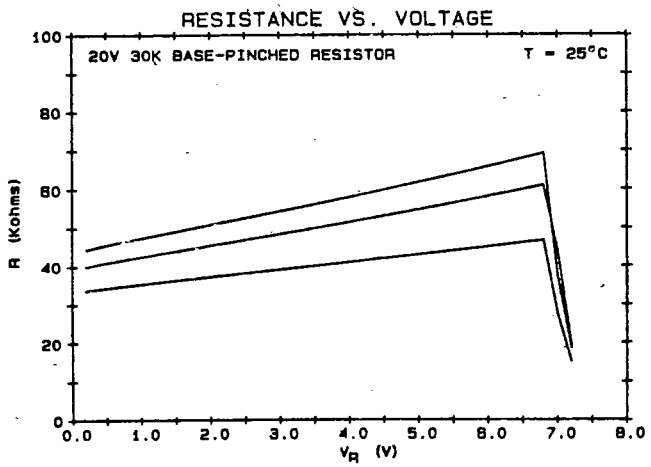
3) On the MCE-A20A chip, these two base pinch resistors are connected in series so that the total capacitance must be considered even when only one of the resistors is being used.

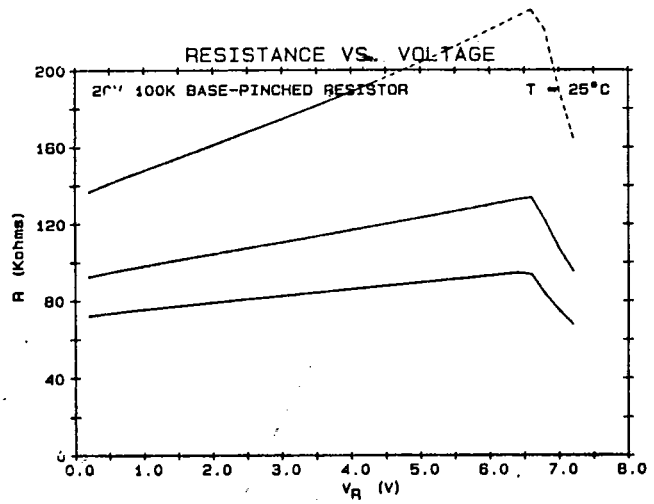



Layout and Cross-Section of 30KΩ Base Pinch Resistor
(Not to Scale)




Layout and Cross-Section of 100KΩ Base Pinch Resistor
(Not to Scale)



# 20V BASE PINCH RESISTORS

## DUAL 60KΩ

**GENERAL DESCRIPTION**

The base pinch resistors have an N+ gate diffusion that overlaps the P diffusion which forms the resistor body. Both resistors are located in a single isolation tub and share a single N+ gate diffusion which has two gate contacts in it. The two resistors can be connected in series or in parallel and one of the gate contacts must be connected to the most positive node of the resistor combination. The voltage drop accross the resistor combination must never be greater than 6V to prevent breakdown. It is also possible to utilize only one of the resistors while the other resistor is left open. Since the N+ gate diffusion has two contacts in it, it can be used as a low resistance cross-under. It should be noted that the pinch resistors are non-linear and have a very strong voltage dependency.

**FEATURES**

High Resistor Values

**TYPICAL APPLICATIONS**

Current Sources
General Purpose Circuitry

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Absolute Value | R | $I_R$=10μA | 30 | 60 | 120 | KΩ |
| Matching of Resistor Values | ΔR | $I_R$=10μA (Note 1) | | ±5 | | % |
| Breakdown Voltage (Across Resistor Terminals) | $BV_R$ | $I_R$=0.3mA | 6 | | | V |
| Resistor-Substrate Breakdown Voltage | $BV_{RS}$ | $I_R$=10μA | 20 | | | V |
| Temperature Coefficient of R | ΔR/ΔT | -55°C < $T_A$ < 125°C | | 0.5 | | %/°C |
| Maximum Power Dissipation | $P_{D(MAX)}$ | | | | 200 | mW |
| Resistor Gate Capacitance | $C_{RG}$ | $V_{RG}$=0V (Notes 2,3) | | 1 | | pF |
| Resistor-Substrate Capacitance | $C_{RS}$ | $V_{RS}$=0V (Notes 2,4) | | 2.6 | | pF |

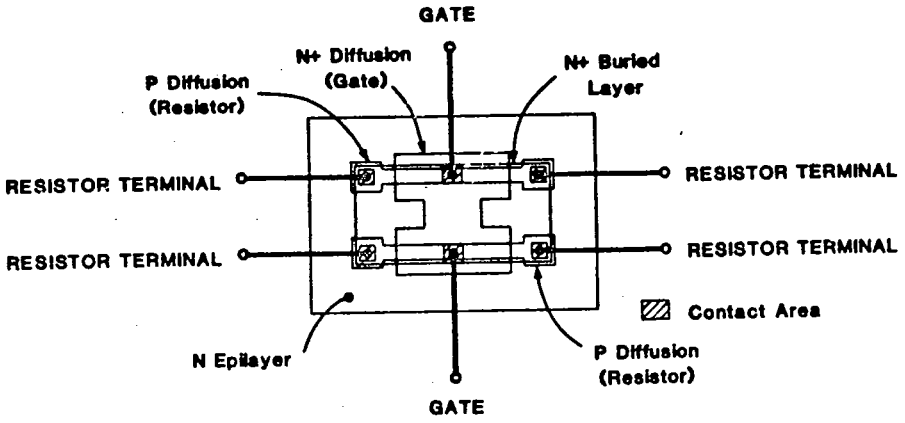
Notes:

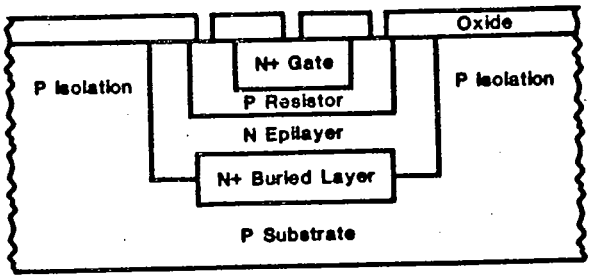
1) Resistor matching is satisfied by $1-2\left|\frac{\Delta R(MAX)}{100\%}\right| < \frac{R_2}{R_1} < 1+2\left|\frac{\Delta R(MAX)}{100\%}\right|$ where $R_1$ and $R_2$ are any two resistors chosen from a population of the same nominal value on chip.

2) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.

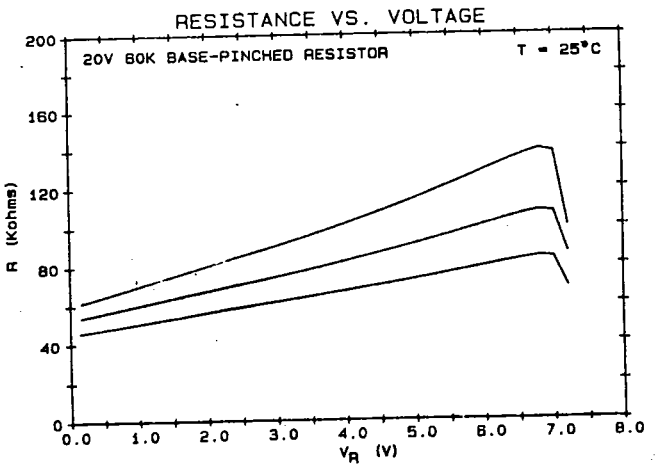
3) $C_{RG}$ is applicable only when the gate is not connected to one of the resistor terminals.

4) $C_{RS}$ is applicable only when the gate is connected to one of the resistor terminals.




Layout and Cross-Section of 60KΩ Base Pinch Resistor
(Not to Scale)



# 20V N+ CROSSUNDER
## 15Ω RESISTANCE

**GENERAL DESCRIPTION**

The 15Ω crossunder is made during the emitter diffusion step of the process. It exhibits a low sheet resistance and is primarily designed to be used as a crossunder connection to aid in the layout process. When layout permits, it is recommended to minimize the number of crossunders used to avoid possible performance degredation. Also, it is recommended not to run metal over the crossunder when metal is connected directly to a bonding pad, to prevent possible breakdown of the thin oxide layer over the crossunder.

**FEATURES**

Low Crossunder Resistance

**TYPICAL APPLICATIONS**

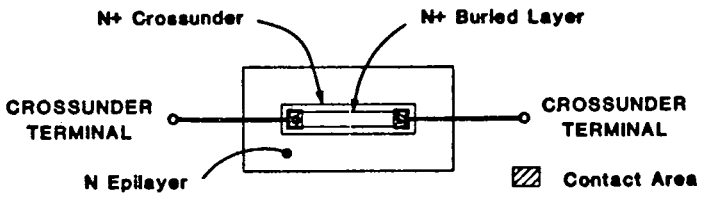
Crossunder Interconnections
Low Value Resistors

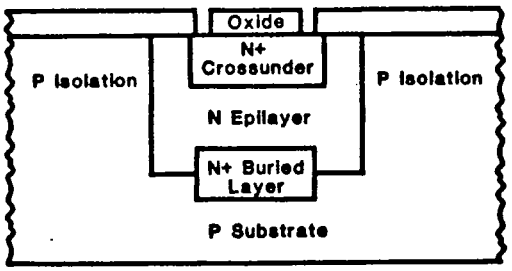
ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Absolute Values | R | $V_R$=5V | 11.25 | 15 | 18.75 | Ω |
| Crossunder-Substrate Breakdown Voltage | $BV_{RS}$ | $I_R$=10μA | 20 | | | V |
| Maximum Crossunder Current | $I_{R(MAX)}$ | | | | 40 | mA |
| Crossunder-Substrate Capacitance | $C_{RS}$ | $V_{RS}$=0V (Note 1) | | 1 | | pF |

Notes:

1) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.




Layout and Cross-Section of 15Ω N+ Crossunder
(Not to Scale)

# 40V SMALL NPN TRANSISTOR

## 10mA QUAD COLLECTOR CONTACT

### GENERAL DESCRIPTION

The small 10mA NPN transistor has two N+ diffusion regions in the collector area with two collector contacts in each of these diffusions. The contacts are normally connected together to reduce the series collector resistance as well as the saturation voltage. The small NPN transistor is available in two versions, with and without a deep N+ diffusion in the collector region. The deep N+ diffusion allows for an additional increase in the operating current.

### FEATURES

Four Collector Contacts
Matched $V_{BE}$ and $h_{FE}$ Transistor Parameters

### TYPICAL APPLICATIONS

Amplifiers
Comparators
Current Sources
Bias Circuits
Level Shifters
Emitter Followers
Diode Connected Transistors
Zener Diode Connections

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| DC Current Gain | $h_{FE}$ | $I_C$=1mA | $V_{CE}$=5V | (Note 1) | 80 | | 500 | |
| Matching of DC Current Gains | $\Delta h_{FE}$ | $I_C$=1mA | $V_{CE}$=5V | (Note 2) | | ±5 | ±10 | % |
| Temperature Coefficient of $h_{FE}$ | $\Delta h_{FE}/\Delta T$ | $I_C$=1mA | -55°C < $T_A$ < 125°C | | | 0.5 | | %/°C |
| Collector-Base Leakage Current | $I_{CBO}$ | $V_{CB}$=40V | $T_A$=25°C | (Note 3) | | 0.02 | 0.2 | nA |
| | | | $T_A$=125°C | (Note 3) | | 1 | 10 | |
| Collector-Emitter Leakage Current | $I_{CEO}$ | $V_{CE}$=40V | $T_A$=25°C | (Note 3) | | 0.5 | 5 | nA |
| | | | $T_A$=125°C | (Note 3) | | 0.5 | 5 | µA |
| Collector-Emitter Breakdown Voltage | $LV_{CEO}$ | $I_C$=1mA | | | 40 | | | V |
| Collector-Base Breakdown Voltage | $BV_{CBO}$ | $I_C$=100µA | | | 60 | | | V |
| Emitter-Base Breakdown Voltage | $BV_{EBO}$ | $I_E$=10µA | | | 6.25 | | 7.25 | V |
| Collector-Substrate Breakdown Voltage | $BV_{CS}$ | $I_C$=10µA | | | 40 | | | V |
| Base-Emitter Forward Voltage | $V_{BE}$ | $\|I_E\|$=1mA | $V_{CE}$=5V | | 0.67 | | 0.79 | V |
| Matching of Base-Emitter Forward Voltages | $\Delta V_{BE}$ | $\|I_E\|$=1mA | $V_{CE}$=5V | (Note 4) | | ±2 | ±6 | mV |
| Temperature Coefficient of $V_{BE}$ | $\Delta V_{BE}/\Delta T$ | $\|I_E\|$=1mA | $V_{CE}$=5V | | | -1.8 | | mV/°C |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_C$=1mA | One Collector Contact (One Diffusion Region) | (Note 5) | | 0.2 | 0.3 | V |
| | | | Two Collector Contacts (Two Diffusion Regions) | (Note 5) | | 0.17 | 0.25 | |
| | | $(I_C/I_B)$=10 | Four Collector Contacts (Two Diffusion Regions) | | | 0.15 | 0.2 | |
| Maximum Collector Current | $I_{C(MAX)}$ | $P_{D(MAX)}$=300mW | | | | | 20 | mA |
| Cutoff Frequency | $f_T$ | $I_C$=5mA | $V_{CE}$=5V | | | 400 | | MHz |

SMALL NPN TRANSISTOR (CONTINUED)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Storage Time | $\tau_S$ | $(I_C/I_B)=10$ $R_B=750\Omega$ | $I_C=1mA$ | | 7 | | ns |
| | | | $I_C=10mA$ | | 120 | | |
| Emitter-Base Capacitance | $C_{EB}$ | $V_{EB}=0V$ | (Note 6) | | 1.1 | | pF |
| Collector-Base Capacitance | $C_{CB}$ | $V_{CB}=0V$ | (Note 6) | | 1.5 | | pF |
| Collector-Substrate Capacitance | $C_{CS}$ | $V_{CS}=0V$ | (Note 6) | | 3 | | pF |

Notes:

1) All collector contacts connected in parallel.

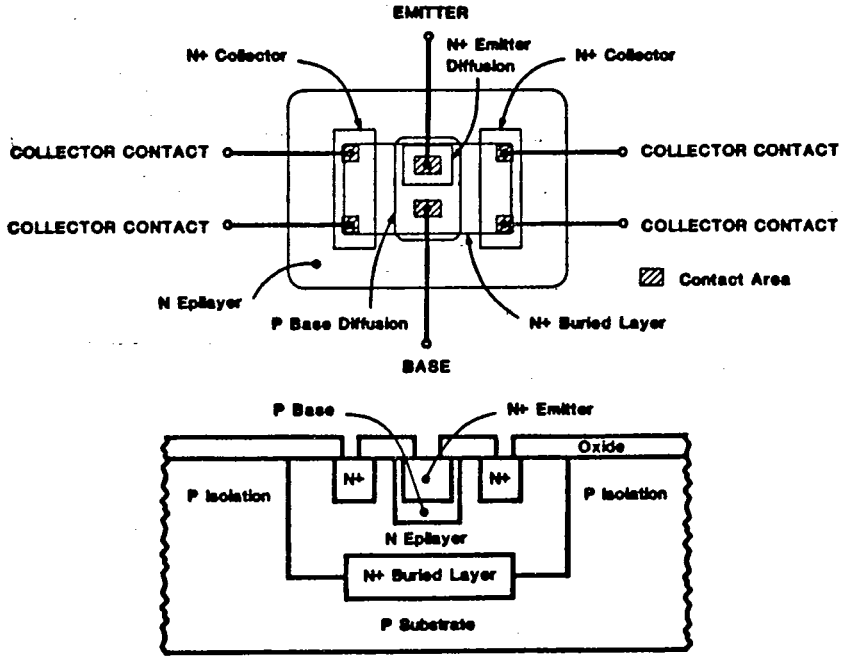
2) $h_{FE}$ matching is satisfied by $1-2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right| < \frac{h_{FE(2)}}{h_{FE(1)}} < 1+2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right|$ where $h_{FE(1)}$ and $h_{FE(2)}$ are any two current gains chosen from a population of like transistors on chip.

3) Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.

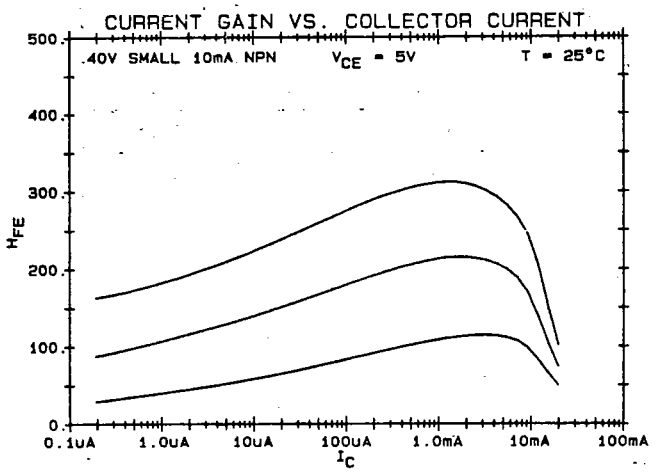
4) Matching of $V_{BE}$ is satisfied by $|V_{BE(2)}-V_{BE(1)}| < 2|\Delta V_{BE(MAX)}|$ where $V_{BE(1)}$ and $V_{BE(2)}$ are any two base-emitter voltages chosen from a population of like transistors on chip.

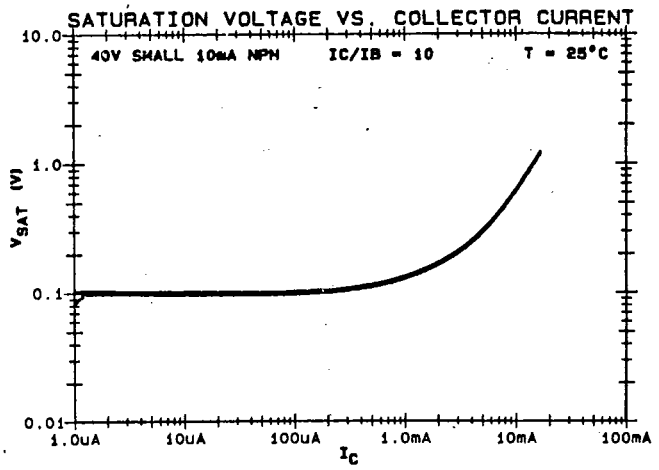
5) It is not recommended to operate the transistor in the saturation mode when only one collector contact or two collector contacts on the same N+ diffusion region are used, since a high saturation voltage is inevitable, especially at increased collector currents.

6) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.




Layout and Cross-Section of Small 10mA NPN Transistor
(Not to Scale)




SMALL 10mA DIODE (TRANSISTOR WITH COLLECTOR AND BASE SHORTED)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITION | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Forward Voltage Drop | $V_F$ | $I_F$=100µA | | 0.61 | | 0.73 | V |
| | | $I_F$=1mA | | 0.67 | | 0.79 | |
| | | $I_F$=10mA | | 0.79 | | 0.91 | |
| Matching of Forward Voltages | $\Delta V_F$ | $I_F$=1mA | (Note 1) | | ±2 | ±6 | mV |
| Temperature Coefficient of $V_F$ | $\Delta V_F/\Delta T$ | $I_F$=1mA | | | -1.8 | | mV/°C |
| Leakage Current | $I_O$ | $V_R$=20V | $T_A$=25°C (Note 2) | | 0.2 | | nA |
| | | | $T_A$=125°C (Note 2) | | 10 | | |
| Breakdown Voltage | $BV_D$ | $I_R$=10µA | | 6.25 | | 7.25 | V |
| Maximum Diode Current | $I_{F(MAX)}$ | | | | | 20 | mA |
| Junction Capacitance | $C_J$ | $V_D$=0V | (Note 3) | | 1.1 | | pF |

Notes:

1) Matching of $V_F$ is satisfied by $|V_{F(2)}-V_{F(1)}| < 2|\Delta V_{F(MAX)}|$ where $V_{F(1)}$ and $V_{F(2)}$ are any two forward voltages chosen from a population of like diodes on chip.

2) Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.

3) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.

## SMALL 10mA ZENER DIODE (EMITTER-BASE JUNCTION OF TRANSISTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Breakdown Voltage | $V_Z$ | $I_Z$=1μA | 6.2 | 6.5 | 7.2 | V |
| | | $I_Z$=10μA | 6.25 | 6.55 | 7.25 | |
| | | $I_Z$=100μA (Note 1) | 6.3 | 6.6 | 7.3 | |
| | | $I_Z$=1mA (Note 1) | 6.4 | 6.7 | 7.4 | |
| | | $I_Z$=10mA (Note 1) | 7 | 7.3 | 8 | |
| Dynamic Impedance (in the Breakdown Mode) | $R_Z$ | $I_Z$=1mA | | 85 | | Ω |
| Temperature Coefficient of Breakdown Voltage | $\Delta V_Z/\Delta T$ | $I_Z$=1mA | | 2.4 | | mV/°C |

Notes:

1) Base-emitter breakdown, unlike base-collector breakdown, can be damaging to the transistor particularly for long breakdown duration at high current. Under these conditions, $h_{FE}$ degradation is inevitable; therefore, $V_Z$ is tested at 1μA and 10μA for each transistor. Operation at higher current has been fully characterized and is guaranteed by extrapolation.

# 40V LATERAL PNP TRANSISTOR

## 1mA QUAD COLLECTOR

### GENERAL DESCRIPTION

The lateral PNP transistor has an oval-shaped, P-type emitter, surrounded by four P-type collector diffusions in a single base region. The base is made with an N+ diffusion with two base contacts in it. All four collectors should be connected together when a single collector transistor is required. When current ratios are important, such as for multiple current sources, the collectors can be used individually. Unused collectors must be connected to the substrate or any other potential that will ensure that the transistor does not saturate.

### FEATURES

Quad Collectors
Matched $V_{BE}$ and $h_{FE}$ Transistor Parameters

### TYPICAL APPLICATIONS

Current Sources
Active Loads
Level Shifters
Biasing Stages
Amplifiers

0.25mA (PER COLLECTOR) QUAD-COLLECTOR LATERAL PNP TRANSISTOR
(EACH COLLECTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| DC Current Gain | $h_{FE}$ | $V_{CE}$=-5V | $I_C$=-25μA One Collector (Note 1) | 5 | | 37.5 | |
| | | | $I_{C(TOTAL)}$=-50μA Two Collectors Connected in Parallel (Note 1) | 10 | | 75 | |
| | | | $I_{C(TOTAL)}$=-100μA Four Collectors Connected in Parallel | 20 | | 150 | |
| Matching of DC Current Gains | $\Delta h_{FE}$ | $I_C$=-100μA $V_{CE}$=-5V (Note 2) | | | ±5 | ±15 | % |
| Temperature Coefficient of $h_{FE}$ | $\Delta h_{FE}/\Delta T$ | $I_C$=-100μA -55°C < $T_A$ < 125°C | | | -0.1 | | %/°C |
| Collector-Base Leakage Current | $I_{CBO}$ | $V_{CB}$=-20V | $T_A$=25°C (Note 3) | | -0.02 | -0.2 | nA |
| | | | $T_A$=125°C (Note 3) | | -5 | -50 | |
| Collector-Emitter Leakage Current | $I_{CEO}$ | $V_{CE}$=-20V | $T_A$=25°C (Note 3) | | -0.2 | -2 | nA |
| | | | $T_A$=125°C (Note 3) | | -0.05 | -0.5 | |
| Collector-Emitter Breakdown Voltage | $BV_{CEO}$ | $I_C$=-100μA | | -40 | | | V |
| Collector-Base Breakdown Voltage | $BV_{CBO}$ | $I_C$=-100μA | | -60 | | | V |
| Emitter-Base Breakdown Voltage | $BV_{EBO}$ | $I_E$=-100μA | | -60 | | | V |
| Base-Substrate Breakdown Voltage | $BV_{BS}$ | $I_B$=10μA | | 40 | | | V |
| Base-Emitter Forward Voltage | $V_{BE}$ | $I_E$=100μA $V_{CE}$=-5V | | -0.62 | | -0.77 | V |
| Matching of Base-Emitter Forward Voltages | $\Delta V_{BE}$ | $I_E$=100μA $V_{CE}$=-5V (Note 4) | | | ±2 | ±6 | mV |
| Temperature Coefficient of $V_{BE}$ | $\Delta V_{BE}/\Delta T$ | $I_E$=100μA $V_{CE}$=-5V | | | 1.8 | | mV/°C |

QUAD-COLLECTOR LATERAL PNP TRANSISTOR (CONTINUED)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $(I_{C(TOTAL)}/I_B)=1$ | $I_C$=-25μA One Collector (Notes 1,5) | | -0.12 | -0.2 | V |
| | | | $I_{C(TOTAL)}$=-50μA Two Collectors Connected in Parallel (Notes 1,5) | | | | |
| | | | $I_{C(TOTAL)}$=-100μA Four Collectors Connected in Parallel (Note 5) | | | | |
| Maximum Usable Collector Current | $I_{C(MAX)}$ | (Per Collector) | | | | -0.5 | mA |
| Cutoff Frequency | $f_T$ | $I_{C(TOTAL)}$=-100μA $V_{CE}$=-5V | Four Collectors Connected in Parallel | | 3.5 | | MHz |
| Storage Time | $t_S$ | $(I_{C(TOTAL)}/I_B)=1$ | $I_{C(TOTAL)}$=-100μA Four Collectors Connected in Parallel | | 100 | | ns |
| | | $R_B$=750Ω | $I_{C(TOTAL)}$=-1mA Four Collectors Connected in Parallel | | 140 | | |
| Emitter-Base Capacitance | $C_{EB}$ | $V_{EB}$=0V | (Note 6) | | 0.2 | | pF |
| Collector-Base Capacitance | $C_{CB}$ | $V_{CB}$=0V | (Note 6) | | 0.5 | | pF |
| Base-Substrate Capacitance | $C_{BS}$ | $V_{BS}$=0V | (Note 6) | | 5 | | pF |

Notes:

1) With the other collectors grounded.

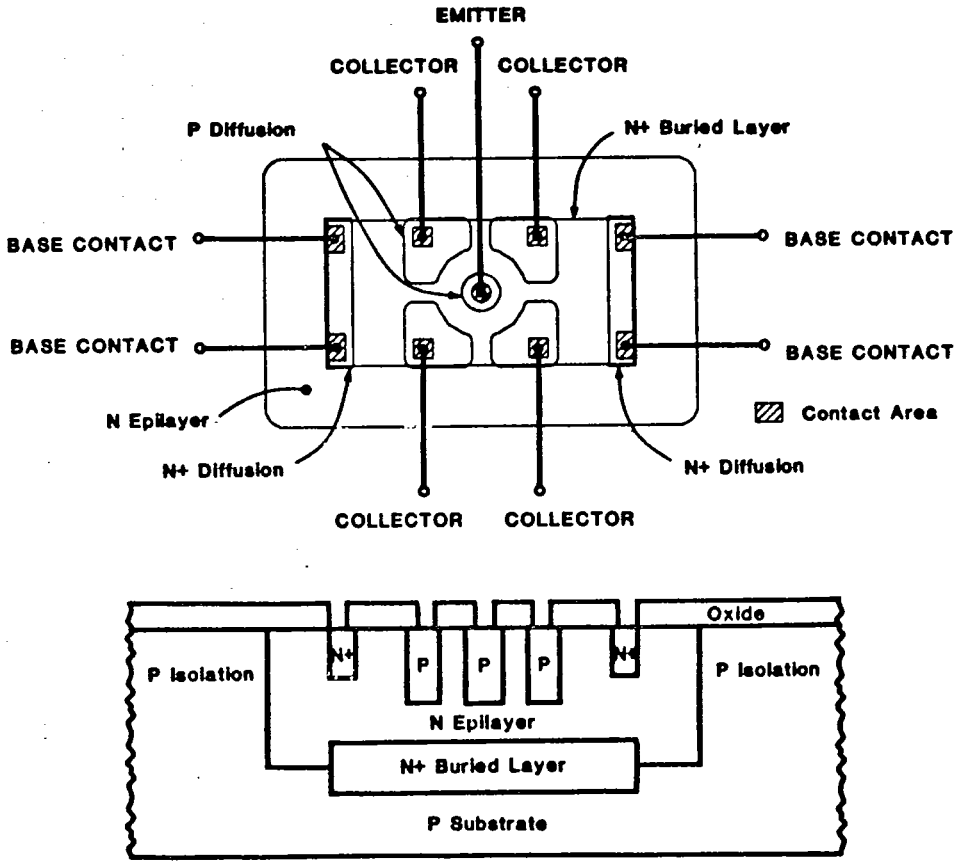
2) $h_{FE}$ matching is satisfied by $1-2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right| < \frac{h_{FE(2)}}{h_{FE(1)}} < 1+2\left|\frac{\Delta h_{FE(MAX)}}{100\%}\right|$ where $h_{FE(1)}$ and $h_{FE(2)}$ are any two current gains chosen from a population of like transistors on chip.

3) Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.

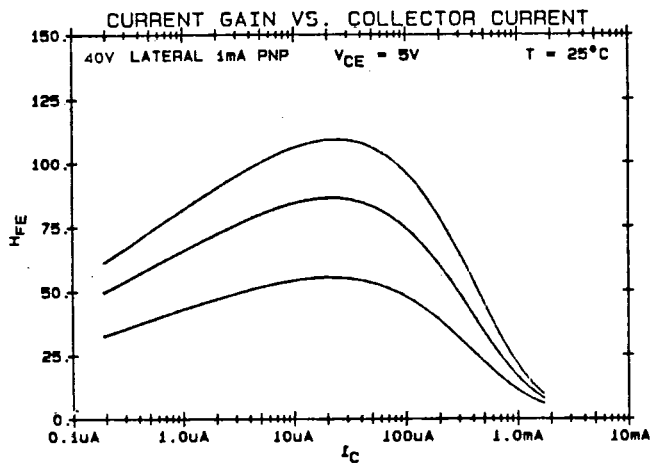
4) Matching of $V_{BE}$ is satisfied by $|V_{BE(2)}-V_{BE(1)}| < 2|\Delta V_{BE(MAX)}|$ where $V_{BE(1)}$ and $V_{BE(2)}$ are any two base-emitter voltages chosen from a population of like transistors on chip.

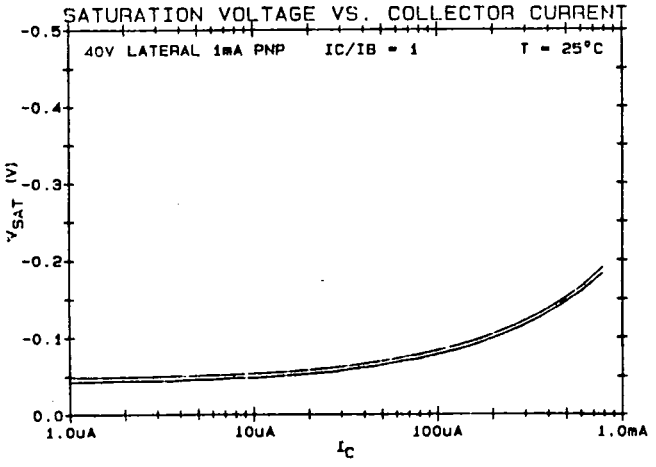
5) It is not advisable to operate the lateral PNP transistor in the saturation mode since the parasitic vertical substrate transistor (related to the lateral transistor) becomes heavily active.

6) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.




Layout and Cross-Section of
0.25mA (Per Collector) Quad-Collector Lateral PNP Transistor
(Not to Scale)



## LATERAL PNP DIODE (EMITTER-BASE JUNCTION OF TRANSISTOR)

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP. | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Forward Voltage Drop | $V_F$ | $I_F$=100μA | | | 0.61 | | 0.73 | V |
| | | $I_F$=1mA | | | 0.74 | | 0.86 | |
| | | $I_F$=10mA | | (Note 1) | | 1.15 | | |
| Matching of Forward Voltages | $\Delta V_F$ | $I_F$=1mA | | (Note 2) | | ±2 | ±6 | mV |
| Temperature Coefficient of $V_F$ | $\Delta V_F/\Delta T$ | $I_F$=1mA | | | | -1.8 | | mV/°C |
| Leakage Current | $I_O$ | $V_R$=40V | $T_A$=25°C | (Note 3) | | 0.5 | | nA |
| | | | $T_A$=125°C | (Note 3) | | 50 | | |
| Breakdown Voltage | $BV_D$ | $I_R$=100uA | | | 60 | | | V |
| Maximum Diode Current | $I_{F(MAX)}$ | | | (Note 1) | | | 10 | mA |
| Junction Capacitance | $C_J$ | $V_D$=0V | | (Note 4) | | 0.2 | | pF |

Notes:

1) The lateral PNP diode, like the lateral PNP transistor, has a parasitic vertical substrate current that becomes dominant at high operating current. This substrate loss current becomes comparable to the diode forward current at about 5mA.

2) Matching of $V_F$ is satisfied by $|V_{F(2)}-V_{F(1)}| < 2|\Delta V_{F(MAX)}|$ where $V_{F(1)}$ and $V_{F(2)}$ are any two forward voltages chosen from a population of like diodes on chip.

3) Device leakage current is specified. Mishandled packaged devices may exhibit much higher leakage currents due to external surface leakage.

4) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.

# 40V P-TYPE DIFFUSED RESISTORS

## 200Ω, 450Ω, 900Ω, 1.8KΩ, 3.6KΩ

**GENERAL DESCRIPTION**

The P-type diffused resistors are made during the base diffusion step in the integrated circuit process. They exhibit excellent ratio matching properties which are primerily dependent on the masking accuracy in the fabrication process. However, the obsolute values are not as accurate as they are directly related to the tolerances in the diffusion process.

**FEATURES**

Matched Resistor Ratios

**TYPICAL APPLICATIONS**

Analog and Digital Circuitry

ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Absolute Values<br>200Ω<br>450Ω<br>900Ω<br>1.8KΩ<br>3.6KΩ | R | $V_R$=5V<br><br>150<br>337.5<br>675<br>1350<br>2700 | | <br>200<br>450<br>900<br>1800<br>3600 | <br>250<br>562.5<br>1125<br>2250<br>4500 | Ω |
| Epi (Vcc Terminal)-Substrate Breakdown Voltage | $BV_{NS}$ | $I_N$=10μA | 40 | | | V |
| Epi (Vcc Terminal)-Resistor Breakdown Voltage | $BV_{NR}$ | $I_N$=100μA | 60 | | | V |
| Resistor-Substrate Breakdown Voltage | $BV_{RS}$ | $I_R$=10μA | 40 | | | V |
| Temperature Coefficient of R | ΔR/ΔT | $V_R$=5V, $-55°C < T_A < -25°C$ | | -0.02 | | %/°C |
| | | $V_R$=5V, $-25°C < T_A < 25°C$ | | 0.06 | | %/°C |
| | | $V_R$=5V, $25°C < T_A < 125°C$ | | 0.13 | | %/°C |
| Matching of Equal Design Value Resistors | ΔR(1:1) | $V_R$=5V, $R_2=R_1$ (Notes 1,2) | | | ±3 | % |
| Ratio Matching of Unequal Design Value Resistors | ΔR(1:2) | $V_R$=5V, $R_2=2R_1$ (Notes 1,2) | | | ±4 | % |
| | ΔR(1:4) | $V_R$=5V, $R_2=4R_1$ (Notes 1,2) | | | ±5 | % |
| | ΔR(1:8) | $V_R$=5V, $R_2=8R_1$ (Notes 1,2) | | | ±6 | % |
| Maximum Power Dissipation | $P_{D(MAX)}$ | | | | 300 | mW |
| Epi (Vcc Terminal)-Resistor Capacitance<br>200Ω<br>450Ω<br>900Ω<br>1.8KΩ<br>3.6KΩ | $C_{NR}$ | $V_{NR}$=0V (Notes 3,4) | | <br>0.7<br>0.4<br>0.6<br>0.8<br>1.7 | | pF |

Notes:

1) Resistor ratio matching is satisfied by

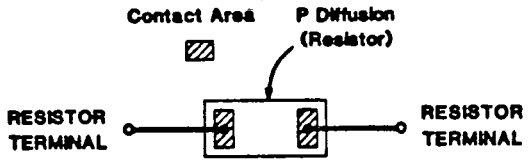
$$k\left(1-2\left|\frac{\Delta R(MAX)}{100\%}\right|\right) < \frac{R_2}{R_1} < k\left(1+2\left|\frac{\Delta R(MAX)}{100\%}\right|\right)$$

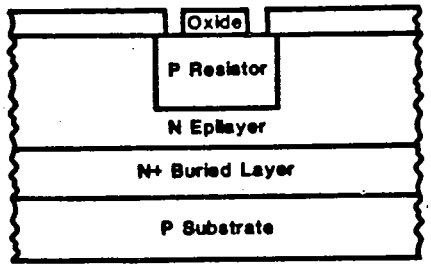
where k is the resistor ratio of the nominal values, and $R_1$ and $R_2$ are any two resistors chosen from these populations on chip.

2) These particular matching parameters apply to the various resistor ratios on chip.

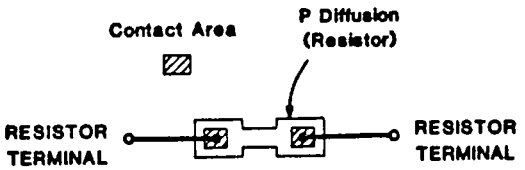
3) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.

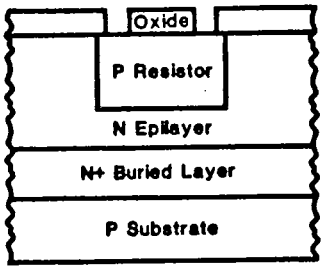
4) These capacitances refer to each individual resistor; however, most resistors on chip are strung together, thus presenting a higher total capacitance for each resistor group.



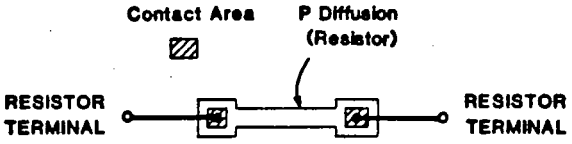



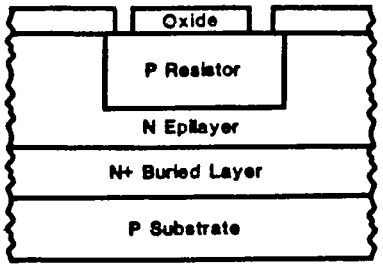

Layout and Cross-Section of 200Ω P-Type Diffused Resistor (Not to Scale)



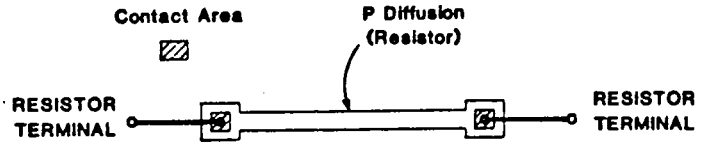



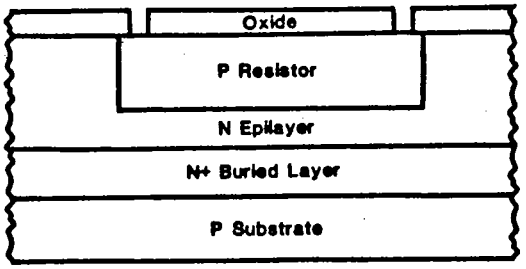

Layout and Cross-Section of 450Ω P-Type Diffused Resistor (Not to Scale)



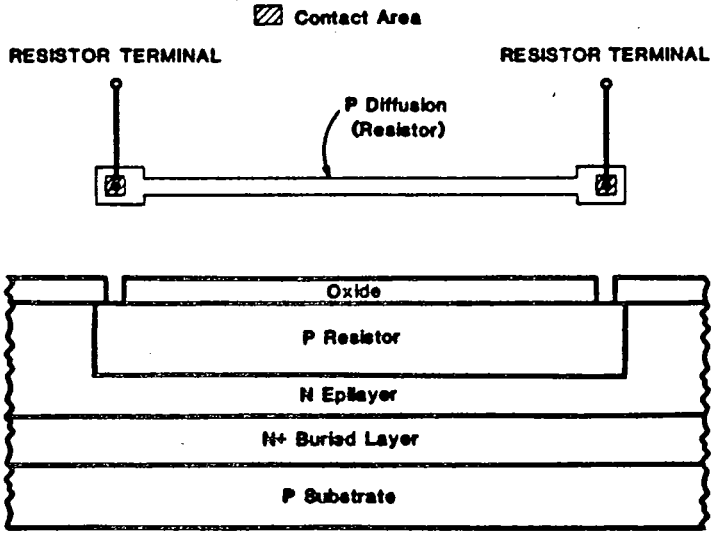




Layout and Cross-Section of 900Ω P-Type Diffused Resistor (Not to Scale)

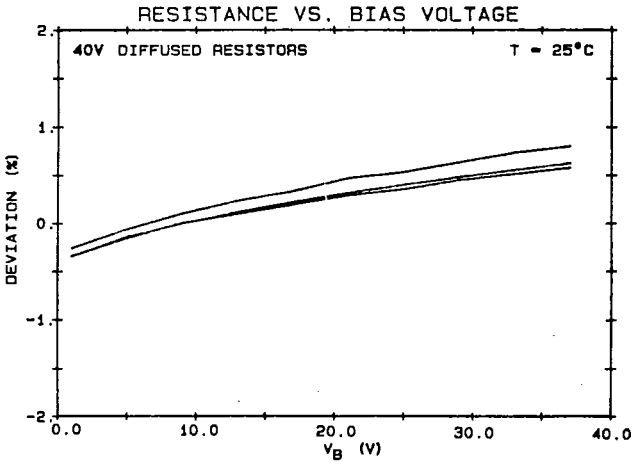



Layout and Cross-Section of 1.8KΩ P-Type Diffused Resistor (Not to Scale)




Layout and Cross-Section of 3.6KΩ P-Type
Diffused Resistor (Not to Scale)



# 40V EPI PINCH RESISTOR

## 60KΩ

**GENERAL DESCRIPTION**

The epi pinch resistor is made with a donut-shaped epilayer region that defines its size and shape. Two small N+ diffusion regions in the epilayer provide the ohmic contacts to the resistor terminals. The P-type substrate and isolation regions act as the resistor gate. The gate is therefore permanently biased at the most negative potential in the circuit. Unlike the base pinch resistor, the epi pinch resistor can sustain at least 40V before breakdown occures.

**FEATURES**

Matched Resistor Values

**TYPICAL APPLICATIONS**

Current Sources
General Purpose Cirultry

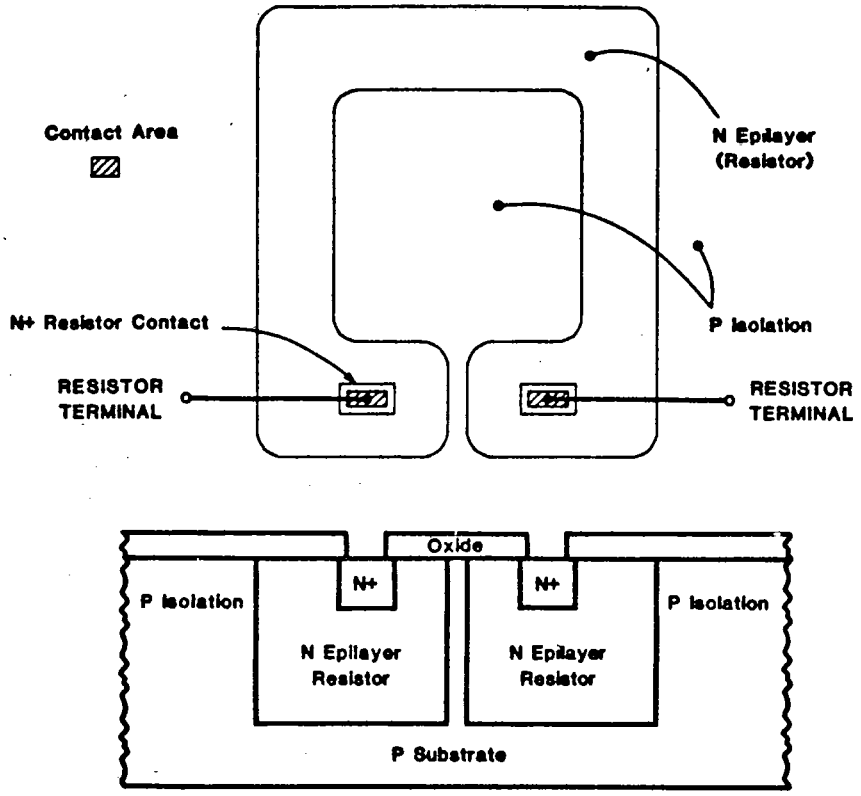
ELECTRICAL CHARACTERISTICS AT AMBIENT TEMPERATURE $T_A$=25°C (Unless otherwise noted)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Absolute Value | R | $I_R$=10μA | 30 | 60 | 120 | KΩ |
| Matching of Resistor Values | ΔR | $I_R$=10μA (Note 1) | | ±5 | | % |
| Breakdown Voltage (Across Resistor Terminals) | $BV_R$ | $I_R$=2mA | 40 | | | V |
| Resistor-Substrate Breakdown Voltage | $BV_{RS}$ | $I_R$=10μA | 40 | | | V |
| Temperature Coefficient of R | ΔR/ΔT | -55°C < $T_A$ < 125°C | | 0.5 | | %/°C |
| Maximum Power Dissipation | $P_{D(MAX)}$ | | | | 200 | mW |
| Resistor-Substrate Capacitance | $C_{RS}$ | $V_{RS}$=0V (Note 2) | | 6.5 | | pF |

Notes:

1) Resistor matching is satisfied by $1-2\left|\frac{\Delta R(MAX)}{100\%}\right| < \frac{R_2}{R_1} < 1+2\left|\frac{\Delta R(MAX)}{100\%}\right|$ where $R_1$ and $R_2$ are any two resistors chosen from a population of the same nominal value on chip.

2) Junction capacitance is specified. An average capacitance of 0.5pF must be added to include the effect of the package. Also included must be a capacitance of 1pF for each bonding pad which is related to the specific junction under test.




Layout and Cross-Section of 60KΩ Epi Pinch Resistor
(Not to Scale)