VECTRON INTERNATIONAL
A DOVER COMPANY

TM-056

Integrated Timing Solution

The TM-056 is a compact Timing Module, which functions as a complete system clock solution for general Stratum 3 timing applications. The TM-056 uses Vectron's Digital and Analog Phase Locked Loop (DPLL and APLL) technology and can lock to 2 reference frequencies automatically. The module has dual output clocks ranging from 8 kHz to 77.76 MHz. Simple control interface with comprehensive state engine, status and alarm indications and fully automatic operation makes seamless system integration of the TM-056 module.

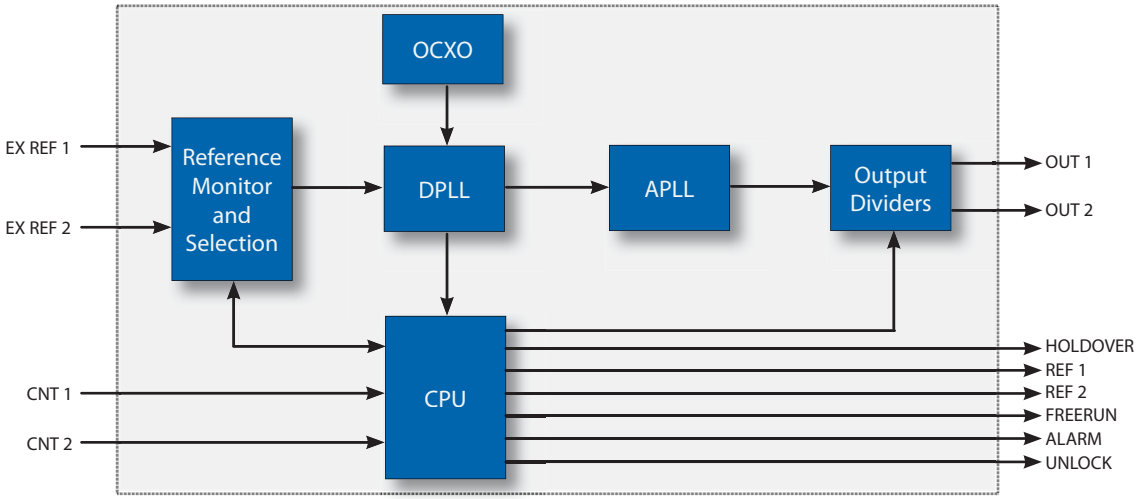
Features

- Single module Statum 3 synchronization solution.
- Complies with Telcordia GR-1244/GR-253 and ITU-T G.812/G.813 recommendations.
- Supports Free-run, Holdover and Lock modes.
- Accepts 2 reference inputs from frequency range 8kHz to 77.76MHz.
- Continuously monitors and evaluates both input reference signals simultaneously.
- Provides two synchronized outputs with frequency range up to 77.76MHz.
- On board OCXO that provides excellent stability in Freerun and Holdover mode.
- Loop filtering utilizing DPLL.
- Automatic "hit-less" switchover on loss of input.
- Holdover mode with 90 seconds of history.
- Alarms and status signals.
- Easy to use control interface and JTAG port for factory programming.
- Small dimensions 1.9" x 1.9" x 0.55".
- Product is compliant to RoHS directive and fully compatible with lead free assembly.

Applications

- Multi-service Switches and Routers
- ATM
- Gateway
- Access
- EDGE
- Core
- SONET
- SDH
- DWDM

Block Diagram



Description

The TM-056 is based on a digital PLL (DPLL) that performs filtering of input signals, and is complemented by an analog PLL (APLL) required to deliver high quality output signals. The most critical element of the TM-056 is the DPLL that generates a phase-locked clock, filters jitter and wander and suppresses input phase transients. All of these features are in agreement with international standards. The DPLL supports three mandatory modes of operation. (Free-run, Lock and Holdover). Each of these modes places specific requirements on the building blocks of the DPLL.

In Free-run mode the output is locked to an internal OCXO, and therefore timing and synchronization signals are based on the accuracy of on-board oscillators. This mode is typically used when a master clock source is required, not valid history of data for the Holdover mode, or immediately following system power-up before network synchronization is achieved.

In Holdover mode, the TM-056 generates a clock based on data collected from past reference signals when the module was locked. The Holdover mode is typically used when no external reference is available. The stability of the output signal in Holdover mode depends of the stability of the on-board oscillator. By default the TM-056 uses an OCXO as an on-board oscillator, but other type of oscillators are available on request.

In Lock mode the device can be locked to one of two external reference signals. The Lock mode is typically used when a slave clock source synchronized to the network is required. In this mode the TM-056 provides timing signals which are synchronized to one of two reference inputs (i.e. REF1 or REF2). The input reference signals may have a variety of nominal frequencies, which are specified by customers.
Both input references are continuously monitored and evaluated by the module in terms of presence and frequency offset relative to the local oscillator. The TM-056 rejects all reference signals that are out of the frequency range of approximately ±17ppm. A reference will be qualified if the signal is present and within the frequency limit for more than approximately 20s.

The TM-056 dynamically changes the loop bandwidth according to the status of the DPLL. There are three stages for the DPLL to be locked. The first stage is frequency acquisition that runs until the frequency becomes equal to the reference. The second stage is phase acquisition that runs until a new phase reference is determined. The third stage is tracking when the DPLL is locked and tracks the phase reference with very low loop bandwidth. This method with three stages ensures a minimum locking time and minimum phase jumps and shifts during rearrangement.

The phase data is continuously collected for the history buffer during the time when the unit is locked to any of the input references. The history buffer is actually a circular buffer in memory that keeps valid phase data for Holdover mode for the last 90 seconds of operation. When the TM-056 enters Holdover mode the data from the buffer is validated and further processed. At the beginning of operation the unit has no valid history buffer.

The APLL is locked to DPLL output and provides low jitter output. The TM-056 module provides two output signals OUT1 and OUT2. The outputs are generated by APLL and scaled by the output dividers. The frequency of the APLL oscillator is specified according to an application where the TM-056 will be used.

The J-TAG service port is used for on board chip programming and debugging purposes during production and testing. The port is for factory use only and any unauthorized access can damage the unit.

The TM-056 provides a detailed monitoring and indications of operation mode and status of the unit. There are six digital outputs that report statuses and alarms of the module. These alarms are mainly used for communication between the module and equipment where the module is operating.

Status Indications	Mode of Operation
HOLDOVER	The signal is ON (logic high) when TM-056 in Holdover mode.
REF 1	The signal is ON (logic high) when TM-056 in Lock mode using EX REF 1.
REF 2	The signal is ON (logic high) when TM-056 in Lock mode using EX REF 2.
FREE-RUN	The signal is ON (logic high) when TM-056 in Free-run mode.
UNLOCK	The signal in ON (logic high) when TM-056 is not locked to an external reference.
ALARM	The signal is ON (logic high) when TM-056 is in Holdover of Free-run mode.

TM-056 Status Indications

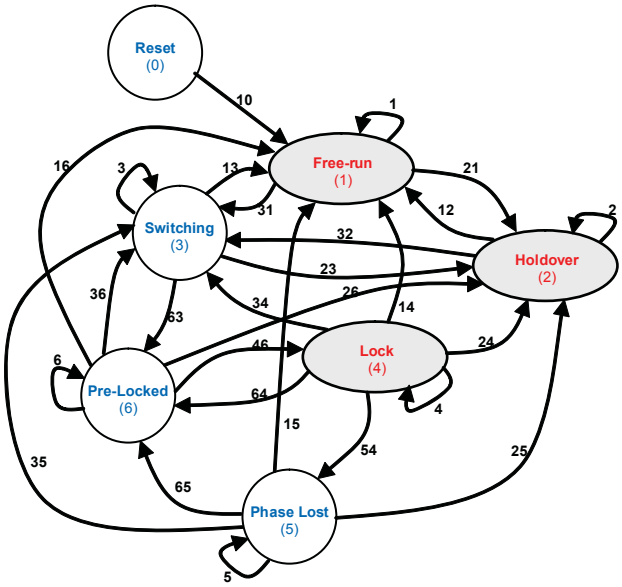
A simple control interface is available for user to control the operation of the TM-056. The two external inputs CNT1 and CNT2 provide this feature. The truth table below shows behavior of the TM-056 module according to the control inputs states.

CNT2	CNT1	Mode of Operation
0	0	Free-run
0	1	Locked to EX REF1
1	0	Locked to EX REF2
1	1	Holdover

TM-056 Mode selection

By changing the control inputs the user can change the state of the TM-056 according to the state engine diagram. The state engine diagram of the TM-056 shows the transients between the three operating modes: Free-run, Lock and Holdover, shown as an ellipse, in a changing environment. The temporary operating states, showed as a circle, are used internally until one of the three modes is reached. Besides the control inputs (CNT1 and CNT2), certain types of inputs and statuses affect the changes in the state engine such as the availability of external references and change of the quality of the input reference signal otside predefined limits.

TM-056 State Engine



Transition	Name/Description	Condition
1	Free-run	Until other conditions are not true
2	Holdover	Until other conditions are not true
3	Switching	Until other conditions are not true
4	Lock	Until other conditions are not true
5	Phase Lost	Until other conditions are not true
6	Pre-Locked	Until other conditions are not true
10	Reset	Until the internal reset flag is not set.
12	Holdover to Free-run	If control signals are changed to CNT0=0 and CNT1=0 or no valid Holdover history available.
13	Switching to Free-run	If control signals are changed to CNT0=0 and CNT1=0 or selected reference is disqualified and no valid Holdover history available.
14	Lock to Free-run	If control signals are changed to CNT0=0 and CNT1=0 or selected reference is disqualified and no valid Holdover history available.
15	Phase Lost to Free-run	If control signals are changed to CNT0=0 and CNT1=0 or selected reference is disqualified and no valid Holdover history available.
16	Pre-Locked to Free-run	If control signals are changed to CNT0=0 and CNT1=0 or selected reference is disqualified and no valid Holdover history available.
21	Free-run to Holdover	If control signals are changed to CNT0=1 and CNT1=1 and valid Holdover history available.
23	Switching to Holdover	If control signals are changed to CNT0=1 and CNT1=1 or selected reference is disqualified and valid Holdover history available.
24	Lock to Holderover	If control signals are changed to CNT0=1 and CNT1=1 or selected reference is disqualified and valid Holdover history available.
25	Phase Lost to Holdover	If control signals are changed to CNT0=1 and CNT1=1 or selected reference is disqualified and valid Holdover history available.
26	Pre-Locked to Holdover	If control signals are changed to CNT0=1 and CNT1=1 or selected reference is disqualified and valid Holdover history available.
31	Free-run to Switching	If qualified reference is selected by the control pins (CNT0 and CNT1).
32	Holdover to Switching	If any changes occurred on the control pins (CNT0 and CNT1) during Holdover or selected reference is qualified.
34	Locked to Switching	If any changes occurred on the control pins (CNT0 and CNT1) during Lock.
35	Phase Lost to Switching	If any changes occurred on the control pins (CNT0 and CNT1) during Phase Lost.
36	Pre-Locked to Switching	If any changes occurred on the control pins (CNT0 and CNT1) during Pre-Locked.
46	Pre-Locked to Lock	If the internal Pre-lock flag is set.
54	Locked to Phase Lost	If the internal Phase Lost flag is set
63	Switching to Pre-Locked	Until the internal flag is not set
64	Locked to Pre-Locked	Until the internal flag is not set.
65	Phase Lost to Pre-Locked	If the internal Phase Lost flag is not set

Specifications

Parameter	*Specifications*	*Notes*
Power		
Voltage	+5 VDC	+3.3VDC available on request
Supply Current During Warm-up	500mA	@ 25˚C
Steady State Current	300mA	@ 25˚C
Input Signals		
Number of Input Signals	2	
Input Reference Frequency	8kHz - 77.76MHz	Per customer request
Signal Level	LVCMOS	
Time Reference Characteristics	Telcordia: GR-1244-CORE 3.2.1. R3-1	
Output Signals		
Number of Output Signals	2	
Output 1	up to 77.76MHz	Per customer request
Output 2	up to 77.76MHz	Per customer request
Signal Level Output 1	LVCMOS	
Signal Level Output 2	LVCMOS	
Input and Output Reference Signal Characteristics		
Input Signal	Telcordia: GR-1244-CORE 3.2.1	
Jitter Tolerance	Telcordia: GR-1244-CORE 4.2, GR-253-CORE 5.4.4.3.6	ITU-T: G.812 Type III/IV
Phase Transient Tolerance	Telcordia: GR-1244-CORE 4.4	
Wander Generation	Telcordia: GR-1244-CORE 5.3, GR-253-CORE 5.4.4.3.2	ITU-T: G.812 para 11.2 Type III/IV
Wander Tolerance	Telcordia: GR-1244-CORE 4.3	ITU-T: G.825
Wander Transfer	Telcordia: GR-1244-CORE 5.4, GR-253-CORE 5.4.4.2.4	ITU-T: G.812 Type III/IV
MTIE	Telcordia: GR-1244-CORE 5.3, GR-253-CORE 5.4.4.3.2	
TDEV	Telcordia: GR-1244-CORE 5.3, GR-253-CORE 5.4.4.3.2	
Phase Transient	Telcordia: GR-1244-CORE 5.6, GR-253-CORE 5.4.4.3.3	
Jitter Generation	Telcordia: GR-1244-CORE 5.5, GR-253-CORE 5.6.2.3	
Jitter Transfer	Telcordia: GR-1244-CORE 5.5, GR-253-CORE 5.6.2.1	
DPLL Performance		
Free Run Accuracy	≤ ±4.6ppm	GR-1244-CORE 5.1
Holdover Stability	≤ ±3.6x10-7 (Stratum 3)	GR-1244-CORE 5.2
Pull in Range	≥ ±17ppm	GR-1244-CORE 3.5
Lock Time	≤ 100s (Stratum 3)	GR-1244-CORE 3.5
Lock Accuracy	≤1x10-11	Average 24h
General		
Mechanical	1.9" x 1.9" x 0.52" (48.26 x 48.26 x 13.28 mm)	18 pin package, RoHS compliant
Operating Temperature	0 to 70°C	-40 to 85°C option available
Local Oscillator	OCXO	TCXO option available

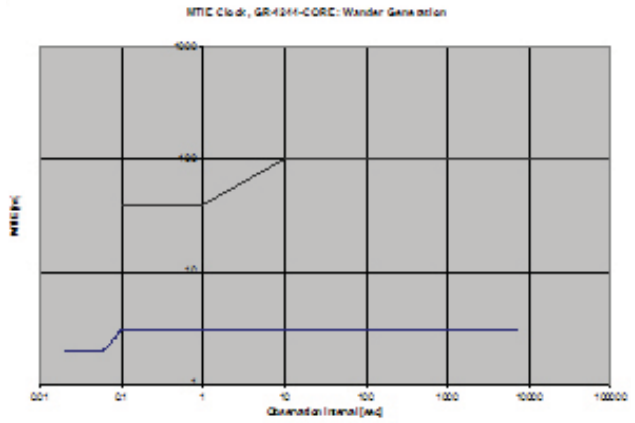
Absolute Maximum/Minimum Rating

Symbol	Parameter	Min	Max	Unit	Notes
V_{CC}	Supply Voltage	-0.5	+7.0	V	1
V_{IN}			V_{CC} +0.5	V	1
T_{STG}	Storage Temperature	-70	+155	C	1

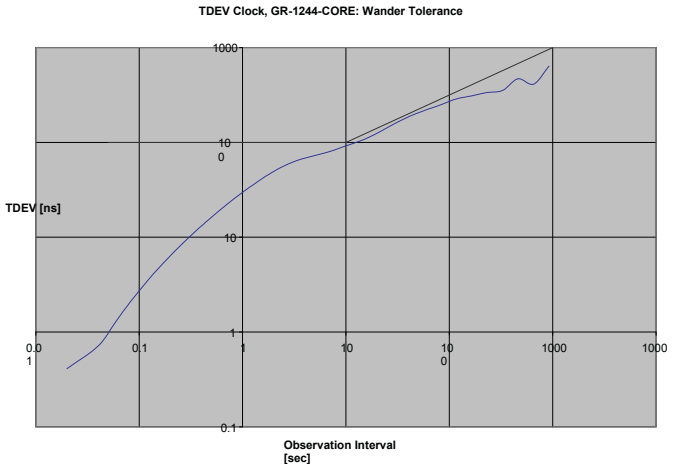
Note 1: Stresses beyond those listed under Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions are not implied. Exposure to Absolute Max Rating conditions for extended periods of time may affect device reliability.

Performance

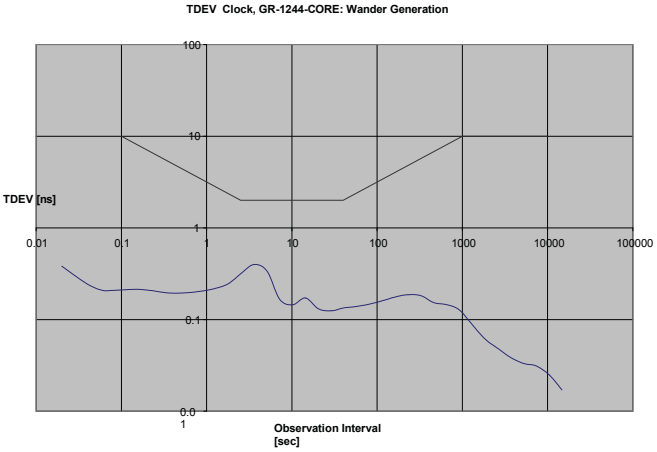
The following paragraph shows typical TM-056 performances. The measurements were performed in according to Telcordia GR-1244-CORE recommendation using a system that emulates standard timing configuration in network equipment. For more details please contact the factory.



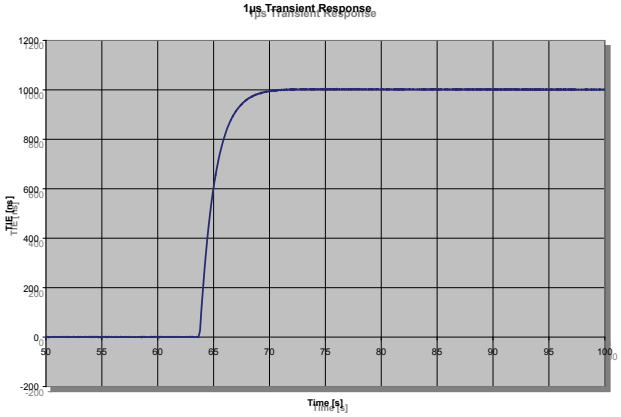
TM-056 typical performance - Wander Generation MTIE GR-1244-CORE



TM-056 typical performance - Wander Tolerance TDEV GR-1244-CORE

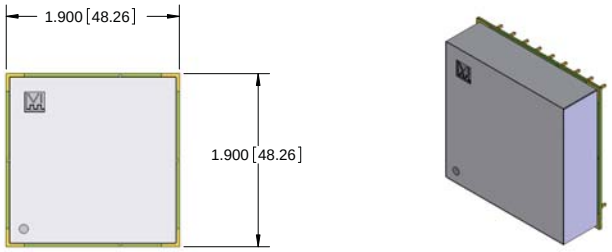


TM-056 typical performance - Wander Generation TDEV GR-1244-CORE

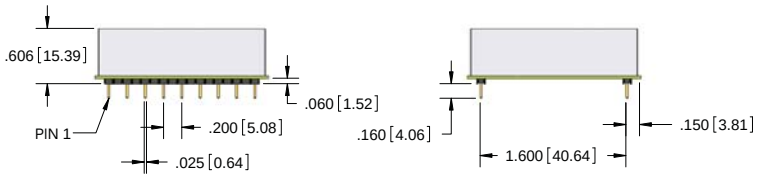


TM-056 typical performance - 1µs Transient Response TIE

Mechanical Dimensions



TM-056 Outline Drawing



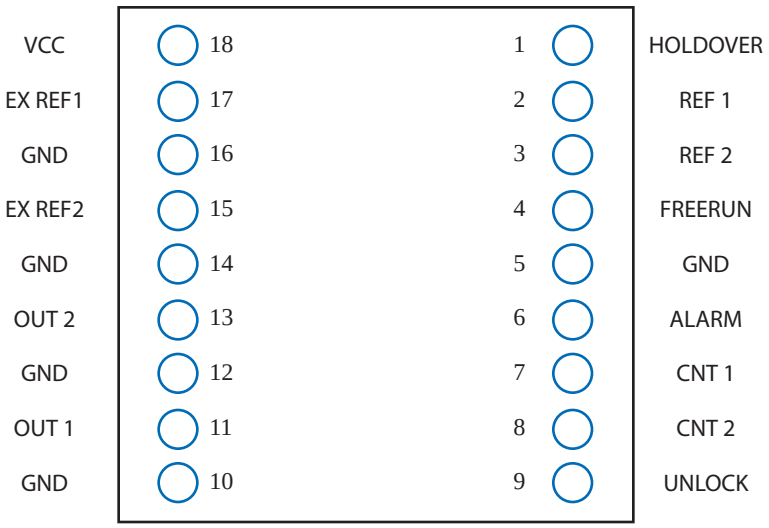
Soldering Information

The TM-056 can be soldered to the main board in following ways:

1. Wave soldering machine - using no cleaning material.
2. Manual soldering - max. Temperature is 370°C, for 2 seconds, using no clean soldering material.

Pin Assignment

The picture below shows the pin-out for the TM-056.



TM-056 Pin Assignment - The Bottom View

Pin	Name	Type	Description
1	HOLDOVER	Output	Indication that TM-056 is in Holdover mode
2	REF 1	Output	Indication that TM-056 is in Lock mode – locked to EX REF 1 signal.
3	REF 2	Output	Indication that TM-056 is in Lock mode – locked to EX REF 2 signal.
4	FREERUN	Output	Indication that TM-056 is in Free-run mode.
5	GND		Ground
6	ALARM	Output	Indication that TM-056 has an alarm.
7	CNT 1	Input	Control Input 1, the external input for selecting mode of TM-056 – see table.
8	CNT 2	Input	Control Input 2, the external input for selecting mode of TM-056 – see table.
9	UNLOCK	Output	Indication that TM-056 is unlocked to any reference input signal.
10	GND		Ground
11	OUT 1	Output	Synchronized Output 1
12	GND		Ground
13	OUT 2	Output	Synchronized Output 2
14	GND		Ground
15	EX REF 2	Input	External reference 2 timing input
16	GND		Ground
17	EX REF 1	Input	External reference 1 timing input.
18	VCC	Power	Power supply input

TM-056 Pin Description

Ordering Information

TM - 056 - X X X - X - XX XX XX XX

Product Family
TM: Timing Module

Package
056: 48.3 x 48.3 x 14.7mm

Supply Voltage
C: 5.0VDC
L: 3.3VDC

Output Type
B: LVCMOS

Operating Temperature
C: 0 to 70°C
F: -40 to 85°C

Frequency Stability
A: Stratum 3
B: Future Use

Sync Output 2
See Table

Sync Output 1
See Table

Reference 2
See Table

Reference 1
See Table

Reference Frequencies		Synchronized Outputs	
A3	8kHz	A3	8kHz
A4	16kHz	A6	10kHz
B3	1.544MHz	B3	1.544MHz
B4	2.048MHz	B4	2.048MHz
D5	16.384MHz	D5	16.384MHz
D6	19.44MHz	D6	19.44MHz
E7	24.704MHz	E7	24.704MHz
H3	32.768MHz	H3	32.768MHz
H6	34.368MHz	H6	34.368MHz
H5	38.88MHz	H5	38.88MHz
J3	44.736MHz	J3	44.736MHz
J4	51.84MHz	J4	51.84MHz
K2	77.76MHz	K2	77.76MHz

Frequency codes reference table

Part number example: TM-056-CBC-A-A3A3D6A6 is the TM-056 module platform with 5V power supply, with LVCMOS input and output signals, operating in 0 to 70°C temperature range, complying with Stratum 3, with 2 external references of 8kHz, OUT1 is 19.44MHz and OUT2 is 10kHz.

Contact the factory for additional frequency options.

Version Change Notes

Version	Date	Note
1.0	5/5/2007	Initial Revision
1.1	5/10/2007	Added RoHS Notes
1.2	5/15/2007	Dimensions Typo error on the first page fixed
1.3	9/30/2008	Product Release