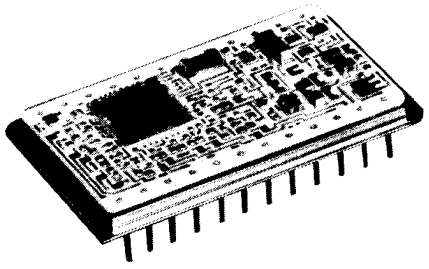
DAC-8528

12 BIT HYBRID D/A CONVERTER
Fast Settling; Very Low Glitch; Voltage or Current Output



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FEATURES

- *F.S. SETTLING TIME:*
  60 ns Max Current Output
  1 μs Max Voltage Output
- *GLITCH ENERGY*
  3 mA·ns Max Current Output
  2.5 V·ns Max Voltage Output
- *CODING:*
  Binary and Offset Binary
- *VOLTAGE RANGES:*
  ±2.5V, ±5V, ±10V, 0 to −5V, 0 to −10V
- *CURRENT RANGES:*
  ±2 mA, 0 to +4 mA
- *LINEARITY ERROR:*
  ±0.0125 % F.S.R.

DESCRIPTION

The DAC-8528 offers fast settling times and very low glitch at a moderate cost. It is a lower cost alternative to deglitched D/A converter systems. The converter is complete with an internal reference, feedback resistors, and an output amplifier. Each unit can be pin programmed for both voltage and current output ranges. The input is TTL compatible and standard packaging is a hermetically sealed 24 pin double DIP metal case.

APPLICATIONS

The high speed and low glitch of the DAC-8528 make it attractive for portable instrumentation, high speed automatic test equipment, aircraft and shipboard displays, and as the D/A in an A/D converter. The converter is a rugged, high reliability device, with standard processing based on MIL-STD-883, except for burn-in, which is an option. It can be used in remotely located and hard to access equipment where its small size and high MTBF are important.

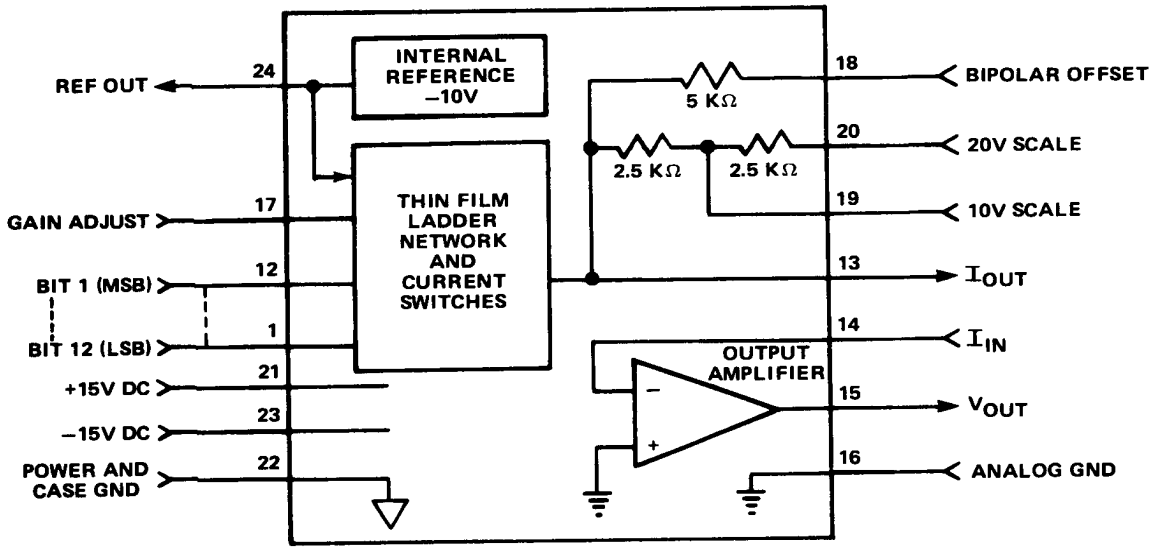

FIGURE 1. DAC 8528 BLOCK DIAGRAM

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DAC-8528 SPECIFICATIONS

Typical values at 25°C and at nominal power supply voltages unless indicated otherwise.

PARAMETER	UNITS	VALUE DAC-8528-11	VALUE DAC-8528-12
RESOLUTION	Bits	12	12
ACCURACY			
Linearity Error	%F.S. Range	±0.025 max	±0.0125 max
Linearity Tempco	ppm/°C	2	1.0
Differential Nonlinearity	LSB	±2 max	±1 max
Gain Error*			
Voltage Mode	%F.S. Range	0 to ±0.4 max	0 to +0.2 max
Current Mode	%F.S. Range	±2.0 max	±1.0 max
Gain Tempco	ppm/°C	30	20
Voltage Offset			
Offset Error*	%F.S. Range	0 to −0.1	
Offset Tempco	ppm/°C	±15 max unipolar ±25 max bipolar	
Current Offset			
Offset Error*	%F.S. Range	±0.025	
Offset Tempco	ppm/°C	±1.0 max unipolar ±10 max bipolar	
*Gain and offset errors can be trimmed to zero.			
DYNAMIC CHARACTERISTICS		Voltage Mode	Current Mode
Update Rate	MHz	20	50
Settling Time to ±1/2 LSB			
For ±F.S. Output Change	ns	1000 max	60 max
For ±1 LSB Change	ns	50 max	20 max
Glitch			
Glitch Energy		2500 mV-ns max	3 mA-ns max
Peak-to-Peak Amplitude		120 mV max	0.3 mA max
Width at 10%		45 ns max	20 ns max
Time Constant (Small Signal)	ns	50	
Output Amplifier Bandwidth	MHz	15	
Slew Rate	V/µs	80 typ, 50 min	
OUTPUT			
Voltage Output			
Voltage Ranges	V	±2.5, ±5, ±10, 0 to −5, 0 to −10	
Max Output Current	mA	10 min	
DC Output Impedance	Ω	0.05 typ; 0.1 max	
Current Output			
Current Ranges	mA	±2, 0 to +4	
Compliance	V	±0.6 max	
Output Impedance	KΩ	1.5 typ	
Short Circuit Protection		Fully protected	
DIGITAL INPUT (TTL COMPATIBLE)			
Type		12 parallel data bits, positive logic	
Coding		Unipolar ranges: Binary Bipolar ranges: Offset Binary. Also Two's Complement if the MSB complement is supplied.	
Switching Levels			
Logic "0"		±40µA at 0V to 0.8V	
Logic "1"		±40µA at +2V to +5.5V	
INTERNAL REFERENCE OUTPUT			
Voltage	V	−10.000	
Accuracy	% of Ref	±2 max for DAC-8528-11 ±1.0 max for DAC-8528-12	
External Current Capability	mA	5 max for unipolar operation 3 max for bipolar operation (2 mA required for bipolar offset)	
POWER SUPPLIES			
Voltage	V	+15 ± 3%	−15 ± 3%
Max Voltage Without Damage	V	+18	−18
Current*	mA	30 typ 40 max	15 typ 20 max
Power Supply Rejection Ratio		DAC-8528-11	DAC-8528-12
Without Trim Circuits or With Trim in Voltage Mode	%F.S.R./%P.S.	±0.0048	±0.0024
With Trim in Current Mode	%F.S.R./%P.S.	±0.0060	±0.0030
*Plus load current when in voltage mode.			
TEMPERATURE RANGES (CASE)			
Operating			
−1 Option	°C	−55 to +125	
−3 Option	°C	0 to +70	
Storage	°C	−65 to +125	
PHYSICAL CHARACTERISTICS			
Size (24 Pin Double DIP)	inch	1.4 x 0.8 x 0.2 (3.6 x 2.0 x 0.51 cm)	
Weight	oz	0.4 typ (11.3 g)	

TECHNICAL INFORMATION

INTRODUCTION

The DAC-8528 consists of a current output D/A converter plus an independent output amplifier, as shown in the block diagram, Figure 1. The ladder network generates currents which are discrete fractions of the ladder reference voltage. The fractions are determined by the digital inputs which control the current switches in the ladder. The ladder network operates from an internal reference, and this reference voltage is accessible at the REF OUT pin.

When the DAC-8528 is operated in the current mode, pin 13 serves at the output and the output amplifier is not used. For voltage mode operation pin 13 is connected to pin 14, and the voltage output is taken from the amplifier, pin 15.

CONNECTIONS FOR OUTPUT RANGES

Figure 2 shows pin connections for the five voltage output ranges using the internal feedback resistors and amplifier, and for two current ranges in which the current is taken directly from the ladder network. The feedback connection from pin 15 for voltage output should be made as close to the load as possible to minimize the effects of line and contact impedance.

CODING

Coding for the DAC-8528 is shown in the bit weight table, Figure 3. The current output coding conforms to the usual description of binary and offset binary coding. Because the output amplifier operates in an inverting mode, the voltage output has the opposite polarity. The values for full scale voltage (F.S.) and 1 LSB to be used in the bit weight table are as follows:

RANGE *	FULL SCALE (F.S.)	1 LSB
±2.5V	2.50000V	0.00122V
±5V	5.00000V	0.00244V
±10V	10.00000V	0.00488V
0 to −5V	5.00000V	0.00122V
0 to −10V	10.00000V	0.00244V
±2 mA	2.00000 mA	0.00098 mA
0 to +4 mA	4.00000 mA	0.00098 mA

*Current direction is defined as positive for currents leaving the V output.

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OUTPUT RANGE*	BIPOLAR OFFSET CONNECTION	CONNECT LOAD TO	LOAD FEEDBACK CONNECTION	OTHER PIN CONNECTIONS
±2.5V	18 to 24	15	15 to 19	13 to 14, 13 to 20
±5V	18 to 24	15	15 to 19	13 to 14
±10V	18 to 24	15	15 to 20	13 to 14
0 to −5V	18 to 16	15	15 to 19	13 to 14, 13 to 20
0 to −10V	18 to 16	15	15 to 19	13 to 14
±2 mA	18 to 24	13	—	—
0 to +4 mA	—	13	—	—

FIGURE 2. CONNECTIONS FOR VOLTAGE AND CURRENT RANGES

CURRENT OUTPUT *		DIGITAL BIT INPUTS												VOLTAGE OUTPUT	
UNIPOLAR	BIPOLAR													UNIPOLAR	BIPOLAR
BINARY	OFFSET BINARY	MSB 1	2	3	4	5	6	7	8	9	10	11	LSB 12		
+F.S. −1 LSB	+F.S. −1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	−F.S. +1 LSB	−F.S. +1 LSB
+3/4 F.S.	+1/2 F.S.	1	1	0	0	0	0	0	0	0	0	0	0	−3/4 F.S.	−1/2 F.S.
+1/2 F.S. +1 LSB	+1 LSB	1	0	0	0	0	0	0	0	0	0	0	1	−1/2 F.S. −1 LSB	−1 LSB
+1/2 F.S.	0	1	0	0	0	0	0	0	0	0	0	0	0	−1/2 F.S.	0
+1/2 F.S. −1 LSB	−1 LSB	0	1	1	1	1	1	1	1	1	1	1	1	−1/2 F.S. +1 LSB	+1 LSB
1/4 F.S.	−1/2 F.S.	0	1	0	0	0	0	0	0	0	0	0	0	−1/4 LSB	+1/2 F.S.
+1 LSB	−F.S. +1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	−1 LSB	+F.S. −1 LSB
0	−F.S.	0	0	0	0	0	0	0	0	0	0	0	0	0	+F.S.

FIGURE 3. BIT WEIGHT TABLE

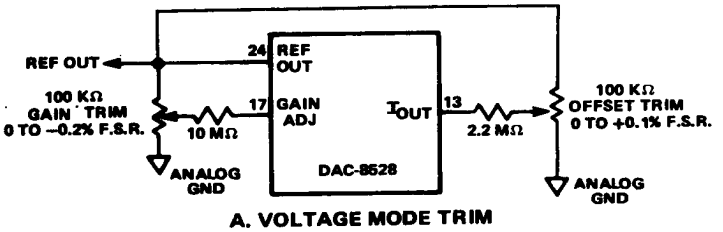
*Current direction is defined as positive for currents leaving the V output.

TRIM ADJUSTMENTS

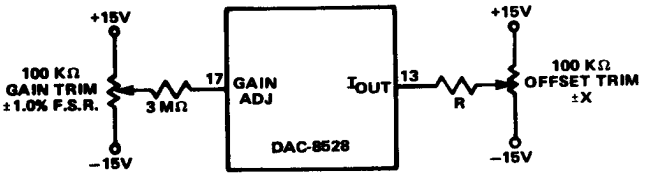
The gain and offset errors are trimmed at the factory to within the limits listed in the specifications table. With the optional trim adjustment circuits shown in Figure 4, both errors can be trimmed to zero, making the overall accuracy equal to the linearity. The fixed resistors shown in Figure 4 should be located close to the converter pins to reduce noise, and the potentiometers should have a tempco of 100 ppm/°C or less.

To trim the offset, apply the all zero's digital code. As shown in the bit table, Figure 3, this corresponds to 0 output for unipolar coding, −F.S. for bipolar current output, and +F.S. for bipolar voltage output. Adjust the offset trim potentiometer for the proper current or voltage output value in each case.

After trimming the offset, apply the all one's code to trim the gain. This corresponds to +F.S. −1 LSB for current output, and −F.S. +1 LSB for voltage output. Adjust the output to this value with the gain potentiometer.



A. VOLTAGE MODE TRIM



B. CURRENT MODE TRIM

	R	X
UNIPOLAR	2.2 MΩ	±0.15% F.S.R.
BIPOLAR	0.62 MΩ	±0.6% F.S.R.

FIGURE 4. OPTIONAL TRIM CIRCUITS

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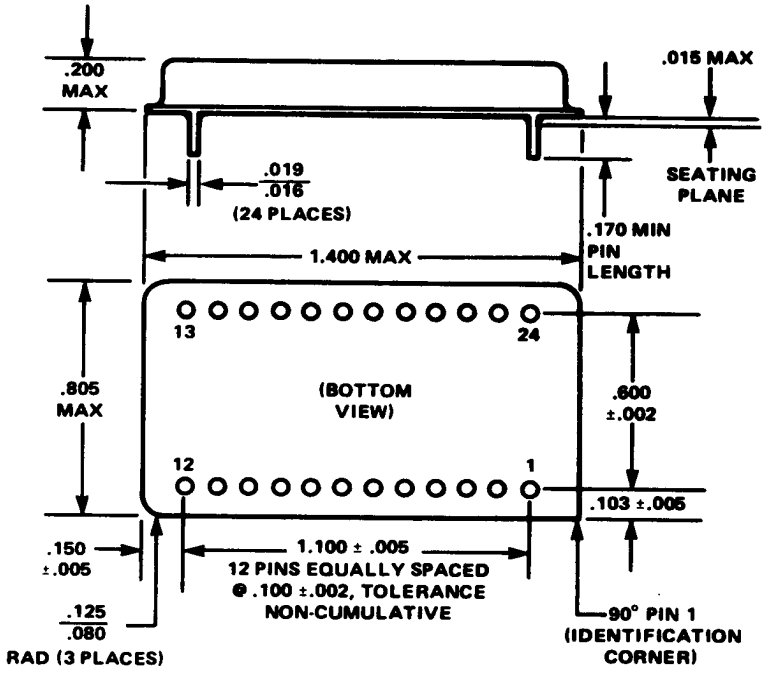
PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Bit 12 (LSB)	13	I_{OUT}
2	Bit 11	14	I_{IN}
3	Bit 10	15	V_{OUT}
4	Bit 9	16	Analog GND
5	Bit 8	17	Gain Adjust
6	Bit 7	18	Bipolar Offset
7	Bit 6	19	10V Scale
8	Bit 5	20	20V Scale
9	Bit 4	21	+15V DC
10	Bit 3	22	Power & Case GND
11	Bit 2	23	−15V DC
12	Bit 1 (MSB)	24	Ref Out

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



NOTES
1. Dimensions shown are in inches.
2. Load identification numbers are for reference only.
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Case tied to analog ground.

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DYNAMIC CHARACTERISTICS

Glitches at the output of the DAC-8528 are caused by a combination of digital data skew and stray coupling between the digital inputs and the analog output. The data skew coming into the DAC-8528 can be decreased by using a low skew holding register such as AMD type 74LS175. The physical layout around the unit should also be done carefully to minimize external coupling from input to output. Techniques such as ground planes between digital and analog runs are recommended. To optimize settling time, and to make the settling time independent of the driver characteristics, 2.2 KΩ, 1/8W pullup resistors, to the +5V logic supply, are suggested for all logic inputs.

POWER SUPPLIES AND GROUNDS

Care must be taken when distributing power supplies and grounds in high speed system to obtain optimum performance. It is recommended that 1μF tantalum capacitors be used to bypass each supply to supplement internal bypassing. The power ground, which is connected to the case, is not internally connected to analog ground and the two grounds must be connected externally.

RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

ORDERING INFORMATION

DAC-8528 – 12 – 1 – 883B

Reliability Grade:
- 883B = Fully compliant with MIL-STD-883.
- —B = Screened to MIL-STD-883 bu without QCI testing.
- Blank = Screened to MIL-STD-883 bu without pre burn-in testing, burn-in, and QCI testing.

Operating Temperature Range (Case):
- −1 = −55°C to +125°C
- −3 = 0°C to +70°C

Linearity:
- 12 = 12 bits (±0.0125%)
- 11 = 11 bits (±0.025%)

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