HI-8010 Series

CMOS High Voltage Display Driver

General Description

The HI-8010 high voltage display driver is constructed of MOS P Channel and N Channel enhancement mode devices in a single monolithic structure. It is designed to drive high voltage Liquid Crystal displays by converting low level input signals, such as TTL or CMOS, to high voltage drive signals.

The chip can drive up to 38 segments of LCD and requires minimal display-to-data source interfacing. Serial data is loaded and held in internal latches until new display data is received.

The HI-8010 is available in ceramic or plastic DIP; leaded or leadless chip carriers; and J-lead PLCC packages.

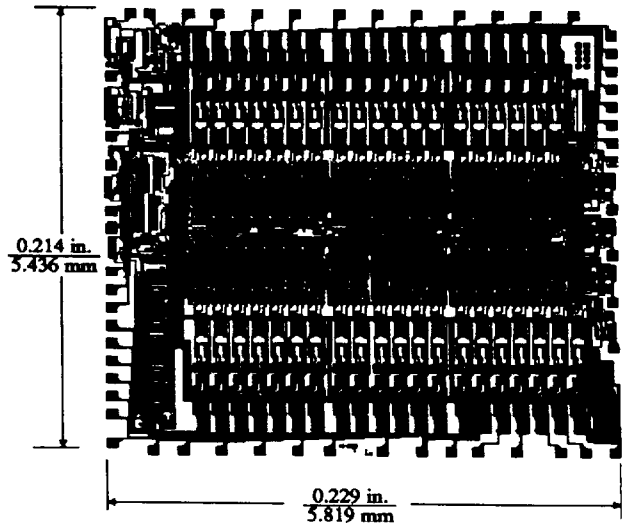
Features

- High Voltage Outputs Controlled by 5 Volt Logic
- Pin-Out Adaptable to 30, 32, 34 or 38 Segments of LCD
- RC Oscillator or External Backplane Input
- TTL Compatible Inputs with Input Protection
- Low Power Consumption
- Wide Range Supply Voltage (V_{DD}, V_{EE})
- Military Temperature Range (-55°C to +125°C)
- Pin for Pin Compatible with AMI S4520 series
- Cascadable
- Military Level Processing Available

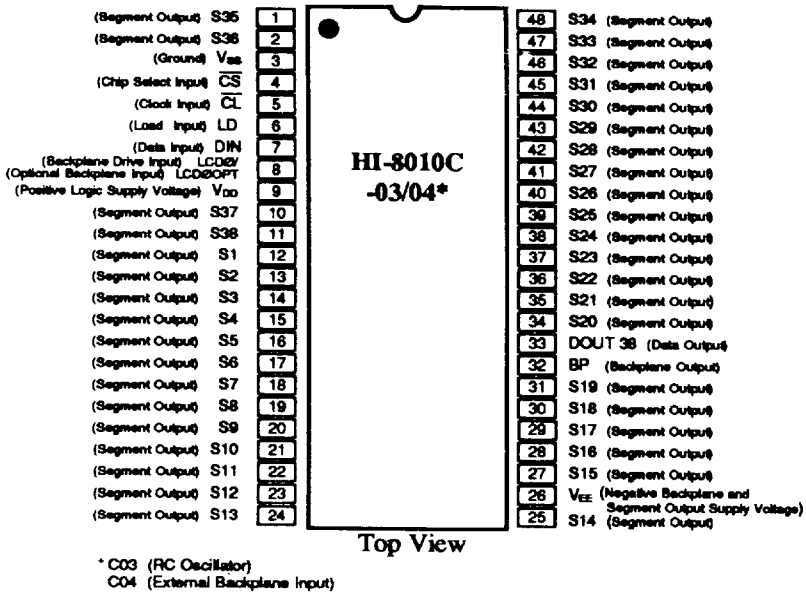
Applications

- Standard Liquid Crystal Displays
- Dichroic Liquid Crystal Displays
- Vacuum Fluorescent Displays

Chip Topography HI-8010 (Typical)



Pin Configuration (Evaluation Unit)



Top View

* C03 (RC Oscillator)
C04 (External Backplane Input)

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Functional Description

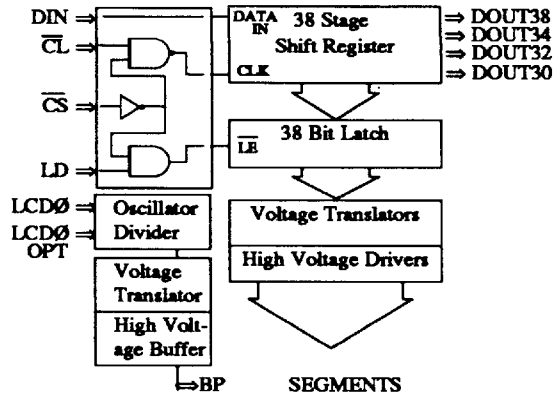
Whenever a Logic "0" is applied to the Chip Select ($\overline{CS}$) input, one bit of data is clocked into the shift register with each negative transition of the Clock ($\overline{CL}$) input ($\overline{CS}$ is internally tied to Vss on the HI-8010-06 version). A Logic "1" present at the Load (LD) input will cause a parallel transfer of data from the shift register to the data latch. If the Load (LD) input is held high while data is clocked into the shift register, the latch will be transparent.

To display segments, a Logic "1" is stored in the appropriate shift register bit position, and the segment output is out-of-phase with the backplane.

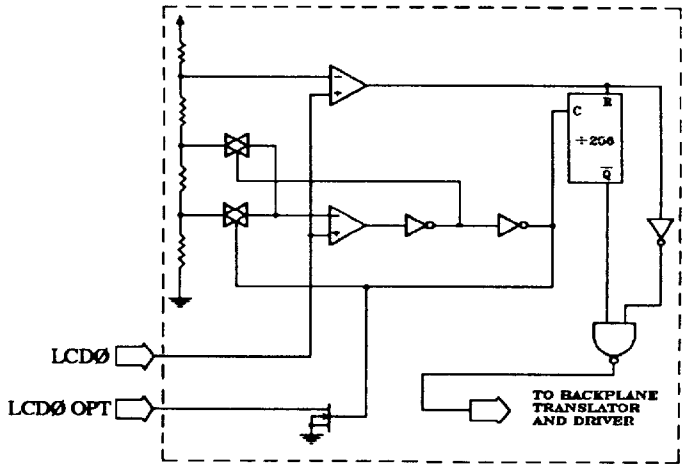
The backplane output functions in 1 of 2 modes; externally driven or self-oscillating. When the LCDØ input is externally driven, and the LCDØ OPT input is not connected (figure 1); the backplane output will be in-phase with LCDØ. Utilizing the self-oscillating mode, inputs LCDØ and LCDØ OPT are tied together and connected to an RC circuit (figure 2). (150KΩ resistor with a 470 pf capacitor generates an approximate backplane frequency of 100 Hz). The LCDØ/LCDØ OPT input frequency is divided by 256 to determine backplane output frequency.

For high voltage displays having a number of segments greater that 38, two or more of the high voltage display drivers may be cascaded together by connecting the serial data output (DOUT) from the first driver, to the serial data input (DIN) of the following driver, etc. Data out (DOUT) will change state on the rising edge of the Clock ($\overline{CL}$). Clock ($\overline{CL}$), Load (LD) and Chip Select ($\overline{CS}$) should be tied in common with each other, respectively, between all cascaded display drivers.

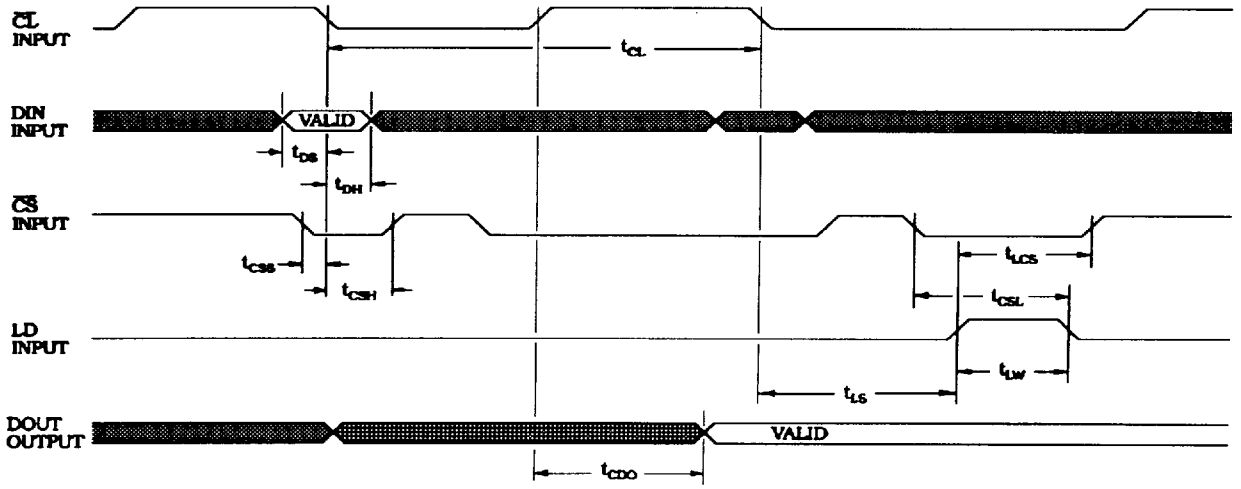
Functional Block Diagram



8010 Internal Oscillator Circuit



Timing Diagram



Absolute Maximum Ratings

(Voltages referenced to V_{SS} = 0V)

Supply Voltage V_{DD} ..... - 0.3 to + 7.0V	Power Dissipation 250mW
V_{EE} ..... V_{DD} - 35V to - 0.3V	Operating Temperature Range: plastic .... - 40°C to + 85°C
Voltage at any Input (except LCDØ) .. - 0.3V to V_{DD} + 0.3V	ceramic .. - 55°C to + 125°C
Voltage at LCDØ Input ..... V_{DD} - 35V to V_{DD} + 0.3V	Storage Temperature Range: plastic .... - 50°C to +150°C
DC Current Drain per Input Pin 10mA	ceramic .. - 65°C to + 150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

V_{DD} = 5V, V_{EE} = - 25V, V_{SS} = 0V, $T_{A(Mil.)}$ = -55°C to +125°C, $T_{A(Ind.)}$ = -40°C to +85°C (Unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage	V_{DD}		3		7	V
Supply Current	I_{DD}	Static, No Load			200	µA
	I_{EE}	Static, No Load f_{BP} = 100HZ			150	µA
Input Low Voltage (excluding LCDØ)	V_{IL}		0		1.3	V
Input High Voltage (excluding LCDØ)	V_{IH}		2		V_{DD}	V
Input Low Voltage (LCDØ)	V_{ILX}		V_{EE}		3	V
Input High Voltage (LCDØ)	V_{IHX}		3.5		V_{DD}	V
Input Current	I_{IN}	V_{IN} = 0 to 5V			1	µA
Input Capacitance	C_I				5	pf
Segment Output Impedance	R_{SEG}	I_L = 10µA			10,000	Ω
Backplane Output Impedance	R_{BP}	I_L = 10µA			450	Ω
Data Out Current	I_{DOH}	Source Current V_{OH} = 4.5V	0.6			mA
	I_{DOL}	Sink Current V_{OL} = 0.5V	- 0.6			mA

AC Electrical Characteristics

V_{DD} = 5V, V_{EE} = - 25V, V_{SS} = 0V, $T_{A(Mil.)}$ = -55°C to +125°C, $T_{A(Ind.)}$ = -40oC to +85°C (Unless otherwise specified)

PARAMETER	SYMBOL	VDD	MIN	TYP	MAX	UNITS
Clock Period	t_{CL}	5V	1200			ns
Clock Pulse Width	t_{CW}	5V	520			ns
Data In - Setup	t_{DS}	5V	50			ns
Data In - Hold	t_{DH}	5V	400			ns
Chip Select - Setup to Clock	t_{CSS}	5V	200			ns
Chip Select - Hold to Clock	t_{CSH}	5V	450			ns
Load - Setup to Clock	t_{LS}	5V	500			ns
Chip Select - Setup to Load	t_{CSL}	5V	300			ns
Load Pulse Width	t_{LW}	5V	500			ns
Chip Select - Hold to Load	t_{LCS}	5V	300			ns
Data Out Valid, from Clock	t_{CDO}	5V			800	ns

FIG. 1 Cascading: Ext. Oscillator

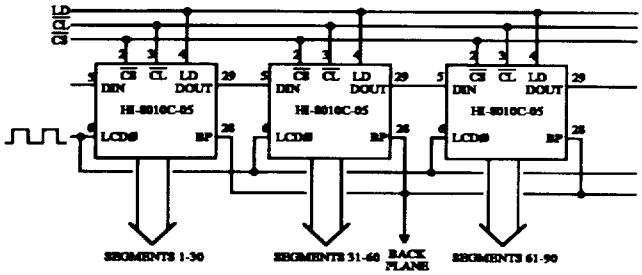
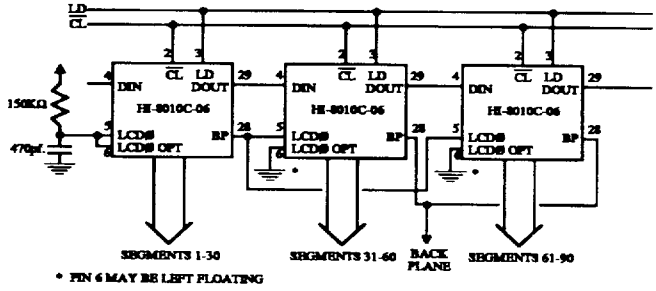
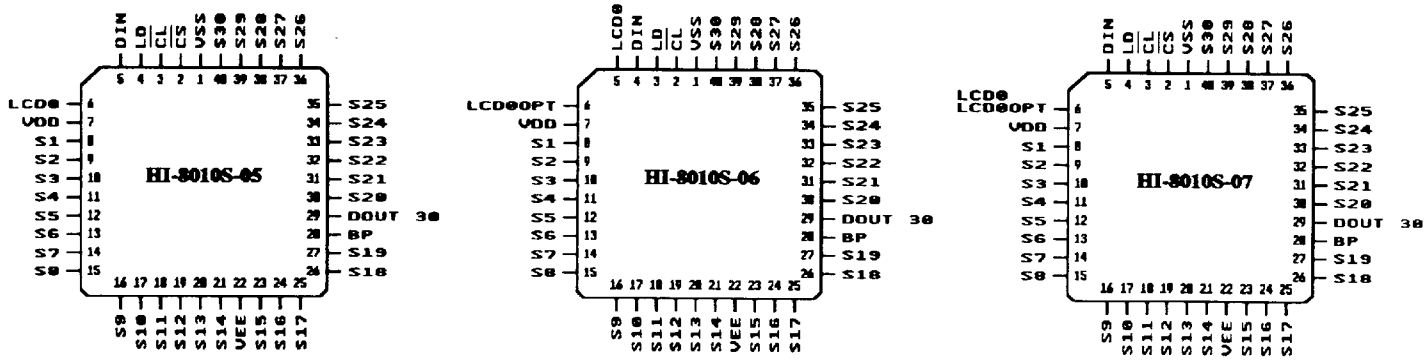


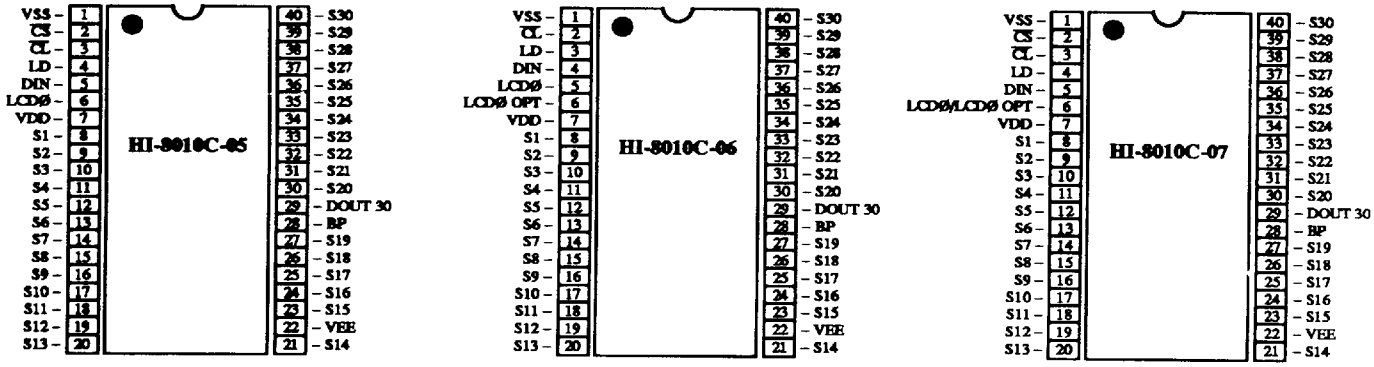
FIG. 2 Cascading: RC Oscillator



Typical Chip Carrier Pin Assignments



HI-8010 Standard Package Device Options



Ordering Information

In addition to the above standard packaging, other packaged device options are available upon request.

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