REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Corrected waveform labeling error on sheet 13. Updated boilerplate. - glg	97-09-18	Raymond Monnin

REV																			
SHEET																			
REV	A	A	A	A	A														
SHEET	15	16	17	18	19														

REV STATUS OF SHEETS															
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
96-03-20

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, MEMORY, DIGITAL, RADIATION- HARDENED, CMOS/SOS, 8K X 8 STATIC RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-95823**

SHEET 1 OF 19

DSCC FORM 2233
APR 97

5962-E176-97

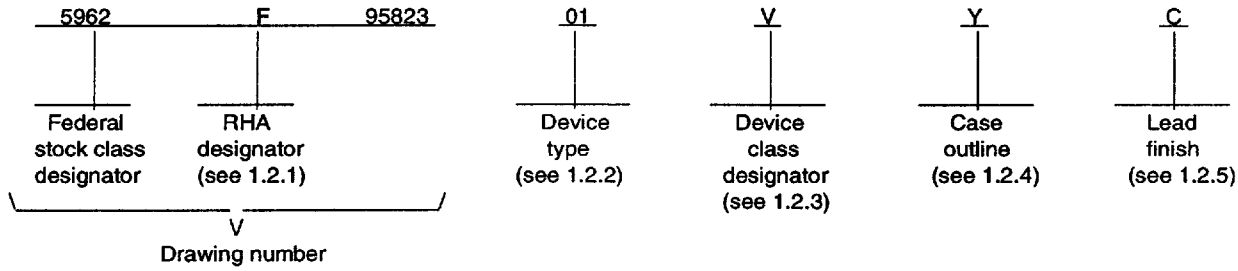
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0032010 T3T

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01	65647RH	8K X 8 Radiation hardened CMOS/SOS SRAM	50 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP2-T28	28	Dual-in-line package
Y	CDFP3-F28	28	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103 (see 6.6 herein).

1.3 Absolute maximum ratings. 2/

Supply voltage range	-0.5 V to +7.0 V dc
Input, output, or I/O voltage	-0.3 V dc to V_{DD} +0.3 V dc
Maximum package power dissipation (P_D) at T_A = +125°C	
Case X	1.11 W 3/
Case Y	0.94 W 3/
Lead temperature (soldering, 10 seconds maximum)	+300°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X	8.0°C/W
Case Y	7.4°C/W
Thermal resistance, junction-to-ambient (Θ_{JA}):	
Case X	45.0°C/W
Case Y	53.4°C/W
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0.0 V dc
Input high voltage (V_{IH})	0.8V_{DD} to V_{DD}
Input Low voltage (V_{IL})	0.0 V dc to 0.2V_{DD}
Case operating temperature range (T_C)	-55°C to +125°C
Input rise and fall time	40 ns max
Radiation features:	
Total dose irradiation	≥ 300 KRads(Si)
Dose rate upset (20 ns pulse)	≥ 1 x 10^{11} Rads(Si)/sec 4/
Dose rate survivability	≥ 1 x 10^{12} Rads(Si)/sec 4/
Single event phenomenon (SEP) effective linear energy threshold (LET) with no upsets	≥ 100 MeV/(cm^2/mg) 4/
Latchup	None 4/
Cosmic ray upset immunity	< 1 x 10^{-10} errors/bit-day 4/ 5/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ If device power exceeds package dissipation capability, provide heat sinking or derate linearly (the derating is based on Θ_{JA}) at the following rate: case outline X - - - 22.2 mW/°C, case outline Y - - - 18.7 mW/°C.
4/ Guaranteed by process or design, but not tested.
5/ Single event upset error rates are obtained using Adams 10% worst case environment under worst case conditions.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document , however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified in table III.

3.2.5 Functional tests. Functional tests used to test this device shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified, the electrical performance characteristics, and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

Table I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits 1/ Min	Limits 1/ Max	Unit
High level output voltage	V_{OH}	V_{DD} = 4.5 V, I_{OH} = -5.0 mA V_{IN} = GND or V_{DD}		1,2,3	01	V_{DD} - 0.4		V
			M,D, L,R, F	1 2/		3/		V
Low level output voltage	V_{OL}	V_{DD} = 4.5 V, I_{OL} = 8.0 mA, V_{IN} = GND or V_{DD}		1,2,3	01		0.4	V
			M,D, L,R, F	1 2/			3/	V
Input leakage current	I_{IN}	V_{DD} = 5.5 V, V_{IN} = GND or V_{DD}		1,2,3	01	-1	1	µA
			M,D, L,R, F	1 2/		3/	3/	µA
High impedance output leakage current	I_{OZ}	V_{DD} = 5.5 V, V_{IN} = V_{OUT} = GND or V_{DD} E_1 = V_{DD}, E_2 = GND		1,3 4/ 2	01	-10 -30 -60	10 30 60	µA
			M,D, L,R, F	1 2/		-60	60	µA
Operating supply current 5/	I_{DDOP}	V_{DD} = 5.5 V, f= 2 MHz, V_{IN} = GND or V_{DD} E_1 = GND, E_2 = V_{DD} I_{OUT} = 0 MA		1 2 3	01		95 85 110	mA
			M,D, L,R, F	1 2/			110	mA
Standby supply current 6/	I_{DDSB}	V_{DD} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = GND or V_{DD}, E_1 = V_{DD}, E_2 = GND		1,3 4/ 2	01		500 4 10	µA mA
			M,D, L,R, F	1 2/			10	mA
Enable supply current	I_{DDEN}	V_{DD} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = GND or V_{DD}, E_1 = GND, E_2 = V_{DD}		1 2 3	01		90 81 105	mA
			M,D, L,R, F	1 2/			105	mA

See footnotes at end of table.

Table I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits 1/ Min	Limits 1/ Max	Unit
Data retention current	I_{DDDR}	V_{DD} = 2.0, I_{OUT} = 0 mA V_{IN} = GND or V_{DD} $E_1 = V_{DD}$, E_2 = GND		1,3	01		100	µA
				4/			1	mA
				2			4	
			M,D, L,R, F	1 2/			6	mA
Input capacitance 7/	C_{IN}	V_{DD} = open, f = 1.0 MHz, see 4.4.1c		4	01		12	pF
I/O capacitance 7/	$C_{I/O}$	V_{DD} = open, f = 1.0 MHz, see 4.4.1c		4	01		12	pF
Functional tests	FT	See 4.4.1d, V_{DD} = 4.5 V and 5.5 V f = 1 MHz, V_{IN} = GND or V_{DD}		7,8A,8B	01			
			M,D, L,R, F	7 2/		3/		
Noise immunity functional test	FN	V_{DD} = 4.5 V, f = 1 MHz, $V_{IH} = 0.8V_{DD}$, $V_{IL} = 0.2V_{DD}$		7,8A,8B	01			
			M,D, L,R, F	7 2/		3/		
Read cycle 7/	t_{AVAX}	See figure 3, V_{DD} = 4.5 V and 5.5 V 8/		9,10,11	01	50		ns
Address access time	t_{AVQV}	See figure 3, V_{DD} = 4.5 V 8/		9,10,11	01		50	ns
			M,D, L,R, F	9 1/			2/	ns
Output hold from address 7/	t_{AXQX}	See figure 3, V_{DD} = 4.5 V and 5.5 V 8/		9,10,11	01	0		ns
Chip enable access time	t_{E1LQV} t_{E2HQV}	See figure 3, V_{DD} = 4.5 V 8/		9,10,11	01		50	ns
			M,D, L,R, F	9 2/			3/	ns
Chip enable to output active 7/	t_{E1LQX} t_{E2HQX}	See figure 3, V_{DD} = 4.5 V and 5.5 V 8/		9,10,11	01	0		ns
Chip enable to output in high Z 7/	t_{E1HQZ} t_{E2LQZ}			9,10,11	01		15	ns

See footnotes at end of table.

Table I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits 1/		Unit
						Min	Max	
Output enable access time	t_{GLQV}	See figure 3, V_{DD} = 4.5 V 8/		9,10,11	01		15	ns
			M,D,L,R,F	9 2/			3/	ns
Output disable to output in high Z 7/	t_{GHQZ}	See figure 3, V_{DD} = 4.5 V and 5.5 V 8/		9,10,11	01		15	ns
Output enable to output active 7/	t_{GLQX}			9,10,11	01	0		ns
Write cycle 7/	t_{AVAX}	See figure 3, V_{DD} = 4.5 V 8/		9,10,11	01	50		ns
Address setup time	t_{AVE1L} t_{AVE2H} t_{AVWL}			9,10,11	01	5		ns
			M,D,L,R,F	9 2/		3/		ns
Write enable pulse width	t_{WLWH}			9,10,11	01	25		ns
			M,D,L,R,F	9 2/		3/		ns
Write recovery time	t_{WHAX} t_{E1HAX} t_{E2LAX}			9,10,11	01	0		ns
			M,D,L,R,F	9 2/		3/		ns
Data to write set-up time	t_{DVWH} t_{DVE1H} t_{DVE2L}			9,10,11	01	30		ns
			M,D,L,R,F	9 2/		3/		ns
Write enable high to output active 7/	t_{WHQX}	See figure 3, V_{DD} = 4.5 V and 5.5 V 8/		9,10,11	01	0		ns
Data hold time	t_{WHDX} t_{E1HDX} t_{E2LDX}	See figure 3, V_{DD} = 4.5 V 8/		9,10,11	01	0		ns
			M,D,L,R,F	9 2/		3/		ns

See footnotes at end of table.

Table I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits 1/		Unit
						Min	Max	
Write enable to output high Z 7/	t_{WLQZ}	See figure 3, V_{DD} = 4.5 V and 5.5 V 8/		9,10,11	01		10	ns
Chip enable to end of write	t_{E1LE1H} t_{E2HE2L}	See figure 3, V_{DD} = 4.5 V 8/		9,10,11	01	35		ns
			M,D, L,R, F	9 2/		3/		ns
Address hold time	t_{AVE1H} t_{AVE2L}			9,10,11	01	40		ns
			M,D, L,R, F	9 2/		3/		ns

1/ This device also receives 100% testing and group A sample inspection at +85°C. Unless otherwise specified, the limit is the same as defined at +125°C.
2/ When performing postirradiation electrical measurements for any RHA level T_A = +25°C. Limits shown are guaranteed at T_A = +25°C ±5°C. The M, D, L, R, and F in the test condition column are the postirradiation limits for the device types specified in the device types column.
3/ Preirradiation values for RHA marked devices shall also be the postirradiation values, unless otherwise specified.
4/ Limit at +85°C.
5/ For each 1MHz increase in address frequency, there is a 3mA(typical) increase in operating supply current.
6/ In order for this device to be in low power standby mode, E_2 must be disabled (low).
7/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
8/ AC measurements assume rise and fall times of 5 ns or less, timing reference levels of 2.0 V, input pulse levels of 0 to V_{DD}, and the output load = 1 TTL equivalent load and $C_L \ge 50$ pF. For $C_L > 50$ pF, access times are derated 0.15ns/pF.

Device types	All
Case outlines	X,Y
Terminal number	Terminal symbol
1	NC
2	A_{12}
3	A_7
4	A_6
5	A_5
6	A_4
7	A_3
8	A_2
9	A_1
10	A_0
11	DQ_0
12	DQ_1
13	DQ_2
14	GND
15	DQ_3
16	DQ_4
17	DQ_5
18	DQ_6
19	DQ_7
20	$\overline{E}_1$
21	A_{10}
22	$\overline{G}$
23	A_{11}
24	A_9
25	A_8
26	E_2
27	$\overline{W}$
28	V_{DD}

FIGURE 1. Terminal connections.

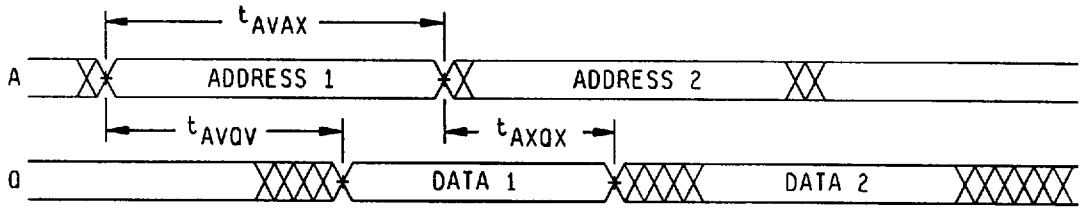
Read modes

Mode	$\overline{E}_1$	E_2	$\overline{G}$	$\overline{W}$	Outputs
Low power supply	X	L	X	X	High Z
Disabled	H	H	X	X	High Z
Enabled	L	H	H	H	High Z
Read	L	H	L	H	Data out
Write	L	H	X	L	Data in

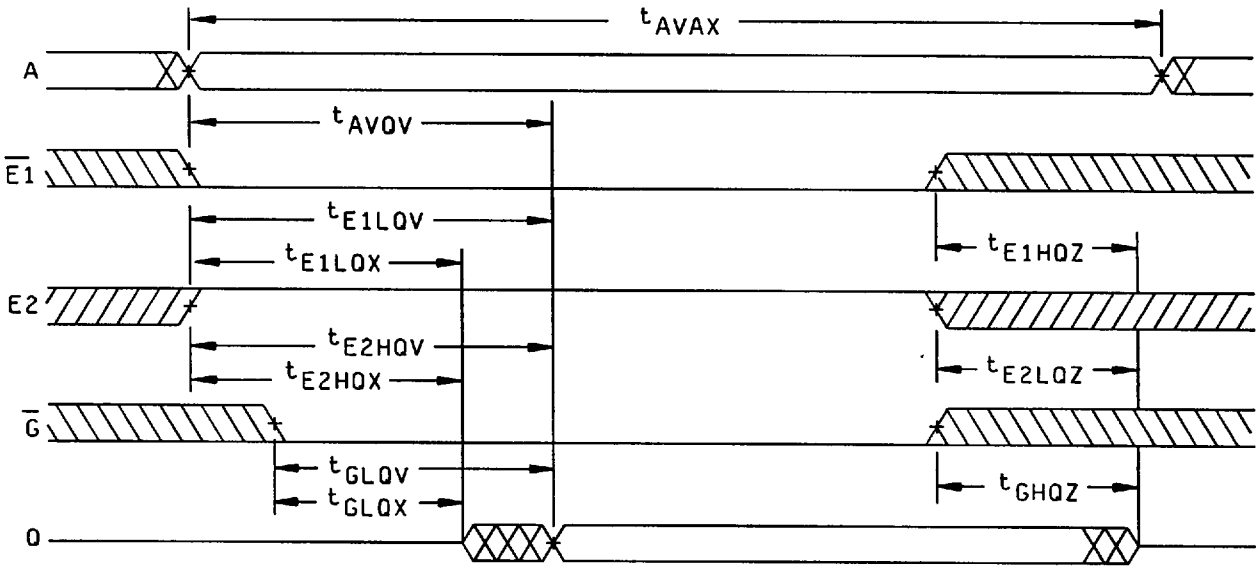
NOTES:
1. L = logic low voltage level; H = logic high voltage level; X can be H or L.
2. High Z is high impedance state.

FIGURE 2. Truth table.

Read cycle 1 (see note 1)



Read cycle 2 (see note 2)



NOTES:
1. $\overline{W}$ and E_2 are high, $\overline{G}$ and $\overline{E}_1$ are low.
2. W is high.

FIGURE 3. Timing waveforms.

Write cycle 1: Late write

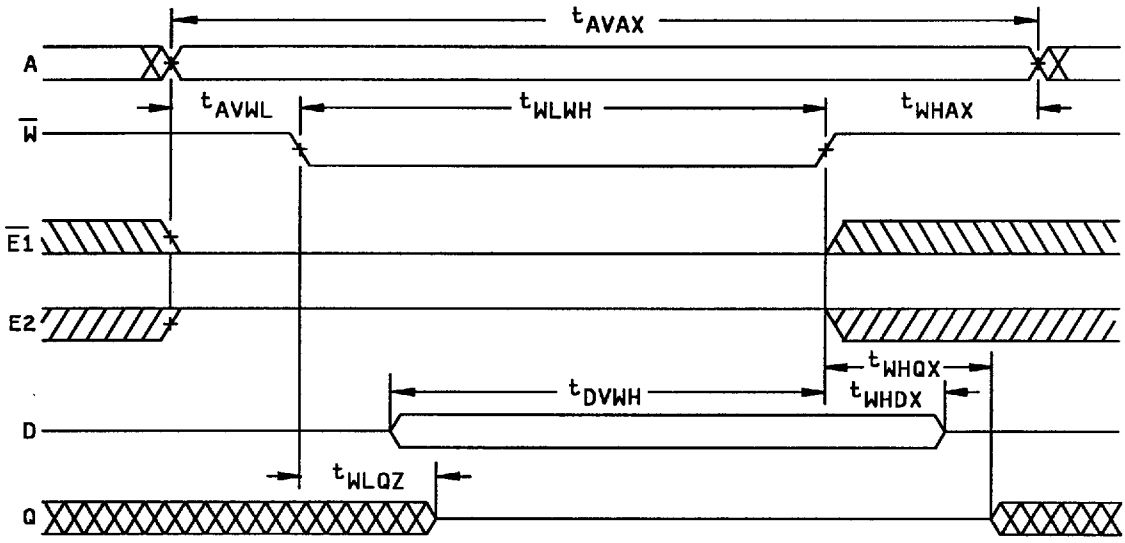


FIGURE 3. Timing waveforms - continued.

Write cycle 2: Early write, E_1 controlled

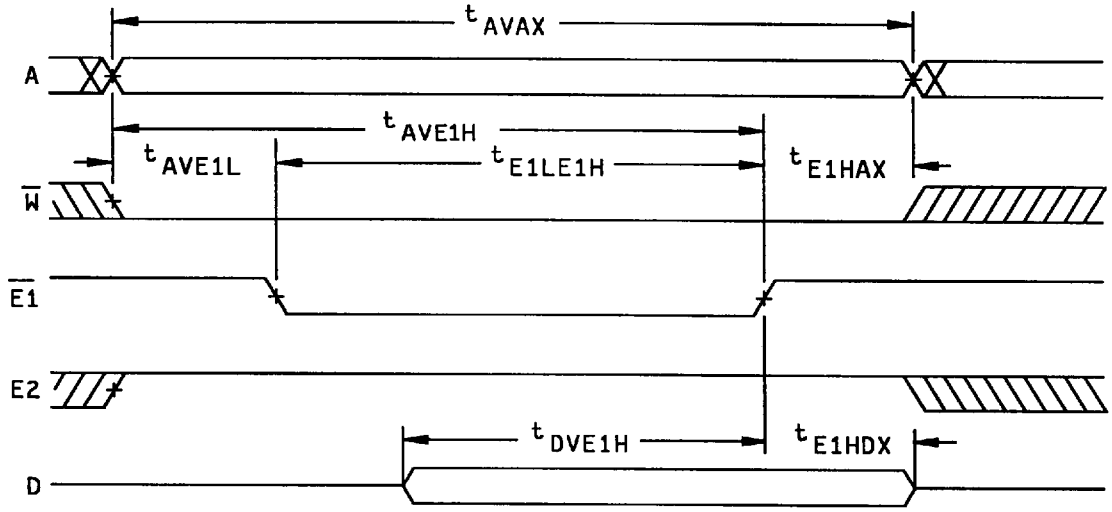


FIGURE 3. Timing waveforms - continued.

Write cycle 3: Early write, E_2 controlled

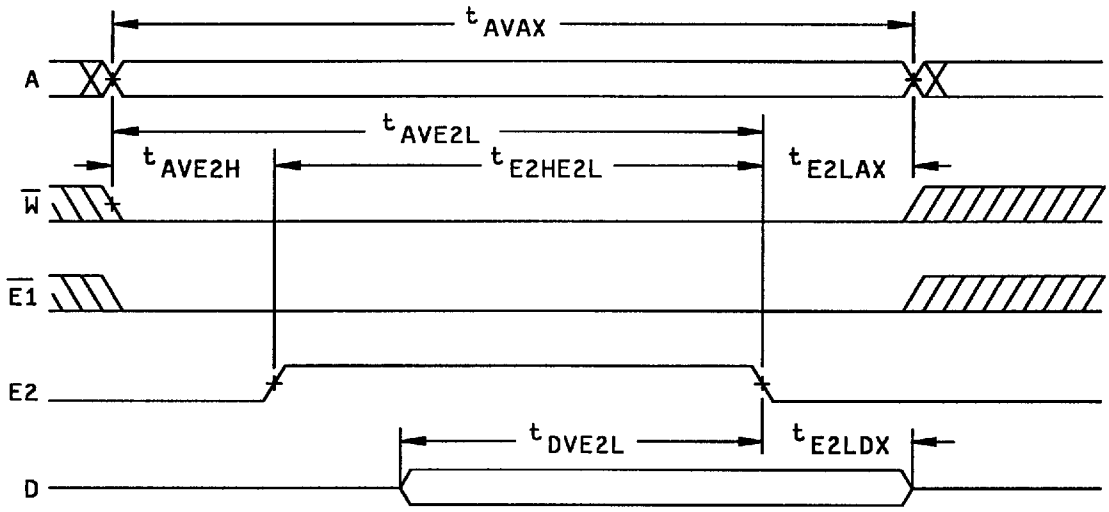


FIGURE 3. Timing waveforms - continued.

Table IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005, table IA)	Subgroups (per MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9
2	Static burn-in I method 1015	Not required	Not required	Required
3	Same as line 1			1*,7*,9 Δ*
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7*,9 Δ*
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
7	Group A test requirements	1,2,3,4**,7,8A ,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	1,2,3,7, 8A,8B	1,2,3,7, 8A,8B,9,10, 11	1,2,3,7, 8A,8B,9,10, 11 Δ
9	Group D end-point electrical parameters	1,7,9	1,7,9	1,7,9
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate test are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * Indicates PDA applies to subgroups 1, 7, and Δ.
5/ ** See 4.4.1c.
6/ Δ Indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the zero hour electrical parameters (see table IIA).
7/ See 4.5.

Table IIB. Delta limits at +25°C.

Test 1/	All device types
I_{IN}	±150 nA of specified value in table I
I_{OZ}	±2 µA of specified value in table I
I_{DDSB}	±150 µA of specified value in table I
V_{OL}	±60 mV of specified value in table I
V_{OH}	±150 mV of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

Table III. Irradiation test connections. 1/

Case	Open	Ground	V_{DD} = 5.5 V ± 0.5 V
X,Y	1	3,5,7,9,11,13,14, 16,18,23,24,26	2,4,6,8,10,12,15,17, 19,20,21,22,25,27,28

1/ Each pin except V_{DD}, NC, and GND will have a series resistor of 10kΩ ± 10%, for irradiation testing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition, and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 or as modified in the device manufacturer's QM plan.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535 or as modified in the device manufacturers Quality Management (QM) plan.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and $C_{I/O}$ measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 Mhz. Sample size is 5 devices with no failures, and all input and output devices tested.

d. For device class M, subgroups 7, 8A and 8B tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7, 8A and 8B shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. For group D inspection, end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.4). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (see 1.4).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices (see 1.4 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at inital qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be +25 °C and the maximum rated operating temperature ±10 °C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1693, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

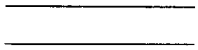
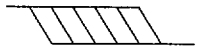
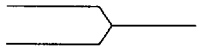
6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Symbols, definitions, and functional descriptions.

C_{IN} ..... Input terminal capacitance.
C_{OUT} ..... Output terminal capacitance.
GND ..... Ground zero voltage potential.
I_{DD} ..... Supply current.
I_I ..... Input current.
I_O ..... Output current.
T_C ..... Case temperature.
V_{DD} ..... Positive supply voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. For example, address setup time would be shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. For example, the access time would be shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurence of latchup (SEP).

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-09-18

Approved sources of supply for SMD 5962-95823 are listed below for immediate acquisition only and shall be added to QML-38535 and MIL-HDBK-103 during the next revision. QML-38535 and MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of QML-38535 and MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F9582301QXC	34371	HS1-65647RH-8
5962F9582301VXC	34371	HS1-65647RH-Q
5962F9582301QYC	34371	HS9-65647RH-8
5962F9582301VYC	34371	HS9-65647RH-Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Harris Semiconductor P. O. Box 883 Melbourne, FL 32902-0883

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.