Intel® 80331 I/O Processor

Datasheet

Product Features

- Integrated Intel XScale® core
  - —500, 667 and 800 MHz
  - —ARM* V5TE Compliant
  - —32 KByte, 32-way Set Associative Instruction Cache with cache locking
  - —32 KByte, 32-way Set Associative Data Cache with cache locking. Supports write through or write back
  - —2 KByte, 2-way Set Associative Mini-Data Cache
  - —128-Entry Branch Target Buffer
  - —8-Entry Write Buffer
  - —4-Entry Fill and Pend Buffer
  - —Performance Monitor Unit
- Internal Bus 266 MHz/64-bit
  - —333 MHz on D-0 stepping.
- PCI-X to PCI-X Bridge
  - —Primary and Secondary 133MHz/64-bit PCI-X Interfaces
  - —8K byte Data Buffers
  - —Four Secondary PCI Output Clocks
  - —Secondary Bus Arbitration
  - —Private Device and Private Memory
- Address Translation Unit
  - —2 KB or 4 KB Outbound Read Queue
  - —4 KB Outbound Write Queue
  - —4 KB Inbound Read and Write Queue
  - —Connects Internal Bus to PCI/X Bus A
  - —Messaging Unit and Expansion ROM
- Two Programmable 32-bit Timers and Watchdog Timer
- Eight General Purpose I/O Pins
- Two I^2C Bus Interface Units
- Memory Controller
  - —PC2700 Double Data Rate (DDR333) SDRAM
  - —DDRII 400 SDRAM
  - —Up to 2 GB of 64-bit DDR333
  - —Up to 1 GB of 64-bit DDRII400
  - —Optional Single-bit Error Correction, Multi-bit Detection Support (ECC)
  - —Supports Unbuffered or Registered DIMMs and Discrete SDRAM
  - —32-bit memory support
- DMA Controller
  - —Two Independent Channels Connected to Internal Bus
  - —Two 1KB Queues in Ch0 and Ch1
  - —CRC-32C Calculation
- Application Accelerator UnitRAID 6 support on D-0 stepping
  - —Performs optional XOR on Read Data
  - —Compute Parity Across Local Memory Blocks
  - —1 KB/512-byte Store Queue
- Two UART (16550) Units
  - —64-byte Receive and Transmit FIFOs
  - —4-pin, Master/Slave Capable
- Peripheral Bus Interface
  - —8-/16-bit Data Bus with Two Chip Selects
- Interrupt Controller Unit
  - —Four Priority Levels
  - —Vector Generation
  - —Twelve External Interrupt Pins with High Priority Interrupt (HPI#)
- 829-Ball, Flip Chip Ball Grid Array (FCBGA)
  - —37.5 mm^2 and 1.27 mm ball pitch

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Revision History

Date	Revision #	Description
August 2005	004	Updated voltages in Section 4.3.
March 2005	003	Revised: Table 14, modified pin mode behavior for DQ[63:32] for 32-bit DDR. Table 19, modified Case Temperature Under Bias to 95° C Max Table 20, modified Case Temperature Under Bias to 95° C Max Table 21, modified Vol1 and Voh1 parameters Table 23, added note 4. Table 24, added note 2. Table 25, modified Tvb4 and Tva4. Figure 12, removed Tvb6 parameter.
November 2004	002	Added D-0 text to Product Features and body text. Revised Ball Maps and Signal designations for intel® 80331 I/O processor design. Added ICC numbers to Table 22.
September 2003	001	Initial Release.

1.0 Introduction

1.1 About This Document

This is the *Intel® 80331 I/O Processor Datasheet*. This document contains a functional overview, package signal locations, targeted electrical specifications, and bus functional waveforms. Detailed functional descriptions other than parametric performance are published in the *Intel® 80331 I/O Processor Developer's Manual*.

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1.1.1 Terminology

To aid the discussion of the Intel® 80331 I/O processor (80331) architecture, the following terminology is used:

Core processor	Intel XScale® core within the 80331
Local processor	Intel XScale® core within the 80331
Host processor	Processor located upstream from the 80331
Local bus	80331 Internal Bus
Local memory	Memory subsystem on the Intel XScale® core, Memory Controller or Peripheral Bus Interface busses.
Inbound	At or toward the Internal Bus of the 80331 from the PCI interface of the ATU.
Outbound	At or toward the PCI interface of the 80331 ATU from the Internal Bus.
Downstream	At or toward the Secondary PCI interface from the Primary PCI interface.
Upstream	At or toward the Primary PCI interface from the Secondary PCI interface.
QWORD	64-bit data quantity (8 bytes).
DWORD	32-bit data quantity (4 bytes).
word	16-bit data quantity (2 bytes).

1.1.2 Other Relevant Documents

1. *Intel XScale® Core Developer's Manual* (273473), Intel Corporation.
2. *Intel® 80331 I/O Processor Developer's Manual* (273942), Intel Corporationl.
3. *Intel® 80331 I/O Processor Design Guide* (273823), Intel Corporationl.
4. *Intel® 80331 I/O Processor Specification Update* (273930), Intel Corporationl.
5. *PCI-to-PCI Bridge Architecture Specification,* Revision 1.1 - PCI Special Interest Group.
6. *PCI Local Bus Specification*, Revision 2.3 - PCI Special Interest Group.
7. *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a - PCI Special Interest Group.
8. *PCI Bus Power Management Interface Specification*, Revision 1.1 - PCI Special Interest Group.

1.2 About the Intel® 80331 I/O Processor

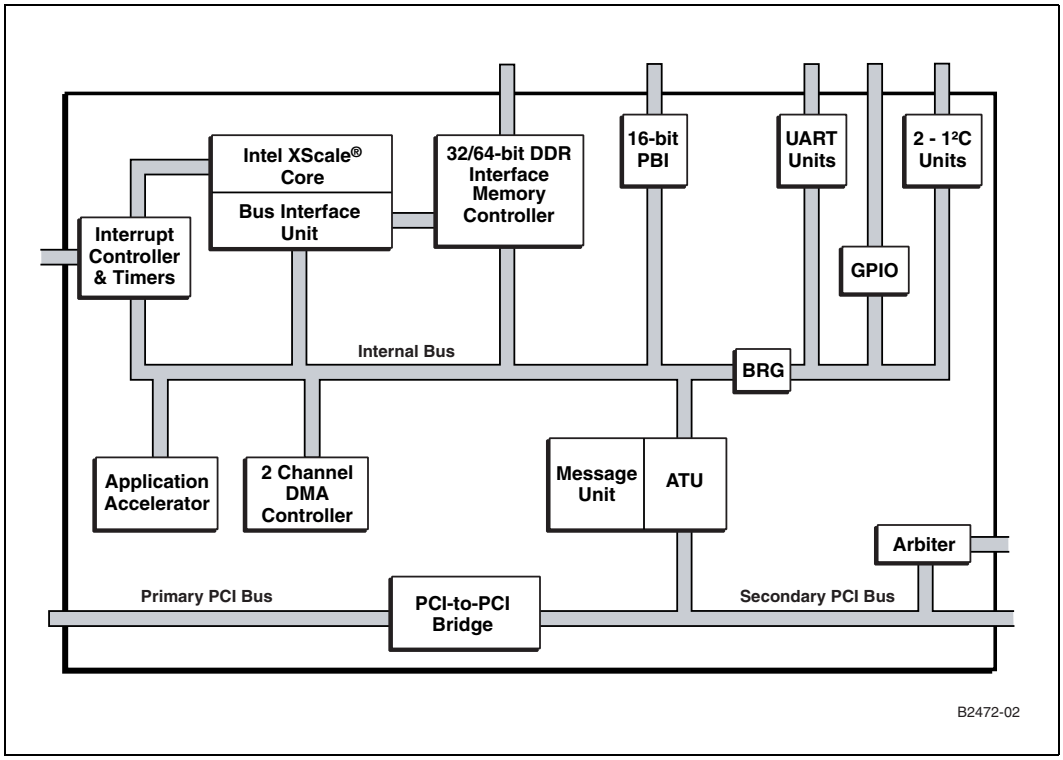
The 80331 is a multi-function device that integrates the Intel XScale® core (ARM* architecture compliant) with intelligent peripherals and PCI-X to PCI-X Bridge. The 80331 consolidates, into a single system:

- Intel XScale® core.
- PCI-to-PCI Bridge supporting PCI-X interfaces on the Primary and Secondary bus.
- Address Translation Unit (PCI-to-Internal Bus Application Bridge) interfaced to the Secondary Bus.
- High-Performance Memory Controller.
- Interrupt Controller with up to 12 external interrupt inputs.
- Two Direct Memory Access (DMA) Controllers.
- Application Accelerator.
- Messaging Unit.
- Peripheral Bus Interface Unit.
- Two I^2C Bus Interface Units.
- Two 16550 compatible UARTs with flow control (four pins).
- Eight General Purpose Input Output (GPIO) ports.

It is an integrated processor that addresses the needs of intelligent I/O applications and helps reduce intelligent I/O system costs.

Figure 1 is a functional block diagram of the 80331.

Figure 1. Intel® 80331 I/O Processor I/O Processor Functional Block Diagram



2.0 Features

The 80331 combines the Intel XScale® core with powerful new features to create an intelligent I/O processor. This multi-device I/O Processor is fully compliant with the *PCI Local Bus Specification*, Revision 2.3 and the *PCI-to-PCI Bridge Architecture Specification*, Revision 1.1. The 80331-specific features include:

- Intel XScale® core
- Application Accelerator Unit
- Address Translation Unit
- Memory Controller
- Peripheral Bus Interface
- Two I2C Bus Interface Units
- PCI-X to PCI-X Bridge with Primary and Secondary 133 MHz/64-bit PCI-X Interfaces
- Interrupt Controller Unit
- Messaging Unit
- Internal Bus
- Two DMA Controllers
- Two UART Units
- Eight GPIOs

The subsections that follow briefly overview each feature. Refer to the *Intel® 80331 I/O Processor Developer's Manual* for full technical descriptions.

2.1 Intel XScale® Core

The 80331 is based upon the Intel XScale® core. The core processor operates at a maximum frequency of 800 MHz. The instruction cache is 32 Kbytes in size and is 32-way set associative. Also, the core processor includes a data cache that is 32 Kbytes and is 32-way set associative, and a mini data cache that is 2 Kbytes and is two-way set associative.

2.2 PCI-to-PCI Bridge Unit

The 80331 provides a PCI-X to PCI-X Bridge unit. The bridge Primary and Secondary PCI-X support 64-bit 133 MHz interfaces compliant to the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a.

2.3 Address Translation Unit

An Address Translation Unit (ATU) allows PCI transactions direct access to the 80331 local memory. The ATU supports transactions between PCI address space and 80331 address space. Address translation for the ATU is controlled through programmable registers accessible from both the PCI interface and the Intel XScale® core. The PCI interface of the ATU is connected to the 80331 Secondary PCI interface of the bridge. Upstream access to the Primary PCI interface is controlled by inverse decode with the address windows of the bridge. Dual access to registers allows flexibility in mapping the two address spaces. The ATU also supports the power management extended capability configuration header that as defined by the *PCI Bus Power Management Interface Specification*, Revision 1.1.

2.4 Memory Controller

The Memory Controller allows direct control of a DDR SDRAM memory subsystem. It features programmable chip selects and support for error correction codes (ECC). The memory controller may be configured for DDR SDRAM at 333 MHz (with 500 MHz and 667 MHz processors) or DDR-II SDRAM at 400 MHz (with 500 MHz and 800 MHz processors). The memory controller interface configuration support includes Unbuffered DIMMs, Registered DIMMs, and discrete DDR SDRAM devices. The memory contoller is dual-ported, with a dedicated interface for the Intel XScale® core Bus Interface Unit and a second interface to the Internal Bus.

External memory may be configured as host addressable memory or private 80331 memory utilizing the Address Translation Unit and Bridge.

2.5 Application Accelerator Unit

The Application Accelerator Unit (AA) provides low-latency, high-throughput data transfer capability between the AA unit, the 80331 local memory and the PCI bus. It executes data transfers from and to the 80331 local memory, from the PCI bus to the 80331 local memory, or from the 80331 local memory to the PCI bus. The AA unit performs XOR operations, computes parity, generates and verifies an eight byte data integrity field, performs memory block fills, and provides the necessary programming interface. The AAU has been enhanced to support RAID 6 in the D-0 stepping of the 80331.

2.6 Peripheral Bus Interface

The Peripheral Bus Interface Unit is a data communication path to the flash memory components or other peripherals of an 80331 hardware system. The PBI includes support for either 8/16 bit devices. To perform these tasks at high bandwidth, the bus features a burst transfer capability which allows successive 8/16-bit data transfers.

2.7 DMA Controller

The DMA Controller allows low-latency, high-throughput data transfers between PCI bus agents and the local memory. Two separate DMA channels accommodate data transfers to the PCI bus. Both channels include a local memory to local memory transfer mode. The DMA Controller supports chaining and unaligned data transfers. It is programmable through the Intel XScale® core only.

2.8 I²C Bus Interface Unit

The I²C (Inter-Integrated Circuit) Bus Interface Unit allows the Intel XScale® core to serve as a master and slave device residing on the I²C bus. The I²C unit uses a serial bus developed by Philips Semiconductor*, consisting of a two-pin interface. The bus allows the 80331 to interface to other I²C peripherals and microcontrollers for system management functions. It requires a minimum of hardware components for an economical system to relay status and reliability information on the I/O subsystem to an external device. Also refer to I²C *Peripherals for Microcontrollers* (Philips Semiconductor).

The 80331 includes two I²C bus interface units.

2.9 Messaging Unit

The Messaging Unit (MU) provides data transfer between the PCI system and the 80331. It uses interrupts to notify each system when new data arrives. The MU has four messaging mechanisms:

- Message Registers
- Doorbell Registers
- Circular Queues
- Index Registers

Each messaging mechanism allows a host processor or external PCI device and the 80331 to communicate through message passing and interrupt generation.

2.10 Internal Bus

The Internal Bus is a high-speed interconnect between internal units and Intel XScale® core processor. The Internal Bus operates at 266 MHz and is 64 bits wide. The internal bus on the D-0 stepping of the 80331 operates at 333MHz.

2.11 UART Units

The 80331 includes two UART units. The UART units allow the Intel XScale® core to serve as a master and slave device residing on the UART bus. The UART units use a serial bus consisting of a four-pin interface. The bus allows the 80331 to interface to other peripherals and microcontrollers. Also refer to *16550 Device Specification* (National Semiconductor*).

2.12 Interrupt Controller Unit

The Interrupt Controller Unit (ICU) aggregates interrupt sources both external and internal of the 80331 to the Intel XScale® core processor. The ICU supports high performance interrupt processing with direct interrupt service routine vector generation on a per source basis. Each source has programmability for masking, core processor interrupt input, and priority.

2.13 GPIO

The 80331 includes eight General Purpose I/O (GPIO) pins which can also be used as external interrupt inputs.

3.0 Package Information

The 80331 is offered in a Flip Chip Ball Grid Array (FCBGA) package. This is a full grid array package with 829 ball connections.

3.1 Functional Signal Descriptions

Table 1. Pin Description Nomenclature

Symbol	Description
C	Configuration
I	Input pin only
O	Output pin only
I/O	Pin may be either an input or output.
OD	Open Drain pin
PWR	Power pin
GND	Ground pin
-	Pin must be connected as described.
Sync(...)	Synchronous. Signal meets timings relative to a clock. Sync(P) Synchronous to **P_CLK** Sync(M) Synchronous to **M_CK[2:0]** Sync(S) Synchronous to **S_CLKIN** Sync(T) Synchronous to **TCK**
Async	Asynchronous. Inputs may be asynchronous relative to all clocks. All asynchronous signals are level-sensitive.
Rst(P)	The pin is reset with **P_RST#**
Rst(S)	The pin is reset with **S_RST#**. Note that **S_RST#** is asserted when **P_RST#** is asserted.
Rst(M)	The pin is reset with **M_RST#**. Note that **M_RST#** is asserted when **P_RST#**is asserted or is asserted with software.
Rst(T)	The pin is reset with **TRST#**.

Table 2. DDR SDRAM Signals

Name	Count	Type	Description
M_CK[2:0]	3	O	**Memory Clocks** are used to provide the positive differential clocks to the external SDRAM memory subsystem.
M_CK[2:0]#	3	O	**Memory Clocks** are used to provide the negative differential clocks to the external SDRAM memory subsystem.
M_RST#	1	O Async	**Memory Reset** indicates when the memory subsystem has been reset with **P_RST#** or a software reset.
MA[13:0]	14	O Sync(M), Rst(M)	**Memory Address Bus** carries the multiplexed row and column addresses to the SDRAM memory banks.
BA[1:0]	2	O Sync(M), Rst(M)	**SDRAM Bank Address** indicates which of the SDRAM internal banks are read or written during the current transaction.
RAS#	1	O Sync(M), Rst(M)	**SDRAM Row Address Strobe** indicates the presence of a valid row address on the Multiplexed Address Bus **MA[12:0]**.
CAS#	1	O Sync(M), Rst(M)	**SDRAM Column Address Strobe** indicates the presence of a valid column address on the Multiplexed Address Bus **MA[12:0]**.
WE#	1	O Sync(M), Rst(M)	**SDRAM Write Enable** indicates that the current memory transaction is a write operation.
CS[1:0]#	2	O Sync(M), Rst(M)	**SDRAM Chip Select** enables the SDRAM devices for a memory access (Physical banks 0 and 1).
CKE[1:0]	2	O Sync(M), Rst(M)	**SDRAM Clock Enable** enables the clocks for the SDRAM memory. Deasserting will place the SDRAM in self-refresh mode.
DQ[63:0]	64	I/O Sync(M), Rst(M)	**SDRAM Data Bus** carries 64-bit data to and from memory. During a data cycle, read or write data is present on one or more contiguous bytes. During write operations, unused pins are driven to determinate values.
CB[7:0]	8	I/O Sync(M), Rst(M)	**SDRAM ECC Check Bits** carry the 8-bit ECC code to and from memory during data cycles.
DQS[8:0]	9	I/O Sync(M), Rst(M)	**SDRAM Data Strobes** carry the strobe signals, output in write mode and input in read mode for source synchronous data transfer.
DM[8:0]	9	O Sync(M), Rst(M)	**SDRAM Data Mask** controls which bytes on the data bus should be written. When **DM[8:0]** is asserted, the SDRAM devices do not accept valid data from the byte lanes.
Total	120		

Table 3. DDR-II SDRAM Signals

Name	Count	Type	Description
DQS[8:0]#	9	I/O Sync(M) Rst(M)	**SDRAM Data Strobes** carry the differential strobe signals in DDR-II mode, output in write mode and input in read mode for source synchronous data transfer.
ODT[1:0]	2	O Sync(M) Rst(M)	**On Die Termination Control,** turns on SDRAM termination during writes.
DDRRES[2:1]	2	I/O	**Compensation For DDR OCD** (analog) DDR-II mode only.
Total	13		

Table 4. MISC SDRAM Signals

Name	Count	Type	Description
DDRCRES0	1	O	**Analog VSS Ref Pin** (analog) both **DDRSLWCRES** and **DDRIMPCRES** signals connect to this pin through a reference resistor.
DDRSLWCRES	1	I/O	**Compensation Voltage Reference** (analog) for DDR driver slew rate control connected through a resistor to **DDRCRES0**.
DDRIMPCRES	1	I/O	**Compensation Voltage Reference** (analog) for DDR driver impedance control connected through a resistor to **DDRCRES0**.
Total	3		

Table 5. Peripheral Bus Interface Signals

Name	Count	Type	Description
A[22:16]	7	O Rst(M)	**Address Bus 22:16** carries a demultiplexed version of address bits A22:16. During address (T_a), wait state (T_w) and data cycles (T_d) cycles, **A22:16** represents the upper seven address bits for the current access. **A22:16** allows the PBI interface to address up to 8 Mbytes per peripheral device. See "*Table 12, "Reset Strap Signals" on page 27*" for a functional description.
AD[15:0]	16	I/O Rst(M)	**Address/Data Bus** carries 16-bit physical addresses and 8-, or 16-bit data to and from memory. During an address (T_a) cycle, bits 2-31 contain a physical word address (bits 0-1 indicate **SIZE**; see below). During a data (T_d) cycle, bits 0-7, or 0-15 contain read or write data, depending on the corresponding bus width. During write operations to 8-bit wide memory regions, the PBI drives unused bus pins high or low. **SIZE**, which comprises bits 0-1 of the AD lines during a T_a cycle, specifies the number of data transfers during the bus transaction. **AD1 AD0** 0 0 1 Transfer 0 1 2 Transfers 1 0 3 Transfers 1 1 4 Transfers See "*Table 12, "Reset Strap Signals" on page 27*" for a functional description.
A[2:0]	3	O Rst(M)	**Address Bus 2:0** carries a demultiplexed version of bits 2:0 of the **AD[15:0]** bus. During an address (T_a) cycle, bits **A[2:0]** matches **AD[2:0]**. During a bursted read data (T_d) cycle, **A[2:0]** will represent the current byte address in the bursted transaction. **A[2:1]** are used for an 16-bit wide peripheral while **A[1:0]** are used for an 8-bit wide peripheral. See "*Table 12, "Reset Strap Signals" on page 27*" for a functional description.
ALE	1	O Rst(M)	**Address Latch Enable** indicates the transfer of a physical address. The pin is asserted during the first address cycle and deasserted during the second address cycle.
POE#	1	O Rst(M)	**Peripheral Output Enable** Indicates whether the bus access is a write or a read with respect to the I/O processor and is valid during the entire bus access. This pin may be used to control the **OE#** input on peripheral devices. 0 = Read 1 = Write
PWE#	1	O Rst(M)	**Peripheral Write Enable** indicates whether the bus access is a write or a read with respect to the I/O processor and is valid during the entire bus access. This pin is use for flash memory accesses and controls the **WE#** input on the ROM. 0 = Write 1 = Read
PCE[1]#	1	O Rst(M)	**Peripheral Chip Enables** specify which of the two memory address ranges are associated with current bus access. The pin remains valid during the entire bus access.
PCE[0]#	1	O Rst(M)	**Peripheral Chip Enables** specify which of the two memory address ranges are associated with current bus access. The pin remains valid during the entire bus access.
Total	31		

Table 6. Primary PCI Bus Signals (Sheet 1 of 2)

Name	Count	Type	Description
P_AD[31:0]	32	I/O Sync(P) Rst(P)	**Primary PCI Address/Data** is the multiplexed PCI address and lower 32 bits of the data bus.
P_AD[63:32]	32	I/O Sync(P) Rst(P)	**Primary PCI Address/Data** is the upper 32 bits of the PCI data bus driven during the data phase.
P_PAR	1	I/O Sync(P) Rst(P)	**Primary PCI Bus Parity** is even parity across **P_AD[31:0]** and **P_C/BE[3:0]#**.
P_PAR64	1	I/O Sync(P) Rst(P)	**Primary PCI Bus Upper DWORD Parity** is even parity across **P_AD[63:32]** and **P_C/BE[7:4]#**
P_C/BE[7:0]#	8	I/O Sync(P) Rst(P)	**Primary PCI Bus Command and Byte Enables** are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables for **P_AD[63:0]**.
P_REQ#	1	O Sync(P) Rst(P)	**Primary PCI Bus Request** indicates to the PCI bus arbiter that the I/O processor desires use of the PCI bus.
P_REQ64#	1	I/O Sync(P) Rst(P)	**Primary PCI Bus Request 64-Bit Transfer** indicates the attempt of a 64-bit transaction on the PCI bus. When the target is 64-bit capable, the target acknowledges the attempt with the assertion of **P_ACK64#**.
P_IDSEL	1	I Sync(P)	**Primary PCI Bus Initialization Device Select** is used to select the 80331 during a Configuration Read or Write command on the PCI bus.
P_GNT#	1	I Sync(P)	**Primary PCI Bus Grant** indicates that access to the PCI bus has been granted.
P_ACK64#	1	I/O Sync(P) Rst(P)	**Primary PCI Bus Acknowledge 64-Bit Transfer** indicates that the device has positively decoded its address as the target of the current access and the target is willing to transfer data using the full 64-bit data bus.
P_FRAME#	1	I/O Sync(P) Rst(P)	**Primary PCI Bus Cycle Frame** is asserted to indicate the beginning and duration of an access.
P_IRDY#	1	I/O Sync(P) Rst(P)	**Primary PCI Bus Initiator Ready** indicates the initiating agent's ability to complete the current data phase of the transaction. During a write, it indicates that valid data is present on the Address/Data bus. During a read, it indicates the processor is ready to accept the data.
P_TRDY#	1	I/O Sync(P) Rst(P)	**Primary PCI Bus Target Ready** indicates the target agent's ability to complete the current data phase of the transaction. During a read, it indicates that valid data is present on the Address/Data bus. During a write, it indicates the target is ready to accept the data.
P_STOP#	1	I/O Sync(P) Rst(P)	**Primary PCI Bus Stop** indicates a request to stop the current transaction on the PCI bus.
P_DEVSEL#	1	I/O Sync(P) Rst(P)	**Primary PCI Bus Device Select** is driven by a target agent that has successfully decoded the address. As an input, it indicates whether or not an agent has been selected.
P_SERR#	1	I/O OD Sync(P) Rst(P)	**Primary PCI Bus System Error** is driven for address parity errors on the PCI bus.

Table 6. Primary PCI Bus Signals (Sheet 2 of 2)

Name	Count	Type	Description
P_PERR#	1	I/O Sync(P) Rst(P)	**Primary PCI Bus Parity Error** is asserted when a data parity error occurs during a PCI bus transaction.
P_M66EN	1	I/O	**Primary PCI Bus 66 MHz Enable** indicates the speed of the PCI bus. When this signal is sampled high the PCI bus speed is 66 MHz, when low, the bus speed is 33 MHz.
P_CLK	1	I	**Primary PCI Bus Input Clock** provides the timing for all PCI transactions and is the clock source for most internal 80331 units.
P_RST#	1	I Async	**RESET** brings PCI-specific registers, sequencers, and signals to a consistent state. When **P_RST#** is asserted: • PCI output signals are driven to a known consistent state. • PCI bus interface output signals are three-stated. • Open drain signals such as **P_SERR#** are floated. **P_RST#** may be asynchronous to **P_CLK** when asserted or deasserted. Although asynchronous, deassertion must be guaranteed to be a clean, bounce-free edge.
P_RCOMP	1	I/O	**PCI Resistor Compensation Pin** is an analog pad that connects to the board resistor to control all pci output driver strengths (analog).
Total	90		

NOTE: When the PCI bridge is disabled (**BRG_EN** = 0), all primary PCI interface signals become inactive, and the secondary interface becomes a primary PCI interface.

Table 7. Secondary PCI Bus Signals (Sheet 1 of 2)

Name	Count	Type	Description
S_AD[31:0]	32	I/O Sync(S) Rst(S)	**Secondary PCI Address/Data** is the multiplexed PCI address and lower 32 bits of the data bus.
S_AD[63:32]	32	I/O Sync(S) Rst(S)	**Secondary PCI Address/Data** is the upper 32 bits of the PCI data bus.
S_PAR	1	I/O Sync(S) Rst(S)	**Secondary PCI Bus Parity** is even parity across **S_AD[31:0]** and **S_C/BE[3:0]#**.
S_PAR64	1	I/O Sync(S) Rst(S)	**Secondary PCI Bus Upper DWORD Parity** is even parity across **S_AD[63:32]** and **S_C/BE[7:4]#**.
S_C/BE[3:0]#	4	I/O Sync(S) Rst(S)	**Secondary PCI Bus Command and Byte Enables** are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as the byte enables for **S_AD[31:0]**.
S_C/BE[7:4]#	4	I/O Sync(S) Rst(S)	**Secondary PCI Byte Enables** are used as byte enables for **S_AD[63:32]** during secondary PCI data phases.
S_REQ64#	1	I/O Sync(S) Rst(S)	**Secondary PCI Bus Request 64-Bit Transfer** indicates the attempt of a 64-bit transaction on the secondary PCI bus. When the target is 64-bit capable, the target acknowledges the attempt with the assertion of **S_ACK64#**.
S_ACK64#	1	I/O Sync(S) Rst(S)	**Secondary PCI Bus Acknowledge 64-Bit Transfer** indicates the device has positively decoded its address as the target of the current access, indicates the target is willing to transfer data using 64 bits.
S_FRAME#	1	I/O Sync(S) Rst(S)	**Secondary PCI Bus Cycle Frame** is asserted to indicate the beginning and duration of an access.
S_IRDY#	1	I/O Sync(S) Rst(S)	**Secondary PCI Bus Initiator Ready** indicates the initiating agent ability to complete current data phase of transaction. During a write, it indicates valid data is present on the secondary Address/Data bus. During a read, it indicates the processor is ready to accept the data.
S_TRDY#	1	I/O Sync(S) Rst(S)	**Secondary PCI Bus Target Ready** indicates the target agent ability to complete the current data phase of the transaction. During a read, it indicates that valid data is present on the secondary Address/Data bus. During a write, it indicates the target is ready to accept the data.
S_STOP#	1	I/O Sync(S) Rst(S)	**Secondary PCI Bus Stop** indicates a request to stop the current transaction on the secondary PCI bus.
S_DEVSEL#	1	I/O Sync(S) Rst(S)	**Secondary PCI Bus Device Select** is driven by a target agent that has successfully decoded the address. As an input, it indicates whether or not an agent has been selected.
S_SERR#	1	I/O OD Sync(S) Rst(S)	**Secondary PCI Bus System Error** is driven for address parity errors on the secondary PCI bus.
S_RST#	1	O Async	**Secondary PCI Bus Reset** is an output based on **P_RST#**. It brings PCI-specific registers, sequencers, and signals to a consistent state. When **P_RST#** is asserted, it causes **S_RST#** to assert and: • PCI output signals are driven to a known consistent state. • PCI bus interface output signals are three-stated. • Open drain signals such as **S_SERR#** are floated. **S_RST#** may be asynchronous to **S_CLKIN** when asserted or deasserted. Although asynchronous, deassertion must be ensured to be a clean, bounce-free edge.

Table 7. Secondary PCI Bus Signals (Sheet 2 of 2)

Name	Count	Type	Description
S_PERR#	1	I/O Sync(S) Rst(S)	**Secondary PCI Bus Parity Error** is asserted when a data parity error during a secondary PCI bus transaction.
S_CLKO[3:0]	4	O	**Secondary PCI Bus Output Clocks** are used to drive external logic on the secondary PCI bus.
S_CLKOUT	1	O	**Secondary PCI Bus Output Clock** is used to drive **S_CLKIN** when the IO processor provides secondary bus clocks.
S_CLKIN/ P_CLK[1]	1	I	**Secondary PCI Bus Input Clock** provides the timing for all PCI transactions. Typically connected on the board to **S_CLKOUT**. Provides the timing clock for all secondary PCI interfaces. When the PCI Bridge is disabled (**BRG_EN**=0), this is the **Primary PCI Input Clock**, driven by an external device.
S_M66EN	1	I/O	**Secondary PCI Bus 66 MHz Enable** indicates the speed of the secondary PCI bus. When this signal is high, the bus speed is 66 MHz and when it is low, the bus speed is 33 MHz.
S_REQ[3]#/ P_IDSEL[1]	1	I Sync(S)	**Secondary PCI Bus Request** is the request signal from device 3 on the secondary PCI bus. When the PCI Bridge is disabled (**BRG_EN**=0), this pin functions as **PCI Bus Initialization Device Select** and is used to select the 80331 during a Configuration Read or Write command on the PCI bus.
S_REQ[1]# P_GNT#[1]	1	I Sync(S)	**Secondary PCI Bus Request** is the request signal from device 1 on the secondary PCI bus. When the PCI Bridge is disabled (**BRG_EN**=0), this pin functions as **Primary PCI Bus Grant** indicating that access to the PCI bus has been granted.
S_REQ[2,0]#	2	I Sync(S)	**Secondary PCI Bus Requests** are the request signals from devices 2 and 0 on the secondary PCI bus.
S_GNT[3,2]#	2	O Sync(A) Rst(A)	**Secondary PCI Bus Grants** are grant signals sent to devices 3 and 2 on the secondary PCI bus.
S_GNT[1]#/ P_REQ#[1]	1	O Sync(S) Rst(S)	**Secondary PCI Bus Grant** is a grant signal sent to device 1 on the secondary PCI bus. When the PCI Bridge is disabled (**BRG_EN**=0), this pin functions as **Primary PCI Bus Request** and indicates to the PCI bus arbiter that the I/O processor desires use of the PCI bus.
S_GNT[0]#/ P_BMI[1]	1	O/OD Sync(S) Rst(S)	**Secondary PCI Bus Grant** is a grant signal sent to device 0 on the secondary PCI bus. When the PCI Bridge is disabled (**BRG_EN**=0), this pin functions as **PCI Bus Master Indicator** to be used with external RAIDIOS logic for private device control.
S_PCIXCAP	1	I	**Secondary PCI-X Capability** is an analog pad that selects PCI/X mode and frequency capabilities. Non-standard, special purpose analog pin.
S_RCOMP	1	I/O	**PCI Resistor Compensation Pin** is an analog pad that connects to the board resistor to control all PCI output driver strengths (analog).
Total	101		

NOTE: When the PCI Bridge is disabled (**BRG_EN**=0), all secondary PCI interface signals become primary interface signals.

1. These signal functions are only valid when BRG_EN=0 and ARB_EN=0.

Table 8. Interrupt Signals

Name	Count	Type	Description
P_INT[D:A]#	4	O OD Async Rst(P)	**Primary PCI Bus Interrupt** requests an interrupt. The assertion and deassertion of **P_INT[D:A]#** is asynchronous to **P_CLK**. A device asserts its **P_INT[D:A]#** line when requesting attention from its device driver. Once the **P_INT[D:A]#** signal is asserted, it remains asserted until the device driver clears the pending request. **P_INT[D:A]#** interrupts are level sensitive.
S_INT[D:A]#	4	I Async Rst(S)	**Secondary PCI Bus Interrupt** requests an interrupt. The assertion and deassertion of **S_INT[D:A]#** is asynchronous to **S_CLKIN**. A device asserts its **S_INT[D:A]#** line when requesting attention from its device driver. Once the **S_INT[D:A]#** signal is asserted, it remains asserted until the device driver clears the pending request. **S_INT[D:A]#** interrupts are level sensitive.
HPI#	1	I Async	**High Priority Interrupt** causes a high priority interrupt to the I/O processor. This pin is level-detect only and is internally synchronized.
Total	9		

Table 9. I^2C Signals

Name	Count	Type	Description
SCL0	1	I/O	I^2C Clock provides synchronous operation of the I^2C bus zero.
SCD0	1	I/O	I^2C Data is used for data transfer and arbitration of the I^2C bus zero.
SCL1	1	I/O	I^2C Clock provides synchronous operation of the I^2C bus one.
SCD1	1	I/O	I^2C Data is used for data transfer and arbitration of the I^2C bus one.
Total	4		

Table 10. UART Signals (Sheet 1 of 2)

Name	Count	Type	Description
GPIO[0]/ U0_RXD	1	I/O	**General Purpose I/O**: These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. **Serial Input**: Serial data input from device pin to receive shift register.
GPIO[1]/ U0_TXD	1	I/O	**General Purpose I/O**: These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. **Serial Output**: Composite serial data output to the communications link-peripheral, modem, or data set. The TXD signal is set to the MARKING (logic 1) state upon a Reset operation.
GPIO[2]/ U0_CTS#	1	I/O	**General Purpose I/O**: These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. **Clear To Send**: When low, this pin indicates that the receiving UART is ready to receive data. When the receiving UART deasserts **CTS#** high, the transmitting UART should stop transmission to prevent overflow of the receiving UARTs buffer. The **CTS#** signal is a modem-status input whose condition may be tested by the host processor or by the UART when in Autoflow mode as described below: **Non-Autoflow Mode**: When not in Autoflow mode, bit 4 (CTS) of the Modem Status register (MSR) indicates the state of **CTS#**. Bit 4 is the complement of the **CTS#** signal. Bit 0 (DCTS) of the Modem Status register indicates whether the **CTS#** input has changed state since the previous reading of the Modem Status register. **CTS#** has no effect on the transmitter. The user may program the UART to interrupt the processor when DCTS changes state. The programmer may then stall the outgoing data stream by starving the transmit FIFO or disabling the UART with the IER register. **NOTE:** When UART transmission is stalled by disabling the UART, the user may not receive an MSR interrupt when **CTS#** reasserts. This occurs because disabling the UART also disables interrupts. As a workaround, the user may use Auto CTS in Autoflow Mode, or program the **CTS#** pin to interrupt. **Autoflow Mode**: **NOTE:** In Autoflow mode, the UART Transmit circuitry will check the state of **CTS#** before transmitting each byte. When **CTS#** is high, no data is transmitted.
GPIO[3]/ U0_RTS#	1	I/O	**General Purpose I/O**: These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. **Request To Send**: When low, this informs the remote device that the UART is ready to receive data. A reset operation sets this signal to its Inactive (high) state. LOOP mode operation holds this signal in its Inactive state. **Non-Autoflow Mode**: The **RTS#** output signal may be asserted by setting bit 1 (RTS) of the Modem Control register to a 1. The RTS bit is the complement of the **RTS#** signal. **Autoflow Mode**: **RTS#** is automatically asserted by the autoflow circuitry when the Receive buffer exceeds its programmed threshold. It is deasserted when enough bytes are removed from the buffer to lower the data level back to the threshold.

Table 10. UART Signals (Sheet 2 of 2)

Name	Count	Type	Description
GPIO[4]/ U1_RXD	1	I/O	**General Purpose I/O**: These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. **Serial Input**: Serial data input from device pin to receive shift register.
GPIO[5]/ U1_TXD	1	I/O	**General Purpose I/O**: These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. **Serial Output**: Composite serial data output to the communications link-peripheral, modem, or data set. The TXD signal is set to the MARKING (logic 1) state upon a Reset operation.
GPIO[6]/ U1_CTS#	1	I/O	**General Purpose I/O**: These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. **Clear To Send**: When low, this pin indicates that the receiving UART is ready to receive data. When the receiving UART deasserts **CTS#** high, the transmitting UART should stop transmission to prevent overflow of the receiving UARTs buffer. The **CTS#** signal is a modem-status input whose condition may be tested by the host processor or by the UART when in Autoflow mode as described below: **Non-Autoflow Mode**: When not in Autoflow mode, bit 4 (CTS) of the Modem Status register (MSR) indicates the state of **CTS#**. Bit 4 is the complement of the **CTS#** signal. Bit 0 (DCTS) of the Modem Status register indicates whether the **CTS#** input has changed state since the previous reading of the Modem Status register. **CTS#** has no effect on the transmitter. The user may program the UART to interrupt the processor when DCTS changes state. The programmer may then stall the outgoing data stream by starving the transmit FIFO or disabling the UART with the IER register. **NOTE:** When UART transmission is stalled by disabling the UART, the user may not receive an MSR interrupt when **CTS#** reasserts. This occurs because disabling the UART also disables interrupts. As a workaround, the user may use Auto CTS in Autoflow Mode, or program the **CTS#** pin to interrupt. **Autoflow Mode**: **NOTE:** In Autoflow mode, the UART Transmit circuitry will check the state of **CTS#** before transmitting each byte. When **CTS#** is high, no data is transmitted.
GPIO[7]/ U1_RTS#	1	I/O	**General Purpose I/O**: These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. **Request To Send**: When low, this informs the remote device that the UART is ready to receive data. A reset operation sets this signal to its Inactive (high) state. LOOP mode operation holds this signal in its Inactive state. **Non-Autoflow Mode**: The **RTS#** output signal may be asserted by setting bit 1 (RTS) of the Modem Control register to a 1. The RTS bit is the complement of the **RTS#** signal. **Autoflow Mode**: **RTS#** is automatically asserted by the autoflow circuitry when the Receive buffer exceeds its programmed threshold. It is deasserted when enough bytes are removed from the buffer to lower the data level back to the threshold.
Total	8		

Table 11. Test and Miscellaneous Signals

Name	Count	Type	Description
TCK	1	I	**Test Clock** provides clock input for IEEE 1149.1 Boundary Scan Testing (JTAG). State information and data are clocked into the device on the rising clock edge and data is clocked out on the falling clock edge.
TDI	1	I Sync(T)	**Test Data Input** is the JTAG serial input pin. **TDI** is sampled on the rising edge of **TCK**, during the SHIFT-IR and SHIFT-DR states of the Test Access Port. This signal has a weak internal pull-up to ensure proper operation when this pin is not being driven.
TDO	1	O Sync(T) Rst(T)	**Test Data Output** is the serial output pin for the JTAG feature. **TDO** is driven on the falling edge of **TCK** during the SHIFT-IR and SHIFT-DR states of the Test Access Port. At other times, **TDO** floats. The behavior of **TDO** is independent of **P_RST#**.
TRST#	1	I Async	**Test Reset** asynchronously resets the Test Access Port controller function of IEEE 1149 Boundary Scan Testing (JTAG). This pin has a weak internal pull-up.
TMS	1	I Sync(T)	**Test Mode Select** is sampled on the rising edge of **TCK** to select the operation of the test logic for IEEE 1149 Boundary Scan testing. This pin has a weak internal pull-up.
N/C	64	-	**No Connect**. Do not connect to any signal, power or ground.
PU1	1	I	**Pullup 1** must be pulled high. **NOTE:** This signal was formerly known as **P_LOCK#**.
PU2	1	I	**Pullup 2** must be pulled high. Is controlled by **PCIODT_EN**. **NOTE:** This signal was formerly known as **S_LOCK#**.
PWRDELAY	1	I Async	**Power Fail Delay** is used to delay the reset of the memory controller in a power-fail condition. This allows the self-refresh command to be sent to the DDR SDRAM array.
Total	72		

Table 12. Reset Strap Signals (Sheet 1 of 2)

Name	Count	Type	Description
RETRY	1	C	**Configuration Retry Mode**: **RETRY** is latched on the rising (deasserting) edge of **P_RST#** and determines when the PCI interface of the ATU will disable PCI configuration cycles by signaling a retry until the configuration cycle retry bit is cleared in the PCI configuration and status register. 0 = Configuration Cycles enabled (Requires pull down resistor.) 1 = Configuration Retry enabled in the ATU (Default mode) **NOTE:** Muxed onto signal **AD[6]**, see Table 15, “Pin Multiplexing for Functional Modes” on page 33.
CORE_RST#	1	C	**Core Reset Mode** is latched on the rising (deasserting) edge of **P_RST#** and determines when the Intel XScale® core is held in reset until the processor reset bit is cleared in PCI configuration and status register. 0 = Hold in reset. (Requires pull-down resistor.) 1 = Do not hold in reset. (Default mode) **NOTE:** Muxed onto signal **AD[5]**, see Table 15, “Pin Multiplexing for Functional Modes” on page 33.
P_BOOT16#	1	C	**Bus Width** is latched on the rising (deasserting) edge of **P_RST#**, it sets the default bus width for the PBI Memory Boot window. 0 = 16 bits wide (Requires a pull-down resistor.) 1 = 8 bits wide (Default mode) **NOTE:** Muxed onto signal **AD[4]**, see Table 15, “Pin Multiplexing for Functional Modes” on page 33.
MEM_TYPE	1	C	**Memory Type**: **MEM_TYPE** is latched on the rising (deasserting) edge of **P_RST#** and it defines the speed of the DDR SDRAM interface. 0 = DDR-II SDRAM at 400 MHz (Required pull-down resistor.) 1 = DDR SDRAM at 333 MHz (Default mode) **NOTE:** Muxed onto signal **AD[2]**, see Table 15, “Pin Multiplexing for Functional Modes” on page 33.
S_PCIX133EN	1	Config	**Secondary PCI Bus 133 MHz Enable**: **S_PCIX133EN** latched on rising (deasserting) edge of **P_RST#** and determines maximum PCI-X mode operating frequency. 0 = 100 MHz enabled (Requires pull down resistor.) 1 = 133 MHz enabled (Default mode) **NOTE:** Muxed onto signal **AD[3]**, see Table 15, “Pin Multiplexing for Functional Modes” on page 33.
PRIVMEM	1	Config	**Private Memory Enable: PRIVMEM** latched at rising (deasserting) edge of **P_RST#** and determines if 80331 operates with Private Memory Space on the secondary PCI bus of the PCI-to-PCI Bridge. 0 = Normal addressing mode (Requires pull-down resistor) 1 = Private Addressing enable in PCI-to-PCI Bridge. (Default mode). **NOTE:** Muxed onto signal **A[1]**, see Table 15, “Pin Multiplexing for Functional Modes” on page 33.
PRIVDEV	1	Config	**Private Device Enable: PRIVDEV** latched at rising (deasserting) edge of **P_RST#** and determines if 80331 operates with Private Device enabled on the secondary PCI bus of the PCI-to-PCI Bridge. 0 = All Secondary PCI devices are accessible to Primary PCI config cycles. (Requires pull-down resistor) 1 = Private Devices enabled in PCI-to-PCI Bridge. (Default mode) **NOTE:** Muxed onto signal **A[0]**, see Table 15, “Pin Multiplexing for Functional Modes” on page 33.

Table 12. Reset Strap Signals (Sheet 2 of 2)

Name	Count	Type	Description
BRG_EN	1	Config	**Bridge Enable**: **BRG_EN** latched at rising (deasserting) edge of **P_RST#** and determines if 80331 operates with PCI-to-PCI Bridge. 0 = Disable Bridge, enable **P_CLK** input on **S_CLKIN** input. (Requires pull-down resistor) 1 = Enabled Bridge. (Default mode) **NOTE:** Muxed onto signal **AD[0]**, see Table 15, "Pin Multiplexing for Functional Modes" on page 33.
ARB_EN	1	Config	**Internal Arbiter Enable: ARB_EN** is latched on the rising (deasserting) edge of **P_RST#** and it determines if the PCI interface will enable the integrated arbiter, or use an external arbiter. **NOTE**: **ARB_EN** only valid when PCI bridge disabled (**BRG_EN**=0). 0 = Internal Arbiter disabled (Requires pull-down resistor). 1 = Internal Arbiter enabled (Default mode). **NOTE:** Muxed onto signal **AD[1]**, see Table 15, "Pin Multiplexing for Functional Modes" on page 33.
P_32BITPCI#	1	Config	**Primary PCI-X Bus Width**: P_32BITPCI# is latched on the rising (deasserting) edge of P_RST#, and by default, identifies 80331 subsystem as 64-bit unless the appropriate pull-down resistor is used. This strap sets bit 16 in the PCI-X Bridge status register. 0 = 32 bit wide bus. (Requires pull-down resistor). 1 = 64 bit wide bus. (Default mode). **NOTE:** Muxed onto signal **A[2]**, see Table 15, "Pin Multiplexing for Functional Modes" on page 33.
PCIODT_EN	1	C	**PCI Bus ODT Enable**: PCIODT_EN is latched on the rising (deasserting) edge of P_RST#, and determines when the PCI-X interface will have On Die Termination enabled. PCI ODT enable is valid for the secondary PCI bus only. The following signals are affected by PCIODT_EN: S_AD[63:32], S_C/BE[7:4]#, S_PAR64, S_REQ64#, S_REQ[3:0]#, S_ACK64#, S_FRAME#, S_IRDY#, S_DEVSEL#, S_TRDY#, S_STOP#, S_PERR#, S_LOCK#, S_M66EN, S_SERR#, S_INT[D:A]# 0 = ODT disabled on the secondary PCI bus. (Requires pull-down resistor). 1 = ODT enabled on the secondary PCI bus. (Default mode). **NOTE:** Muxed onto signal **A[20]**, see Table 15, "Pin Multiplexing for Functional Modes" on page 33.
Total	11		

Table 13. Power and Ground Pins

Name	Count	Type	Description
$V_{CCPLL[1-5]}$	4	PWR	**PLL 1-5 Power** is a separate V_{CC15} supply ball for the phase lock loop clock generator. It is to be connected to the board V_{CC15} plane. Each V_{CCPLL} requires a lowpass filter circuit to reduce noise-induced clock jitter and its effects on timing relationships. See the *Intel® 80331 I/O Processor Design Guide* for more information. **Note:** There is no VCCPLL3 signal.
V_{CC33}	49	PWR	**3.3 V Power** balls to be connected to a 3.3 V power board plane.
$V_{CC25/18}$	29	PWR	**2.5 V/1.8 V Power** balls to be connected to a 2.5 V or 1.8 V power board plane, dependent on DDR or DDRII mode.
V_{CC15}	58	PWR	**1.5 V Power** balls to be connected to a 1.5 V power board plane.
V_{CC13}	7	PWR	**1.3 V Power** balls to be connected to a 1.35 V power board plane.
DDR_VREF	1	I	**SDRAM Voltage Reference** is used to supply the reference voltage to the differential inputs of the memory controller pins.
V_{SS}	226	GND	**Ground** balls to be connected to a ground board plane.
$V_{SSA[1-5]}$	4	GND	**Analog Ground** balls need to be connected to the appropriate V_{CCPLL} filter, and not to board ground. **Note:** There is no VSSA3 signal.

Table 14. Pin Mode Behavior (Sheet 1 of 3)

Pin	Reset Lind	Reset Lind nobrg	Norm Lind	Norm Lind nobrg	ECC off DDR	32Bit DDR	32Bit P_PCI	32Bit S_PCI
M_CK[2:0]	X (1)	X (1)	VO	VO	VO	VO	-	-
M_CK[2:0]#	X (1)	X (1)	VO	VO	VO	VO	-	-
M_RST#	0	0	VO	VO	VO	VO	-	-
MA[13:0]	0*	0*	VO	VO	VO	VO	-	-
BA[1:0]	0*	0*	VO	VO	VO	VO	-	-
RAS#	1*	1*	VO	VO	VO	VO	-	-
CAS#	1*	1*	VO	VO	VO	VO	-	-
WE#	1*	1*	VO	VO	VO	VO	-	-
CS[1:0]#	1*	1*	VO	VO	VO	VO	-	-
CKE[1:0]	0*	0*	VO	VO	VO	VO	-	-
DQ[63:32]	Z*	Z*	VB	VB	VB	ID,Z	-	-
DQ[31:0]	Z*	Z*	VB	VB	VB	VB	-	-
CB[7:0]	Z*	Z*	VB	VB	VB	VB	-	-
DQS[8]	Z*	Z*	VB	VB	ID,Z	VB	-	-
DQS[7:4]	Z*	Z*	VB	VB	VB	ID,Z	-	-
DQS[3:0]	Z*	Z*	VB	VB	VB	VB	-	-
DQS[8]#	Z*	Z*	VB	VB	ID,Z	VB	-	-
DQS[7:4]#	Z*	Z*	VB	VB	VB	ID,Z	-	-
DQS[3:0]#	Z*	Z*	VB	VB	VB	VB	-	-
DM[8]	Z*	Z*	VO	VO	Z	VO	-	-
DM[7:4]	Z*	Z*	VO	VO	VO	Z	-	-
DM[3:0]	Z*	Z*	VO	VO	VO	VO	-	-
DDR_VREF	VI	VI	VI	VI	VI	VI	-	-
ODT[1:0] (2)	0	0	VO	VO	VO	VO	-	-
DDRRES[2:1]	Z*	Z*	VB	VB	VB	VB	-	-
DDRCRES0	0	0	0	0	0	0	-	-
DDRSLWCRES	VB	VB	VB	VB	VB	VB	-	-
DDRIMPCRES	VB	VB	VB	VB	VB	VB	-	-
A[22:16]	H	H	VO	VO	-	-	-	-
AD[15:0]	H	H	VB	VB	-	-	-	-
A[2:0]	H	H	VO	VO	-	-	-	-
ALE	0	0	VO	VO	-	-	-	-
POE#	1	1	VO	VO	-	-	-	-
PWE#	1	1	VO	VO	-	-	-	-
PCE[1]#	H	H	VO	VO	-	-	-	-
PCE[0]#	H	H	VO	VO	-	-	-	-
P_AD[63:32]	Z	Z	VB	H	-	-	H	-
P_AD[31:0]	0	Z	VB	H	-	-	VB	-
P_PAR	Z	Z	VB	H	-	-	VB	-

Table 14. Pin Mode Behavior (Sheet 2 of 3)

Pin	Reset Lind	Reset Lind nobrg	Norm Lind	Norm Lind nobrg	ECC off DDR	32Bit DDR	32Bit P_PCI	32Bit S_PCI
P_PAR64	Z	Z	VB	H	-	-	H	-
P_C/BE[7:4]#	Z	Z	VB	H	-	-	H	-
P_C/BE[3:0]#	Z	Z	VB	H	-	-	VB	-
P_REQ#	1	Z	VO	Z	-	-	-	-
P_REQ64#	VI	H	VB	H	-	-	-	-
P_IDSEL	VI	H	VI	H	-	-	-	-
P_GNT#	VI	H	VI	H	-	-	-	-
P_ACK64#	Z	H	VB	H	-	-	-	-
P_FRAME#	Z	H	VB	H	-	-	-	-
P_IRDY#	Z	H	VB	H	-	-	-	-
P_TRDY#	VI	H	VB	H	-	-	-	-
P_STOP#	VI	H	VB	H	-	-	-	-
P_DEVSEL#	VI	H	VB	H	-	-	-	-
P_LOCK#	Z	H	VB	H	-	-	-	-
P_SERR#	Z	H	VB	H	-	-	-	-
P_CLK	VI	H	VI	H	-	-	-	-
P_RST#	VI	VI	VI	VI	-	-	-	-
P_PERR#	Z	H	VB	H	-	-	-	-
P_M66EN	VB	H	VB	H	-	-	-	-
S_AD[63:32]	Z	Z	VB	VB	-	-	-	H
S_AD[31:0]	0	Z	VB	VB	-	-	-	-
S_PAR	0	Z	VB	VB	-	-	-	-
S_PAR64	Z	Z	VB	VB	-	-	-	H
S_C/BE[3:0]#	0	Z	VB	VB	-	-	-	-
S_C/BE[7:4]#	Z	Z	VB	VB	-	-	-	H
S_REQ64#	VO	VI	VB	VB	-	-	-	-
S_ACK64#	Z	Z	VB	VB	-	-	-	-
S_FRAME#	Z	Z	VB	VB	-	-	-	-
S_IRDY#	Z	Z	VB	VB	-	-	-	-
S_TRDY#	VO	VI	VB	VB	-	-	-	-
S_STOP#	VO	VI	VB	VB	-	-	-	-
S_DEVSEL#	VO	VI	VB	VB	-	-	-	-
S_SERR#	Z	Z	VB	VB	-	-	-	-
S_RST#	VO	Z	VO	Z	-	-	-	-
S_PERR#	Z	Z	VB	VB	-	-	-	-
S_LOCK#	Z	Z	VB	VB	-	-	-	-
S_CLKO[3:0]	VO	Z	VO	Z	-	-	-	-
S_CLKOUT	VO	Z	VO	Z	-	-	-	-

Table 14. Pin Mode Behavior (Sheet 3 of 3)

Pin	Reset Lind	Reset Lind nobrg	Norm Lind	Norm Lind nobrg	ECC off DDR	32Bit DDR	32Bit P_PCI	32Bit S_PCI
S_CLKIN	VI	VI	VI	VI	-	-	-	-
S_M66EN	VB	VB	VB	VB	-	-	-	-
S_REQ[3]#/ P_IDSEL	VI	VI	VI	VI	-	-	-	-
S_REQ[1]#/ P_GNT#	VI	VI	VI	H	-	-	-	-
S_REQ[2,0]#	VI	H	VI	H	-	-	-	-
S_GNT[3,2]#,	H	H	VO	H	-	-	-	-
S_GNT[1]#/ P_REQ#	H	H	VO	VO	-	-	-	-
S_GNT[0]#/ P_BMI	H	H	VO	VO	-	-	-	-
S_PCIXCAP	VI	VSS	VI	VSS	-	-	-	-
P_RCOMP	AO	AO	AO	AO	-	-	-	-
S_RCOMP	AO	AO	AO	AO	-	-	-	-
P_INT[D:A]#	Z	Z (3)	Z/0	Z (3)	-	-	-	-
S_INT[D:A]#	VI	ID	VI	ID	-	-	-	-
HPI#	VI	VI	VI	VI	-	-	-	-
SCL0, SCD0, SCL1, SCD1	H	H	VB	VB	-	-	-	-
GPIO[3:0]/ U0_RTS#, U0_CTS#, U0_TXD, U0_RXD,	VI	VI	VB	VB	-	-	-	-
GPIO[7:4]/ U1_RTS#, U1_CTS#, U1_TXD, U1_RXD	VI	VI	VB	VB	-	-	-	-
TCK	VI	VI	VI	VI	-	-	-	-
TDI	H	H	H	H	-	-	-	-
TDO(4)	VO*	VO*	VO	VO	-	-	-	-
TRST#	H	H	H	H	-	-	-	-
TMS	H	H	H	H	-	-	-	-
PWRDELAY	VI	VI	VI	VI	-	-	-	-
NC[3:0]	H	H	H	H	-	-	-	-

NOTES:

1 = driven to V_{CC}
0 = driven to V_{SS}
X = driven to unknown state
ID = The input is disabled.
H = pulled up to V_{CC}
PD = pull-up disabled
L = pulled down to V_{SS}

Z = output disabled (Floats)
VB = acts like a Valid Bidirectional pin.
VO = a Valid Output level is driven.
VI = Need to drive a Valid Input level.
* = After power fail sequence completes.
** = Caused by Hi-Z from mode pins only.
AO = analog output level.

1. Clocks become valid right before M_RST# deasserts.
2. ODT signal to be low during power up and initialization per DDRII JEDEC specification.
3. P_INT[A]# is the only active ouput in 80331 no bridge mode.
4. Test inputs pulled up as noted in signal description table Table 11, “Test and Miscellaneous Signals” on page 26 and test outputs tristated during normal functional operation.

Table 15. Pin Multiplexing for Functional Modes

Pin	Bridge Disabled	Reset Straps
A[20]	-	PCIODT_EN
AD[6]	-	RETRY
AD[5]	-	CORE_RST#
AD[4]	-	P_BOOT16#
AD[3]	-	S_PCIX133EN
AD[2]	-	MEM_TYPE
AD[1]	-	ARB_EN
AD[0]	-	BRG_EN
A[2]	-	P_32BITPCI#
A[1]	-	PRIVMEM
A[0]	-	PRIVDEV
S_REQ[3]#	P_IDSEL	-
S_REQ[1]#	P_GNT#	-
S_GNT[1]#	P_REQ#	-
S_GNT[0]#	P_BMI	-
S_CLKIN	P_CLK	-

Figure 2. 829-Ball FCBGA Package Diagram

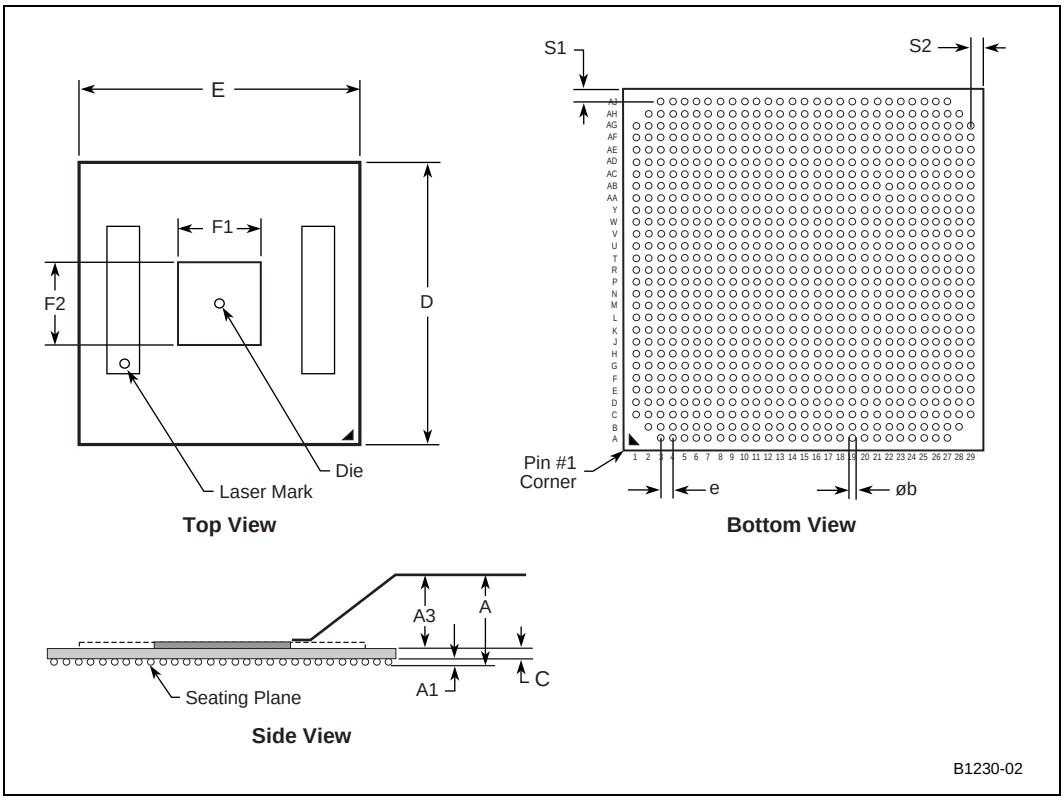


Table 16. FC-style, H-PBGA Package Dimensions

829-Pin BGA		
Symbol	**Minimum**	**Maximum**
A	2.392	2.942
A1	0.50	0.70
A3	0.742	0.872
b	0.61 Ref.	
C	1.15	1.37
D	37.45	37.55
E	37.45	37.55
F1	9.88 Ref.	
F2	10.16 Ref.	
e	1.27 Ref.	
S1	0.97 Ref.	
S2	0.97 Ref.	

NOTE: Measurement in millimeters.

Figure 3. Intel® 80331 I/O Processor Ballout (Bottom View)

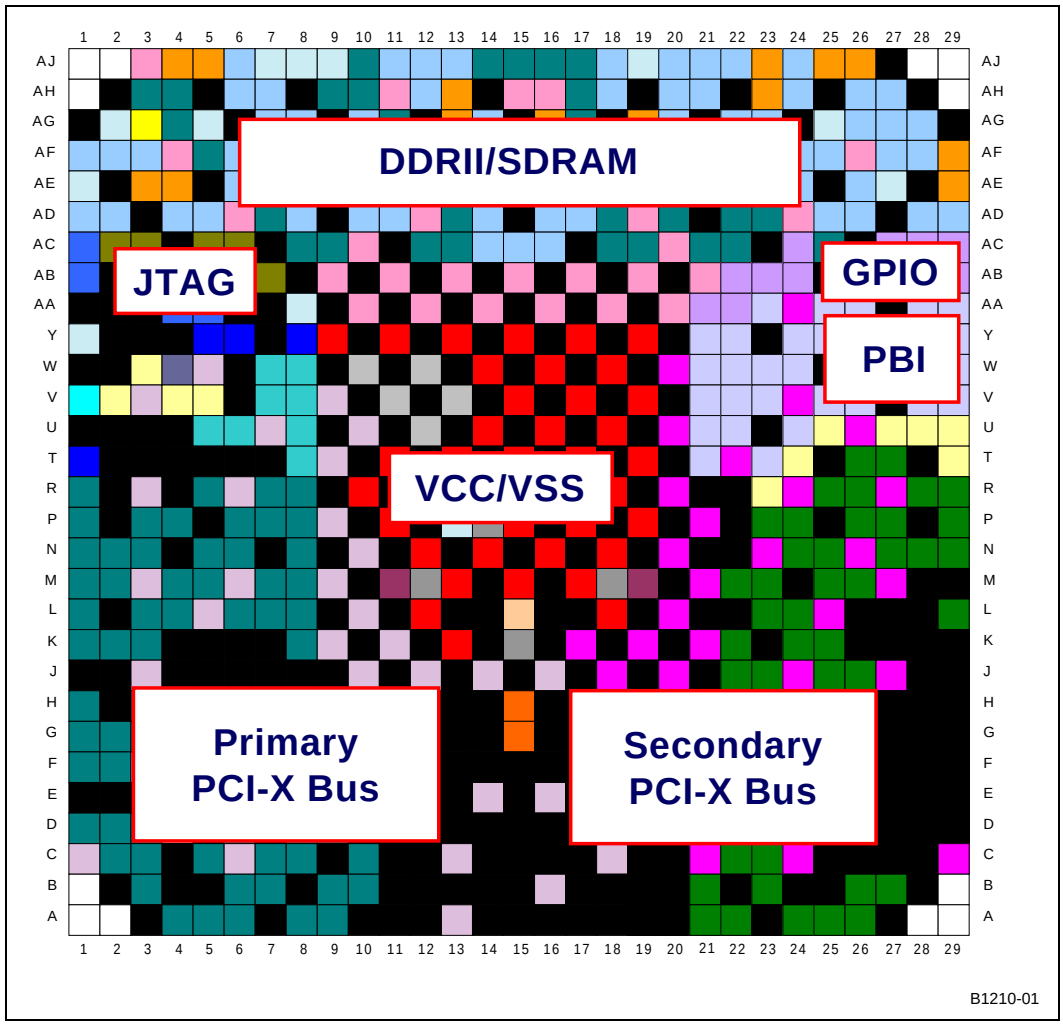


Figure 4. Intel® 80331 I/O Processor Ballout - Left Side (Bottom View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
AJ	NB	NB	VCC 25/18	DQS1#	DQS1	DQ15	DQ10	DQ17	DM2	MA8	DQ28	DQ25	DM3	M_CK1	M_ CK1#
AH	NB	VSS	M_RST#	CKE1	VSS	DQ14	DQ20	VSS	MA6	MA5	VCC 25/18	DQ24	DQS3#	VSS	DM8
AG	VSS	DQ3	VSS	CKE0	DM1	VSS	DQ11	DQ16	VSS	DQ18	MA4	VSS	DQS3	DQ31	VSS
AF	DQ6	DQ7	DQ2	VCC 25/18	MA12	DQ9	VSS	DQ21	DQS2	VCC 25/18	MA3	DQ29	VCC 25/18	DQ30	CB1
AE	DM0	VSS	DQS0#	DQS0	VSS	DQ13	DQ8	VSS	DQS2#	DQ23	VSS	MA1	DQ26	VSS	CB0
AD	DQ5	DQ4	VSS	DQ1	DQ0	VCC 25/18	MA7	DQ12	VSS	DQ22	DQ19	VCC 25/18	BA1	DQ27	VSS
AC	DDR_ VREF	VSS	VSS	VSS	VSS	VSS	VSS	MA11	MA9	VCC 25/18	VSS	MA2	MA0	CB5	CB4
AB	N/C	VSS	TDO	TMS	VSS	VSS	VCC 25/18	VSS	VCC 25/18	VSS	VCC 25/18	VSS	VCC 25/18	VSS	VCC 25/18
AA	N/C	N/C	VSS	N/C	TRST#	VSS	P_ RST#	HPI#	VSS	VCC 25/18	VSS	VCC 25/18	VSS	VCC 25/18	VSS
Y	VCC15	TCK	VSS	VSS	N/C	TDI	VSS	N/C	VCC13	VSS	VCC13	VSS	VCC13	VSS	VCC15
W	PWR DELAY	VSS	P_ INTA#	VSS	VCC33	N/C	N/C	N/C	VSS	VCC13	VSS	VCC13	VSS	VCC15	VSS
V	P_ RCOMP	P_ INTD#	VCC33	P_ INTC#	P_ INTB#	VSS	N/C	N/C	VCC15	VSS	VCC15	VSS	VCC13	VSS	VCC15
U	P_ C/BE4#	P_ C/BE5#	P_ C/BE7#	VSS	N/C	N/C	VCC33	N/C	VSS	VCC15	VSS	VCC13	VSS	VCC15	VSS
T	N/C	VSS	P_ C/BE6#	N/C	VSS	N/C	VSS	N/C	VCC15	VSS	VCC15	VSS	VCC15	VSS	VCC15
R	P_ AD63	P_ PAR64	VCC33	N/C	P_ AD45	VCC33	P_ AD46	P_ AD47	VSS	VCC15	VSS	VCC15	VSS	VCC15	VCC PLL4
P	P_ AD60	VSS	P_ AD61	P_ AD62	VSS	P_ AD44	P_ AD43	P_ AD42	VCC15	VSS	VCC15	VSS	VCC PLL5	VSSA5	VCC15
N	P_ AD59	P_ AD58	P_ AD57	VSS	P_ AD41	P_ AD40	VSS	P_ AD39	VSS	VCC15	VSS	VCC15	VSS	VCC15	VSS
M	P_ AD56	P_ AD55	VCC33	P_ AD54	P_ AD38	VCC33	P_ AD37	P_ AD36	VCC15	VSS	VCC PLL2	VSSA2	VCC15	VSS	VCC15
L	P_ AD53	VSS	P_ AD52	P_ AD51	VCC33	P_ AD35	P_ AD34	P_ AD33	VSS	VCC15	VSS	VCC15	VSS	VSS	VSS
K	P_ AD50	N/C	P_ IDSEL	VSS	N/C	N/C	VSS	P_ AD32	VCC15	VCC15	VCC15	VSS	VCC15	VSS	VSS
J	P_ AD49	P_ AD48	VCC33	P_ PERR#	P_ SERR#	VSS	PU1	N/C	VSS	VCC15	VSS	VCC15	VSS	VCC15	VSS
H	P_ AD0	VSS	P_ AD1	P_ AD2	VCC33	P_ ACK64#	N/C	N/C	N/C	P_ TRDY#	P_ REQ#	N/C	N/C	VSS	VCC15
G	P_ AD3	P_ AD4	P_ AD5	VSS	P_ DEVSEL#	P_ STOP#	VSS	VSS	P_ CLK	VCC33	P_ REQ64#	P_GNT#	VSS	N/C	VSS
F	P_ AD6	P_ AD7	VCC33	P_ AD8	P_ IRDY#	VCC33	N/C	VSS	VSS	VSS	N/C	VSS	N/C	N/C	VSS
E	P_ C/BE0#	VSS	P_ M66EN	P_ AD9	VSS	P_ FRAME#	N/C	VSS	VCC33	VSS	VSS	N/C	N/C	VCC15	N/C
D	P_ AD10	P_ AD11	P_ AD12	VCC33	P_ C/BE2#	P_ AD19	VSS	P_ AD24	P_ AD27	VSS	N/C	N/C	VSS	N/C	N/C
C	VCC33	P_ AD13	P_ AD14	P_ PAR	P_ AD17	VCC33	P_ AD22	P_ AD25	VCC33	P_ AD30	N/C	N/C	VCC15	N/C	VSS
B	NB	VSS	P_ AD15	P_ C/BE1#	VSS	P_ AD20	P_ AD23	VSS	P_ AD28	P_ AD31	VSS	N/C	VSS	VSS	VSS
A	NB	NB	VSS	P_ AD16	P_ AD18	P_ AD21	P_ C/BE3#	P_ AD26	P_ AD29	VSS	N/C	N/C	VCC15	VSS	VCC15
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

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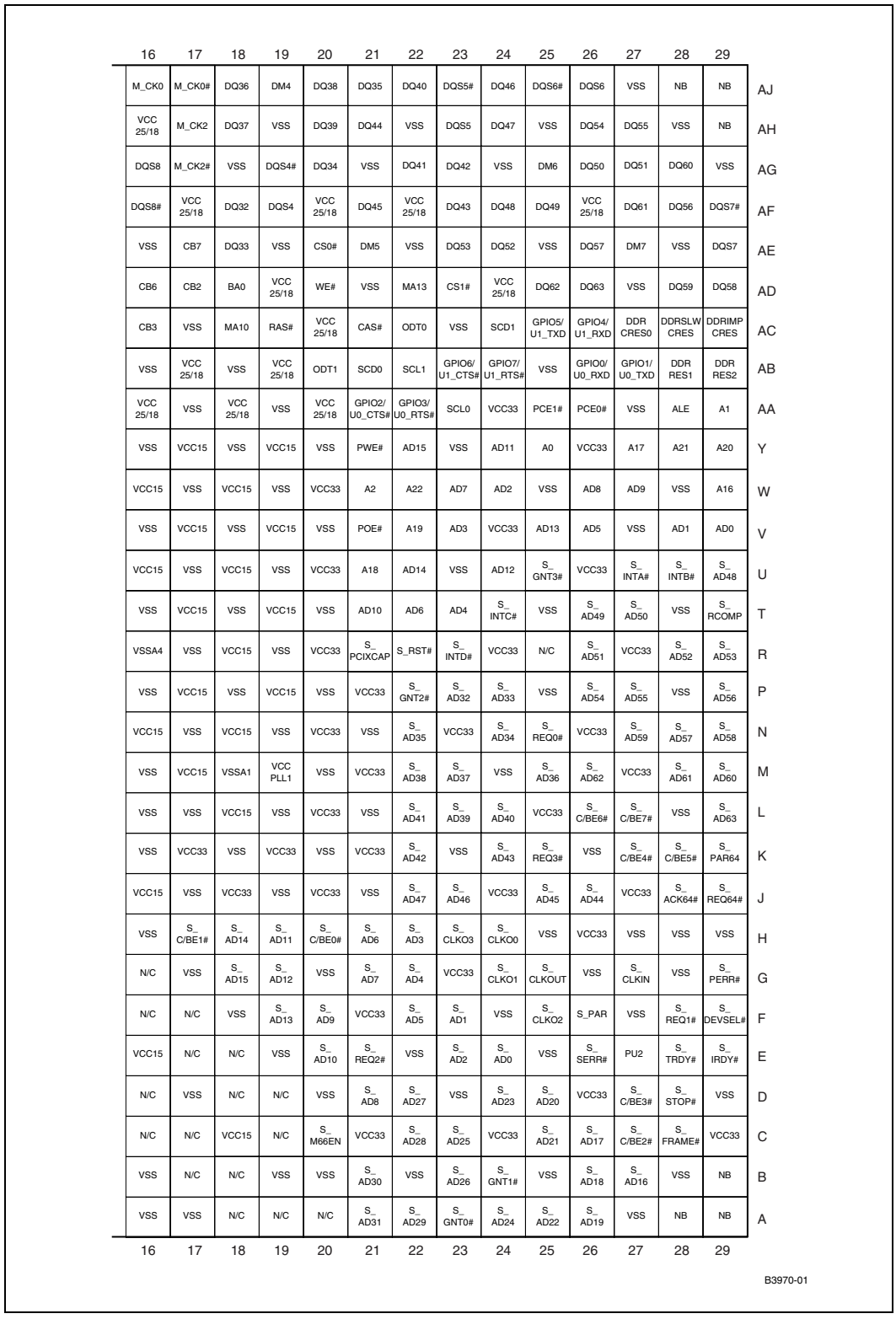
Figure 5. Intel® 80331 I/O Processor Ballout - Right Side (Bottom View)



16	17	18	19	20	21	22	23	24	25	26	27	28	29	
M_CK0	M_CK0#	DQ36	DM4	DQ38	DQ35	DQ40	DQS5#	DQ46	DQS6#	DQS6	VSS	NB	NB	AJ
VCC 25/18	M_CK2	DQ37	VSS	DQ39	DQ44	VSS	DQS5	DQ47	VSS	DQ54	DQ55	VSS	NB	AH
DQS8	M_CK2#	VSS	DQS4#	DQ34	VSS	DQ41	DQ42	VSS	DM6	DQ50	DQ51	DQ60	VSS	AG
DQS8#	VCC 25/18	DQ32	DQS4	VCC 25/18	DQ45	VCC 25/18	DQ43	DQ48	DQ49	VCC 25/18	DQ61	DQ56	DQS7#	AF
VSS	CB7	DQ33	VSS	CS0#	DM5	VSS	DQ53	DQ52	VSS	DQ57	DM7	VSS	DQS7	AE
CB6	CB2	BA0	VCC 25/18	WE#	VSS	MA13	CS1#	VCC 25/18	DQ62	DQ63	VSS	DQ59	DQ58	AD
CB3	VSS	MA10	RAS#	VCC 25/18	CAS#	ODT0	VSS	SCD1	GPIO5/ U1_TXD	GPIO4/ U1_RXD	DDR CRES0	DDRSLW CRES	DDRIMP CRES	AC
VSS	VCC 25/18	VSS	VCC 25/18	ODT1	SCD0	SCL1	GPIO6/ U1_CTS#	GPIO7/ U1_RTS#	VSS	GPIO0/ U0_RXD	GPIO1/ U0_TXD	DDR RES1	DDR RES2	AB
VCC 25/18	VSS	VCC 25/18	VSS	VCC 25/18	GPIO2/ U0_CTS#	GPIO3/ U0_RTS#	SCL0	VCC33	PCE1#	PCE0#	VSS	ALE	A1	AA
VSS	VCC15	VSS	VCC15	VSS	PWE#	AD15	VSS	AD11	A0	VCC33	A17	A21	A20	Y
VCC15	VSS	VCC15	VSS	VCC33	A2	A22	AD7	AD2	VSS	AD8	AD9	VSS	A16	W
VSS	VCC15	VSS	VCC15	VSS	POE#	A19	AD3	VCC33	AD13	AD5	VSS	AD1	AD0	V
VCC15	VSS	VCC15	VSS	VCC33	A18	AD14	VSS	AD12	S_ GNT3#	VCC33	S_ INTA#	S_ INTB#	S_ AD48	U
VSS	VCC15	VSS	VCC15	VSS	AD10	AD6	AD4	S_ INTC#	VSS	S_ AD49	S_ AD50	VSS	S_ RCOMP	T
VSSA4	VSS	VCC15	VSS	VCC33	S_ PCIXCAP	S_RST#	S_ INTD#	VCC33	N/C	S_ AD51	VCC33	S_ AD52	S_ AD53	R
VSS	VCC15	VSS	VCC15	VSS	VCC33	S_ GNT2#	S_ AD32	S_ AD33	VSS	S_ AD54	S_ AD55	VSS	S_ AD56	P
VCC15	VSS	VCC15	VSS	VCC33	VSS	S_ AD35	VCC33	S_ AD34	S_ REQ0#	VCC33	S_ AD59	S_ AD57	S_ AD58	N
VSS	VCC15	VSSA1	VCC PLL1	VSS	VCC33	S_ AD38	S_ AD37	VSS	S_ AD36	S_ AD62	VCC33	S_ AD61	S_ AD60	M
VSS	VSS	VCC15	VSS	VCC33	VSS	S_ AD41	S_ AD39	S_ AD40	VCC33	S_ C/BE6#	S_ C/BE7#	VSS	S_ AD63	L
VSS	VCC33	VSS	VCC33	VSS	VCC33	S_ AD42	VSS	S_ AD43	S_ REQ3#	VSS	S_ C/BE4#	S_ C/BE5#	S_ PAR64	K
VCC15	VSS	VCC33	VSS	VCC33	VSS	S_ AD47	S_ AD46	VCC33	S_ AD45	S_ AD44	VCC33	S_ ACK64#	S_ REQ64#	J
VSS	S_ C/BE1#	S_ AD14	S_ AD11	S_ C/BE0#	S_ AD6	S_ AD3	S_ CLKO3	S_ CLKO0	VSS	VCC33	VSS	VSS	VSS	H
N/C	VSS	S_ AD15	S_ AD12	VSS	S_ AD7	S_ AD4	VCC33	S_ CLKO1	S_ CLKOUT	VSS	S_ CLKIN	VSS	S_ PERR#	G
N/C	N/C	VSS	S_ AD13	S_ AD9	VCC33	S_ AD5	S_ AD1	VSS	S_ CLKO2	S_PAR	VSS	S_ REQ1#	S_ DEVSEL#	F
VCC15	N/C	N/C	VSS	S_ AD10	S_ REQ2#	VSS	S_ AD2	S_ AD0	VSS	S_ SERR#	PU2	S_ TRDY#	S_ IRDY#	E
N/C	VSS	N/C	N/C	VSS	S_ AD8	S_ AD27	VSS	S_ AD23	S_ AD20	VCC33	S_ C/BE3#	S_ STOP#	VSS	D
N/C	N/C	VCC15	N/C	S_ M66EN	VCC33	S_ AD28	S_ AD25	VCC33	S_ AD21	S_ AD17	S_ C/BE2#	S_ FRAME#	VCC33	C
VSS	N/C	N/C	VSS	VSS	S_ AD30	VSS	S_ AD26	S_ GNT1#	VSS	S_ AD18	S_ AD16	VSS	NB	B
VSS	VSS	N/C	N/C	N/C	S_ AD31	S_ AD29	S_ GNT0#	S_ AD24	S_ AD22	S_ AD19	VSS	NB	NB	A
16	17	18	19	20	21	22	23	24	25	26	27	28	29	

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Table 17. 829-Lead Package - Alphabetical Ball Listings (Sheet 1 of 7)

Ball	Signal	Ball	Signal	Ball	Signal
A1	--	B13	VSS	C25	S_AD21
A2	--	B14	VSS	C26	S_AD17
A3	VSS	B15	VSS	C27	S_C/BE2#
A4	P_AD16	B16	VSS	C28	S_FRAME#
A5	P_AD18	B17	N/C	C29	VCC33
A6	P_AD21	B18	N/C	D1	P_AD10
A7	P_C/BE3#	B19	VSS	D2	P_AD11
A8	P_AD26	B20	VSS	D3	P_AD12
A9	P_AD29	B21	S_AD30	D4	VCC33
A10	VSS	B22	VSS	D5	P_C/BE2#
A11	N/C	B23	S_AD26	D6	P_AD19
A12	N/C	B24	S_GNT1#	D7	VSS
A13	VCC15	B25	VSS	D8	P_AD24
A14	VSS	B26	S_AD18	D9	P_AD27
A15	VCC15	B27	S_AD16	D10	VSS
A16	VSS	B28	VSS	D11	N/C
A17	VSS	B29	--	D12	N/C
A18	N/C	C1	VCC33	D13	VSS
A19	N/C	C2	P_AD13	D14	N/C
A20	N/C	C3	P_AD14	D15	N/C
A21	S_AD31	C4	P_PAR	D16	N/C
A22	S_AD29	C5	P_AD17	D17	VSS
A23	S_GNT0#	C6	VCC33	D18	N/C
A24	S_AD24	C7	P_AD22	D19	N/C
A25	S_AD22	C8	P_AD25	D20	VSS
A26	S_AD19	C9	VCC33	D21	S_AD8
A27	VSS	C10	P_AD30	D22	S_AD27
A28	--	C11	N/C	D23	VSS
A29	--	C12	N/C	D24	S_AD23
B1	--	C13	VCC15	D25	S_AD20
B2	VSS	C14	N/C	D26	VCC33
B3	P_AD15	C15	VSS	D27	S_C/BE3#
B4	P_C/BE1#	C16	N/C	D28	S_STOP#
B5	VSS	C17	N/C	D29	VSS
B6	P_AD20	C18	VCC15	E1	P_C/BE0#
B7	P_AD23	C19	N/C	E2	VSS
B8	VSS	C20	S_M66EN	E3	P_M66EN
B9	P_AD28	C21	VCC33	E4	P_AD9
B10	P_AD31	C22	S_AD28	E5	VSS
B11	VSS	C23	S_AD25	E6	P_FRAME#
B12	N/C	C24	VCC33	E7	N/C

Table 17. 829-Lead Package - Alphabetical Ball Listings (Sheet 2 of 7)

Ball	Signal	Ball	Signal	Ball	Signal
E8	VSS	F20	S_AD9	H3	P_AD1
E9	VCC33	F21	VCC33	H4	P_AD2
E10	VSS	F22	S_AD5	H5	VCC33
E11	VSS	F23	S_AD1	H6	P_ACK64#
E12	N/C	F24	VSS	H7	N/C
E13	N/C	F25	S_CLKO2	H8	N/C
E14	VCC15	F26	S_PAR	H9	N/C
E15	N/C	F27	VSS	H10	P_TRDY#
E16	VCC15	F28	S_REQ1#	H11	P_REQ#
E17	N/C	F29	S_DEVSEL#	H12	N/C
E18	N/C	G1	P_AD3	H13	N/C
E19	VSS	G2	P_AD4	H14	VSS
E20	S_AD10	G3	P_AD5	H15	VCC15
E21	S_REQ2#	G4	VSS	H16	VSS
E22	VSS	G5	P_DEVSEL#	H17	S_C/BE1#
E23	S_AD2	G6	P_STOP#	H18	S_AD14
E24	S_AD0	G7	VSS	H19	S_AD11
E25	VSS	G8	VSS	H20	S_C/BE0#
E26	S_SERR#	G9	P_CLK	H21	S_AD6
E27	PU2	G10	VCC33	H22	S_AD3
E28	S_TRDY#	G11	P_REQ64#	H23	S_CLKO3
E29	S_IRDY#	G12	P_GNT#	H24	S_CLKO0
F1	P_AD6	G13	VSS	H25	VSS
F2	P_AD7	G14	N/C	H26	VCC33
F3	VCC33	G15	VSS	H27	VSS
F4	P_AD8	G16	N/C	H28	VSS
F5	P_IRDY#	G17	VSS	H29	VSS
F6	VCC33	G18	S_AD15	J1	P_AD49
F7	N/C	G19	S_AD12	J2	P_AD48
F8	VSS	G20	VSS	J3	VCC33
F9	VSS	G21	S_AD7	J4	P_PERR#
F10	VSS	G22	S_AD4	J5	P_SERR#
F11	N/C	G23	VCC33	J6	VSS
F12	VSS	G24	S_CLKO1	J7	PU1
F13	N/C	G25	S_CLKOUT	J8	N/C
F14	N/C	G26	VSS	J9	VSS
F15	VSS	G27	S_CLKIN	J10	VCC15
F16	N/C	G28	VSS	J11	VSS
F17	N/C	G29	S_PERR#	J12	VCC15
F18	VSS	H1	P_AD0	J13	VSS
F19	S_AD13	H2	VSS	J14	VCC15

Table 17. 829-Lead Package - Alphabetical Ball Listings (Sheet 3 of 7)

Ball	Signal	Ball	Signal	Ball	Signal
J15	VSS	K27	S_C/BE4#	M10	VSS
J16	VCC15	K28	S_C/BE5#	M11	VCCPLL2
J17	VSS	K29	S_PAR64	M12	VSSA2
J18	VCC33	L1	P_AD53	M13	VCC15
J19	VSS	L2	VSS	M14	VSS
J20	VCC33	L3	P_AD52	M15	VCC15
J21	VSS	L4	P_AD51	M16	VSS
J22	S_AD47	L5	VCC33	M17	VCC15
J23	S_AD46	L6	P_AD35	M18	VSSA1
J24	VCC33	L7	P_AD34	M19	VCCPLL1
J25	S_AD45	L8	P_AD33	M20	VSS
J26	S_AD44	L9	VSS	M21	VCC33
J27	VCC33	L10	VCC15	M22	S_AD38
J28	S_ACK64#	L11	VSS	M23	S_AD37
J29	S_REQ64#	L12	VCC15	M24	VSS
K1	P_AD50	L13	VSS	M25	S_AD36
K2	N/C	L14	VSS	M26	S_AD62
K3	P_IDSEL	L15	VSS	M27	VCC33
K4	VSS	L16	VSS	M28	S_AD61
K5	N/C	L17	VSS	M29	S_AD60
K6	N/C	L18	VCC15	N1	P_AD59
K7	VSS	L19	VSS	N2	P_AD58
K8	P_AD32	L20	VCC33	N3	P_AD57
K9	VCC15	L21	VSS	N4	VSS
K10	VCC15	L22	S_AD41	N5	P_AD41
K11	VCC15	L23	S_AD39	N6	P_AD40
K12	VSS	L24	S_AD40	N7	VSS
K13	VCC15	L25	VCC33	N8	P_AD39
K14	VSS	L26	S_C/BE6#	N9	VSS
K15	VSS	L27	S_C/BE7#	N10	VCC15
K16	VSS	L28	VSS	N11	VSS
K17	VCC33	L29	S_AD63	N12	VCC15
K18	VSS	M1	P_AD56	N13	VSS
K19	VCC33	M2	P_AD55	N14	VCC15
K20	VSS	M3	VCC33	N15	VSS
K21	VCC33	M4	P_AD54	N16	VCC15
K22	S_AD42	M5	P_AD38	N17	VSS
K23	VSS	M6	VCC33	N18	VCC15
K24	S_AD43	M7	P_AD37	N19	VSS
K25	S_REQ3#	M8	P_AD36	N20	VCC33
K26	VSS	M9	VCC15	N21	VSS

Table 17. 829-Lead Package - Alphabetical Ball Listings (Sheet 4 of 7)

Ball	Signal	Ball	Signal	Ball	Signal
N22	S_AD35	R5	P_AD45	T17	VCC15
N23	VCC33	R6	VCC33	T18	VSS
N24	S_AD34	R7	P_AD46	T19	VCC15
N25	S_REQ0#	R8	P_AD47	T20	VSS
N26	VCC33	R9	VSS	T21	AD10
N27	S_AD59	R10	VCC15	T22	AD6
N28	S_AD57	R11	VSS	T23	AD4
N29	S_AD58	R12	VCC15	T24	S_INTC#
P1	P_AD60	R13	VSS	T25	VSS
P2	VSS	R14	VCC15	T26	S_AD49
P3	P_AD61	R15	VCCPLL4	T27	S_AD50
P4	P_AD62	R16	VSSA4	T28	VSS
P5	VSS	R17	VSS	T29	S_RCOMP
P6	P_AD44	R18	VCC15	U1	P_C/BE4#
P7	P_AD43	R19	VSS	U2	P_C/BE5#
P8	P_AD42	R20	VCC33	U3	P_C/BE7#
P9	VCC15	R21	S_PCIXCAP	U4	VSS
P10	VSS	R22	S_RST#	U5	N/C
P11	VCC15	R23	S_INTD#	U6	N/C
P12	VSS	R24	VCC33	U7	VCC33
P13	VCCPLL5	R25	N/C	U8	N/C
P14	VSSA5	R26	S_AD51	U9	VSS
P15	VCC15	R27	VCC33	U10	VCC15
P16	VSS	R28	S_AD52	U11	VSS
P17	VCC15	R29	S_AD53	U12	VCC13
P18	VSS	T1	N/C	U13	VSS
P19	VCC15	T2	VSS	U14	VCC15
P20	VSS	T3	P_C/BE6#	U15	VSS
P21	VCC33	T4	N/C	U16	VCC15
P22	S_GNT2#	T5	VSS	U17	VSS
P23	S_AD32	T6	N/C	U18	VCC15
P24	S_AD33	T7	VSS	U19	VSS
P25	VSS	T8	N/C	U20	VCC33
P26	S_AD54	T9	VCC15	U21	A18
P27	S_AD55	T10	VSS	U22	AD14
P28	VSS	T11	VCC15	U23	VSS
P29	S_AD56	T12	VSS	U24	AD12
R1	P_AD63	T13	VCC15	U25	S_GNT3#
R2	P_PAR64	T14	VSS	U26	VCC33
R3	VCC33	T15	VCC15	U27	S_INTA#
R4	N/C	T16	VSS	U28	S_INTB#

Table 17. 829-Lead Package - Alphabetical Ball Listings (Sheet 5 of 7)

Ball	Signal	Ball	Signal	Ball	Signal
U29	S_AD48	W12	VCC13	Y24	AD11
V1	P_RCOMP	W13	VSS	Y25	A0
V2	P_INTD#	W14	VCC15	Y26	VCC33
V3	VCC33	W15	VSS	Y27	A17
V4	P_INTC#	W16	VCC15	Y28	A21
V5	P_INTB#	W17	VSS	Y29	A20
V6	VSS	W18	VCC15	AA1	N/C
V7	N/C	W19	VSS	AA2	N/C
V8	N/C	W20	VCC33	AA3	VSS
V9	VCC15	W21	A2	AA4	N/C
V10	VSS	W22	A22	AA5	TRST#
V11	VCC15	W23	AD7	AA6	VSS
V12	VSS	W24	AD2	AA7	P_RST#
V13	VCC13	W25	VSS	AA8	HPI#
V14	VSS	W26	AD8	AA9	VSS
V15	VCC15	W27	AD9	AA10	VCC25/18
V16	VSS	W28	VSS	AA11	VSS
V17	VCC15	W29	A16	AA12	VCC25/18
V18	VSS	Y1	VCC15	AA13	VSS
V19	VCC15	Y2	TCK	AA14	VCC25/18
V20	VSS	Y3	VSS	AA15	VSS
V21	POE#	Y4	VSS	AA16	VCC25/18
V22	A19	Y5	N/C	AA17	VSS
V23	AD3	Y6	TDI	AA18	VCC25/18
V24	VCC33	Y7	VSS	AA19	VSS
V25	AD13	Y8	N/C	AA20	VCC25/18
V26	AD5	Y9	VCC13	AA21	GPIO2/U0_CTS#
V27	VSS	Y10	VSS	AA22	GPIO3/U0_RTS#
V28	AD1	Y11	VCC13	AA23	SCL0
V29	AD0	Y12	VSS	AA24	VCC33
W1	PWRDELAY	Y13	VCC13	AA25	PCE1#
W2	VSS	Y14	VSS	AA26	PCE0#
W3	P_INTA#	Y15	VCC15	AA27	VSS
W4	VSS	Y16	VSS	AA28	ALE
W5	VCC33	Y17	VCC15	AA29	A1
W6	N/C	Y18	VSS	AB1	N/C
W7	N/C	Y19	VCC15	AB2	VSS
W8	N/C	Y20	VSS	AB3	TDO
W9	VSS	Y21	PWE#	AB4	TMS
W10	VCC13	Y22	AD15	AB5	VSS
W11	VSS	Y23	VSS	AB6	VSS

Table 17. 829-Lead Package - Alphabetical Ball Listings (Sheet 6 of 7)

Ball	Signal	Ball	Signal	Ball	Signal
AB7	VCC25/18	AC19	RAS#	AE2	VSS
AB8	VSS	AC20	VCC25/18	AE3	DQS0#
AB9	VCC25/18	AC21	CAS#	AE4	DQS0
AB10	VSS	AC22	ODT0	AE5	VSS
AB11	VCC25/18	AC23	VSS	AE6	DQ13
AB12	VSS	AC24	SCD1	AE7	DQ8
AB13	VCC25/18	AC25	GPIO5/U1_TXD	AE8	VSS
AB14	VSS	AC26	GPIO4/U1_RXD	AE9	DQS2#
AB15	VCC25/18	AC27	DDRCRES0	AE10	DQ23
AB16	VSS	AC28	DDRSLWCRES	AE11	VSS
AB17	VCC25/18	AC29	DDRIMPCRES	AE12	MA1
AB18	VSS	AD1	DQ5	AE13	DQ26
AB19	VCC25/18	AD2	DQ4	AE14	VSS
AB20	ODT1	AD3	VSS	AE15	CB0
AB21	SCD0	AD4	DQ1	AE16	VSS
AB22	SCL1	AD5	DQ0	AE17	CB7
AB23	GPIO6/U1_CTS#	AD6	VCC25/18	AE18	DQ33
AB24	GPIO7/U1_RTS#	AD7	MA7	AE19	VSS
AB25	VSS	AD8	DQ12	AE20	CS0#
AB26	GPIO0/U0_RXD	AD9	VSS	AE21	DM5
AB27	GPIO1/U0_TXD	AD10	DQ22	AE22	VSS
AB28	DDRRES1	AD11	DQ19	AE23	DQ53
AB29	DDRRES2	AD12	VCC25/18	AE24	DQ52
AC1	DDR_VREF	AD13	BA1	AE25	VSS
AC2	VSS	AD14	DQ27	AE26	DQ57
AC3	VSS	AD15	VSS	AE27	DM7
AC4	VSS	AD16	CB6	AE28	VSS
AC5	VSS	AD17	CB2	AE29	DQS7
AC6	VSS	AD18	BA0	AF1	DQ6
AC7	VSS	AD19	VCC25/18	AF2	DQ7
AC8	MA11	AD20	WE#	AF3	DQ2
AC9	MA9	AD21	VSS	AF4	VCC25/18
AC10	VCC25/18	AD22	MA13	AF5	MA12
AC11	VSS	AD23	CS1#	AF6	DQ9
AC12	MA2	AD24	VCC25/18	AF7	VSS
AC13	MA0	AD25	DQ62	AF8	DQ21
AC14	CB5	AD26	DQ63	AF9	DQS2
AC15	CB4	AD27	VSS	AF10	VCC25/18
AC16	CB3	AD28	DQ59	AF11	MA3
AC17	VSS	AD29	DQ58	AF12	DQ29
AC18	MA10	AE1	DM0	AF13	VCC25/18

Table 17. 829-Lead Package - Alphabetical Ball Listings (Sheet 7 of 7)

Ball	Signal	Ball	Signal	Ball	Signal
AF14	DQ30	AG26	DQ50	AJ9	DM2
AF15	CB1	AG27	DQ51	AJ10	MA8
AF16	DQS8#	AG28	DQ60	AJ11	DQ28
AF17	VCC25/18	AG29	VSS	AJ12	DQ25
AF18	DQ32	AH1	--	AJ13	DM3
AF19	DQS4	AH2	VSS	AJ14	M_CK1
AF20	VCC25/18	AH3	M_RST#	AJ15	M_CK1#
AF21	DQ45	AH4	CKE1	AJ16	M_CK0
AF22	VCC25/18	AH5	VSS	AJ17	M_CK0#
AF23	DQ43	AH6	DQ14	AJ18	DQ36
AF24	DQ48	AH7	DQ20	AJ19	DM4
AF25	DQ49	AH8	VSS	AJ20	DQ38
AF26	VCC25/18	AH9	MA6	AJ21	DQ35
AF27	DQ61	AH10	MA5	AJ22	DQ40
AF28	DQ56	AH11	VCC25/18	AJ23	DQS5#
AF29	DQS7#	AH12	DQ24	AJ24	DQ46
AG1	VSS	AH13	DQS3#	AJ25	DQS6#
AG2	DQ3	AH14	VSS	AJ26	DQS6
AG3	VSS	AH15	DM8	AJ27	VSS
AG4	CKE0	AH16	VCC25/18	AJ28	--
AG5	DM1	AH17	M_CK2	AJ29	--
AG6	VSS	AH18	DQ37		
AG7	DQ11	AH19	VSS		
AG8	DQ16	AH20	DQ39		
AG9	VSS	AH21	DQ44		
AG10	DQ18	AH22	VSS		
AG11	MA4	AH23	DQS5		
AG12	VSS	AH24	DQ47		
AG13	DQS3	AH25	VSS		
AG14	DQ31	AH26	DQ54		
AG15	VSS	AH27	DQ55		
AG16	DQS8	AH28	VSS		
AG17	M_CK2#	AH29	--		
AG18	VSS	AJ1	--		
AG19	DQS4#	AJ2	--		
AG20	DQ34	AJ3	VCC25/18		
AG21	VSS	AJ4	DQS1#		
AG22	DQ41	AJ5	DQS1		
AG23	DQ42	AJ6	DQ15		
AG24	VSS	AJ7	DQ10		
AG25	DM6	AJ8	DQ17		

Table 18. 829-Lead Package - Alphabetical Signal Listings (Sheet 1 of 7)

Signal	Ball	Signal	Ball	Signal	Ball
--	A1	CAS#	AC21	DQ20	AH7
--	A2	CB0	AE15	DQ21	AF8
--	A28	CB1	AF15	DQ22	AD10
--	A29	CB2	AD17	DQ23	AE10
--	AH1	CB3	AC16	DQ24	AH12
--	AH29	CB4	AC15	DQ25	AJ12
--	AJ1	CB5	AC14	DQ26	AE13
--	AJ2	CB6	AD16	DQ27	AD14
--	AJ28	CB7	AE17	DQ28	AJ11
--	AJ29	CKE0	AG4	DQ29	AF12
--	B1	CKE1	AH4	DQ3	AG2
--	B29	CS0#	AE20	DQ30	AF14
A0	Y25	CS1#	AD23	DQ31	AG14
A1	AA29	DDR_VREF	AC1	DQ32	AF18
A16	W29	DDRCRES0	AC27	DQ33	AE18
A17	Y27	DDRIMPCRES	AC29	DQ34	AG20
A18	U21	DDRRES1	AB28	DQ35	AJ21
A19	V22	DDRRES2	AB29	DQ36	AJ18
A2	W21	DDRSLWCRES	AC28	DQ37	AH18
A20	Y29	DM0	AE1	DQ38	AJ20
A21	Y28	DM1	AG5	DQ39	AH20
A22	W22	DM2	AJ9	DQ4	AD2
AD0	V29	DM3	AJ13	DQ40	AJ22
AD1	V28	DM4	AJ19	DQ41	AG22
AD10	T21	DM5	AE21	DQ42	AG23
AD11	Y24	DM6	AG25	DQ43	AF23
AD12	U24	DM7	AE27	DQ44	AH21
AD13	V25	DM8	AH15	DQ45	AF21
AD14	U22	DQ0	AD5	DQ46	AJ24
AD15	Y22	DQ1	AD4	DQ47	AH24
AD2	W24	DQ10	AJ7	DQ48	AF24
AD3	V23	DQ11	AG7	DQ49	AF25
AD4	T23	DQ12	AD8	DQ5	AD1
AD5	V26	DQ13	AE6	DQ50	AG26
AD6	T22	DQ14	AH6	DQ51	AG27
AD7	W23	DQ15	AJ6	DQ52	AE24
AD8	W26	DQ16	AG8	DQ53	AE23
AD9	W27	DQ17	AJ8	DQ54	AH26
ALE	AA28	DQ18	AG10	DQ55	AH27
BA0	AD18	DQ19	AD11	DQ56	AF28
BA1	AD13	DQ2	AF3	DQ57	AE26

Table 18. 829-Lead Package - Alphabetical Signal Listings (Sheet 2 of 7)

Signal	Ball	Signal	Ball	Signal	Ball
DQ58	AD29	M_CK2	AH17	N/C	D19
DQ59	AD28	M_CK2#	AG17	N/C	E12
DQ6	AF1	M_RST#	AH3	N/C	E13
DQ60	AG28	MA0	AC13	N/C	E15
DQ61	AF27	MA1	AE12	N/C	E17
DQ62	AD25	MA10	AC18	N/C	E18
DQ63	AD26	MA11	AC8	N/C	E7
DQ7	AF2	MA12	AF5	N/C	F11
DQ8	AE7	MA13	AD22	N/C	F13
DQ9	AF6	MA2	AC12	N/C	F14
DQS0	AE4	MA3	AF11	N/C	F16
DQS0#	AE3	MA4	AG11	N/C	F17
DQS1	AJ5	MA5	AH10	N/C	F7
DQS1#	AJ4	MA6	AH9	P_GNT#	G12
DQS2	AF9	MA7	AD7	N/C	G14
DQS2#	AE9	MA8	AJ10	N/C	G16
DQS3	AG13	MA9	AC9	P_REQ#	H11
DQS3#	AH13	N/C	A11	N/C	H12
DQS4	AF19	N/C	A12	N/C	H13
DQS4#	AG19	N/C	A18	N/C	H7
DQS5	AH23	N/C	A19	N/C	H8
DQS5#	AJ23	N/C	A20	N/C	H9
DQS6	AJ26	N/C	AA1	N/C	J8
DQS6#	AJ25	N/C	AA2	N/C	K2
DQS7	AE29	N/C	AA4	N/C	K5
DQS7#	AF29	N/C	AB1	N/C	K6
DQS8	AG16	N/C	B12	N/C	R25
DQS8#	AF16	N/C	B17	N/C	T1
GPIO0/U0_RXD	AB26	N/C	B18	N/C	T4
GPIO1/U0_TXD	AB27	N/C	C11	N/C	T8
GPIO2/U0_CTS#	AA21	N/C	C12	N/C	U5
GPIO3/U0_RTS#	AA22	N/C	C14	N/C	U6
GPIO4/U1_RXD	AC26	N/C	C16	N/C	U8
GPIO5/U1_TXD	AC25	N/C	C17	N/C	V7
GPIO6/U1_CTS#	AB23	N/C	C19	N/C	V8
GPIO7/U1_RTS#	AB24	N/C	D11	N/C	W6
HPI#	AA8	N/C	D12	N/C	W7
M_CK0	AJ16	N/C	D14	N/C	W8
M_CK0#	AJ17	N/C	D15	N/C	Y5
M_CK1	AJ14	N/C	D16	N/C	Y8
M_CK1#	AJ15	N/C	D18	ODT0	AC22

Table 18. 829-Lead Package - Alphabetical Signal Listings (Sheet 3 of 7)

Signal	Ball	Signal	Ball	Signal	Ball
ODT1	AB20	P_AD45	R5	P_INTD#	V2
P_ACK64#	H6	P_AD46	R7	P_IRDY#	F5
P_AD0	H1	P_AD47	R8	PU1	J7
P_AD1	H3	P_AD48	J2	P_M66EN	E3
P_AD10	D1	P_AD49	J1	P_PAR	C4
P_AD11	D2	P_AD5	G3	P_PAR64	R2
P_AD12	D3	P_AD50	K1	P_PERR#	J4
P_AD13	C2	P_AD51	L4	P_RCOMP	V1
P_AD14	C3	P_AD52	L3	N/C	T6
P_AD15	B3	P_AD53	L1	P_REQ64#	G11
P_AD16	A4	P_AD54	M4	P_RST#	AA7
P_AD17	C5	P_AD55	M2	P_SERR#	J5
P_AD18	A5	P_AD56	M1	P_STOP#	G6
P_AD19	D6	P_AD57	N3	P_TRDY#	H10
P_AD2	H4	P_AD58	N2	PCE0#	AA26
P_AD20	B6	P_AD59	N1	PCE1#	AA25
P_AD21	A6	P_AD6	F1	POE#	V21
P_AD22	C7	P_AD60	P1	PWE#	Y21
P_AD23	B7	P_AD61	P3	PWRDELAY	W1
P_AD24	D8	P_AD62	P4	RAS#	AC19
P_AD25	C8	P_AD63	R1	S_ACK64#	J28
P_AD26	A8	P_AD7	F2	S_AD0	E24
P_AD27	D9	P_AD8	F4	S_AD1	F23
P_AD28	B9	P_AD9	E4	S_AD10	E20
P_AD29	A9	P_C/BE0#	E1	S_AD11	H19
P_AD3	G1	P_C/BE1#	B4	S_AD12	G19
P_AD30	C10	P_C/BE2#	D5	S_AD13	F19
P_AD31	B10	P_C/BE3#	A7	S_AD14	H18
P_AD32	K8	P_C/BE4#	U1	S_AD15	G18
P_AD33	L8	P_C/BE5#	U2	S_AD16	B27
P_AD34	L7	P_C/BE6#	T3	S_AD17	C26
P_AD35	L6	P_C/BE7#	U3	S_AD18	B26
P_AD36	M8	P_CLK	G9	S_AD19	A26
P_AD37	M7	P_DEVSEL#	G5	S_AD2	E23
P_AD38	M5	P_FRAME#	E6	S_AD20	D25
P_AD39	N8	N/C	R4	S_AD21	C25
P_AD4	G2	P_IDSEL	K3	S_AD22	A25
P_AD40	N6	P_INTA#	W3	S_AD23	D24
P_AD41	N5	P_INTB#	V5	S_AD24	A24
P_AD42	P8	P_INTC#	V4	S_AD25	C23
P_AD43	P7	P_AD45	R5	S_AD26	B23

Table 18. 829-Lead Package - Alphabetical Signal Listings (Sheet 4 of 7)

Signal	Ball	Signal	Ball	Signal	Ball
S_AD27	D22	S_AD7	G21	S_SERR#	E26
S_AD28	C22	S_AD8	D21	S_STOP#	D28
S_AD29	A22	S_AD9	F20	S_TRDY#	E28
S_AD3	H22	S_C/BE0#	H20	SCD0	AB21
S_AD30	B21	S_C/BE1#	H17	SCD1	AC24
S_AD31	A21	S_C/BE2#	C27	SCL0	AA23
S_AD32	P23	S_C/BE3#	D27	SCL1	AB22
S_AD33	P24	S_C/BE4#	K27	TCK	Y2
S_AD34	N24	S_C/BE5#	K28	TDI	Y6
S_AD35	N22	S_C/BE6#	L26	TDO	AB3
S_AD36	M25	S_C/BE7#	L27	TMS	AB4
S_AD37	M23	S_CLKIN	G27	TRST#	AA5
S_AD38	M22	S_CLKO0	H24	VCC13	U12
S_AD39	L23	S_CLKO1	G24	VCC13	V13
S_AD4	G22	S_CLKO2	F25	VCC13	W10
S_AD40	L24	S_CLKO3	H23	VCC13	W12
S_AD41	L22	S_CLKOUT	G25	VCC13	Y11
S_AD42	K22	S_DEVSEL#	F29	VCC13	Y13
S_AD43	K24	S_FRAME#	C28	VCC13	Y9
S_AD44	J26	S_GNT0#	A23	VCC15	A13
S_AD45	J25	S_GNT1#	B24	VCC15	A15
S_AD46	J23	S_GNT2#	P22	VCC15	C13
S_AD47	J22	S_GNT3#	U25	VCC15	C18
S_AD48	U29	S_INTA#	U27	VCC15	E14
S_AD49	T26	S_INTB#	U28	VCC15	E16
S_AD5	F22	S_INTC#	T24	VCC15	H15
S_AD50	T27	S_INTD#	R23	VCC15	J10
S_AD51	R26	S_IRDY#	E29	VCC15	J12
S_AD52	R28	PU2	E27	VCC15	J14
S_AD53	R29	S_M66EN	C20	VCC15	J16
S_AD54	P26	S_PAR	F26	VCC15	K10
S_AD55	P27	S_PAR64	K29	VCC15	K11
S_AD56	P29	S_PCIXCAP	R21	VCC15	K13
S_AD57	N28	S_PERR#	G29	VCC15	K9
S_AD58	N29	S_RCOMP	T29	VCC15	L10
S_AD59	N27	S_REQ0#	N25	VCC15	L12
S_AD6	H21	S_REQ1#	F28	VCC15	L18
S_AD60	M29	S_REQ2#	E21	VCC15	M13
S_AD61	M28	S_REQ3#	K25	VCC15	M15
S_AD62	M26	S_REQ64#	J29	VCC15	M17
S_AD63	L29	S_RST#	R22	VCC15	M9

Table 18. 829-Lead Package - Alphabetical Signal Listings (Sheet 5 of 7)

Signal	Ball	Signal	Ball	Signal	Ball
VCC15	N10	VCC25/18	AA20	VCC33	J18
VCC15	N12	VCC25/18	AB11	VCC33	J20
VCC15	N14	VCC25/18	AB13	VCC33	J24
VCC15	N16	VCC25/18	AB15	VCC33	J27
VCC15	N18	VCC25/18	AB17	VCC33	J3
VCC15	P11	VCC25/18	AB19	VCC33	K17
VCC15	P15	VCC25/18	AB7	VCC33	K19
VCC15	P17	VCC25/18	AB9	VCC33	K21
VCC15	P19	VCC25/18	AC10	VCC33	L20
VCC15	P9	VCC25/18	AC20	VCC33	L25
VCC15	R10	VCC25/18	AD12	VCC33	L5
VCC15	R12	VCC25/18	AD19	VCC33	M21
VCC15	R14	VCC25/18	AD24	VCC33	M27
VCC15	R18	VCC25/18	AD6	VCC33	M3
VCC15	T11	VCC25/18	AF10	VCC33	M6
VCC15	T13	VCC25/18	AF13	VCC33	N20
VCC15	T15	VCC25/18	AF17	VCC33	N23
VCC15	T17	VCC25/18	AF20	VCC33	N26
VCC15	T19	VCC25/18	AF22	VCC33	P21
VCC15	T9	VCC25/18	AF26	VCC33	R20
VCC15	U10	VCC25/18	AF4	VCC33	R24
VCC15	U14	VCC25/18	AH11	VCC33	R27
VCC15	U16	VCC25/18	AH16	VCC33	R3
VCC15	U18	VCC25/18	AJ3	VCC33	R6
VCC15	V11	VCC33	AA24	VCC33	U20
VCC15	V15	VCC33	C1	VCC33	U26
VCC15	V17	VCC33	C21	VCC33	U7
VCC15	V19	VCC33	C24	VCC33	V24
VCC15	V9	VCC33	C29	VCC33	V3
VCC15	W14	VCC33	C6	VCC33	W20
VCC15	W16	VCC33	C9	VCC33	W5
VCC15	W18	VCC33	D26	VCC33	Y26
VCC15	Y1	VCC33	D4	VCCPLL1	M19
VCC15	Y15	VCC33	E9	VCCPLL2	M11
VCC15	Y17	VCC33	F21	VCCPLL4	R15
VCC15	Y19	VCC33	F3	VCCPLL5	P13
VCC25/18	AA10	VCC33	F6	VSS	A10
VCC25/18	AA12	VCC33	G10	VSS	A14
VCC25/18	AA14	VCC33	G23	VSS	A16
VCC25/18	AA16	VCC33	H26	VSS	A17
VCC25/18	AA18	VCC33	H5	VSS	A27

Table 18. 829-Lead Package - Alphabetical Signal Listings (Sheet 6 of 7)

Signal	Ball	Signal	Ball	Signal	Ball
VSS	A3	VSS	AE28	VSS	D23
VSS	AA11	VSS	AE5	VSS	D29
VSS	AA13	VSS	AE8	VSS	D7
VSS	AA15	VSS	AF7	VSS	E10
VSS	AA17	VSS	AG1	VSS	E11
VSS	AA19	VSS	AG12	VSS	E19
VSS	AA27	VSS	AG15	VSS	E2
VSS	AA3	VSS	AG18	VSS	E22
VSS	AA6	VSS	AG21	VSS	E25
VSS	AA9	VSS	AG24	VSS	E5
VSS	AB10	VSS	AG29	VSS	E8
VSS	AB12	VSS	AG3	VSS	F10
VSS	AB14	VSS	AG6	VSS	F12
VSS	AB16	VSS	AG9	VSS	F15
VSS	AB18	VSS	AH14	VSS	F18
VSS	AB2	VSS	AH19	VSS	F24
VSS	AB25	VSS	AH2	VSS	F27
VSS	AB5	VSS	AH22	VSS	F8
VSS	AB6	VSS	AH25	VSS	F9
VSS	AB8	VSS	AH28	VSS	G13
VSS	AC11	VSS	AH5	VSS	G15
VSS	AC17	VSS	AH8	VSS	G17
VSS	AC2	VSS	AJ27	VSS	G20
VSS	AC23	VSS	B11	VSS	G26
VSS	AC3	VSS	B13	VSS	G28
VSS	AC4	VSS	B14	VSS	G4
VSS	AC5	VSS	B15	VSS	G7
VSS	AC6	VSS	B16	VSS	G8
VSS	AC7	VSS	B19	VSS	H14
VSS	AD15	VSS	B2	VSS	H16
VSS	AD21	VSS	B20	VSS	H2
VSS	AD27	VSS	B22	VSS	H25
VSS	AD3	VSS	B25	VSS	H27
VSS	AD9	VSS	B28	VSS	H28
VSS	AE11	VSS	B5	VSS	H29
VSS	AE14	VSS	B8	VSS	J11
VSS	AE16	VSS	C15	VSS	J13
VSS	AE19	VSS	D10	VSS	J15
VSS	AE2	VSS	D13	VSS	J17
VSS	AE22	VSS	D17	VSS	J19
VSS	AE25	VSS	D20	VSS	J21

Table 18. 829-Lead Package - Alphabetical Signal Listings (Sheet 7 of 7)

Signal	Ball	Signal	Ball	Signal	Ball
VSS	J6	VSS	P2	VSS	W19
VSS	J9	VSS	P20	VSS	W2
VSS	K12	VSS	P25	VSS	W25
VSS	K14	VSS	P28	VSS	W28
VSS	K15	VSS	P5	VSS	W4
VSS	K16	VSS	R11	VSS	W9
VSS	K18	VSS	R13	VSS	Y10
VSS	K20	VSS	R17	VSS	Y12
VSS	K23	VSS	R19	VSS	Y14
VSS	K26	VSS	R9	VSS	Y16
VSS	K4	VSS	T10	VSS	Y18
VSS	K7	VSS	T12	VSS	Y20
VSS	L11	VSS	T14	VSS	Y23
VSS	L13	VSS	T16	VSS	Y3
VSS	L14	VSS	T18	VSS	Y4
VSS	L15	VSS	T2	VSS	Y7
VSS	L16	VSS	T20	VSSA1	M18
VSS	L17	VSS	T25	VSSA2	M12
VSS	L19	VSS	T28	VSSA4	R16
VSS	L2	VSS	T5	VSSA5	P14
VSS	L21	VSS	T7	WE#	AD20
VSS	L28	VSS	U11		
VSS	L9	VSS	U13		
VSS	M10	VSS	U15		
VSS	M14	VSS	U17		
VSS	M16	VSS	U19		
VSS	M20	VSS	U23		
VSS	M24	VSS	U4		
VSS	N11	VSS	U9		
VSS	N13	VSS	V10		
VSS	N15	VSS	V12		
VSS	N17	VSS	V14		
VSS	N19	VSS	V16		
VSS	N21	VSS	V18		
VSS	N4	VSS	V20		
VSS	N7	VSS	V27		
VSS	N9	VSS	V6		
VSS	P10	VSS	W11		
VSS	P12	VSS	W13		
VSS	P16	VSS	W15		
VSS	P18	VSS	W17		

3.2 Package Thermal Specifications

See *Intel® 80331 I/O Processor Thermal Design Guidelines Application Note* (273980).

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

Table 19. Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–55° C to +125°C
Case Temperature Under Bias	0°C to +95°C
Supply Voltage V_{CC33} wrt. V_{SS}	–0.5 V to +4.1 V
Supply Voltage V_{CC25} wrt. V_{SS}	–0.5 V to +3.2 V
Supply Voltage V_{CC15} wrt. V_{SS}	–0.5 V to +2.1 V
Supply Voltage V_{CC13} wrt. V_{SS}	–0.5 V to +2.1 V
Voltage on Any Ball wrt. V_{SS}	–0.5 V to V_{CCP} + 0.5 V

NOTE: This data sheet contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product becomes available. The specifications are subject to change without notice. Contact your local Intel representative before finalizing a design.

WARNING: Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only. Operation beyond the Operating Conditions is not recommended and extended exposure beyond the Operating Conditions may affect device reliability.

Table 20. Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{CC33}	3.3 V PCI/PCI-X Supply Voltage	3.0	3.6	V	+/- 10%
$V_{CC25/18}$	2.5 V/1.8V DDR/DDR-II Supply Voltage	2.3/1.7	2.7/1.9	V	+/-8%, 5%[1]
V_{CC15}	1.5 V IOP Core Supply Voltage	1.425	1.575	V	+/- 5%[1]
V_{CC13}	1.35 V Intel XScale® core Supply Voltage	1.282	1.418	V	+/- 5%
$V_{CCPLL1-5}$	PLL Supply Voltage	V_{CC15}	V_{CC15}	V	
DDR_VREF	Memory I/O Reference Voltage	0.49$V_{CC25/18}$	0.51 $V_{CC25/18}$	V	
P_CLK	Input Clock Frequency	16	133	MHz	
T_C	Case Temperature Under Bias	0	95	°C	

1. +/- 3% DC; additional +/- 2% for AC transients. Under no circumstance may the supply voltage go past the AC min/max window. The supply voltage window may go outside the DC min/max window for transient events.

4.2 V_{CCPLL} Pin Requirements

The $V_{CCPLL[1-5]}$ balls for the Phase Lock Loop (PLL) circuit must each have filters, and be connected to the appropriate VSSA ball. See the *Intel® 80331 I/O Processor Design Guide* for specific recommendations.

NOTE: There are no VCCPLL3 or VSSA3 signals.

4.3 Targeted DC Specifications

Table 21. DC Characteristics

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{IL1}	Input Low Voltage (DDR SDRAM)	-0.3	**DDR_VREF** - 0.18	V	(1, 2)
V_{IH1}	Input High Voltage (DDR SDRAM)	**DDR_VREF** + 0.18	$\mathbf{V_{CC25}}$ + 0.3	V	(1, 2)
V_{IL2}	Input Low Voltage (DDR-II SDRAM)	-0.2	**DDR_VREF** - 0.125	V	(1, 3)
V_{IH2}	Input High Voltage (DDR-II SDRAM)	**DDR_VREF** + 0.125	$\mathbf{V_{CC25}}$ + 0.2	V	(1, 3)
V_{IL2}	Input Low Voltage (Misc.)	-0.3	0.8	V	(4)
V_{IH2}	Input High Voltage (Misc.)	2.0	$\mathbf{V_{CC33}}$ + 0.3	V	(4)
V_{IL3}	Input Low Voltage (PCI-X)	-0.5	0.35 $\mathbf{V_{CC33}}$	V	
V_{IH3}	Input High Voltage (PCI-X/PCI)	0.5 $\mathbf{V_{CC33}}$	$\mathbf{V_{CC33}}$ + 0.5	V	
V_{IL5}	Input Low Voltage (PCI)	-0.5	0.3 $\mathbf{V_{CC33}}$	V	
V_{OL2}	Output Low Voltage (Misc.)		0.4	V	$\mathbf{I_{OL}}$ = 6 mA
V_{OH2}	Output High Voltage (Misc.)	2.4		V	$\mathbf{I_{OH}}$ = -2 mA
V_{OL1}	Output Low Voltage (DDR SDRAM)		0.35	V	$\mathbf{I_{OL}}$ = 12.5 mA (1, 2)
V_{OH1}	Output High Voltage (DDR SDRAM)	1.95		V	$\mathbf{I_{OH}}$ = -12.5 mA (1, 2)
V_{OL2}	Output Low Voltage (DDR-II SDRAM)		0.414	V	I_{OL} = 20.7mA (3)
V_{OH2}	Output High Voltage (DDR-II SDRAM)	1.314		V	I_{OH} = -18mA (3)
V_{OL3}	Output Low Voltage (PCI-X)		0.1 $\mathbf{V_{CC33}}$	V	$\mathbf{I_{OL}}$ = 1500 µA
V_{OH3}	Output High Voltage (PCI-X)	0.9 $\mathbf{V_{CC33}}$		V	$\mathbf{I_{OH}}$ = -500 µA
C_{IN}	Input pin Capacitance		8	pF	(5)
C_{CLK}	PCI clock pin Capacitance		8	pF	(5)
L_{PIN}	Ball Inductance		15	nH	(1, 2, 5)

NOTES:
1. SDRAM signals include **MA[12:0]**, **BA[1:0]**, **CAS#**, **CS[1:0]#**, **CKE[1:0]**, **DM[8:0]**, **RAS#**, **WE#**,**M_CK[2:0]**, **M_CK[2:0]#**, **DQ[63:0]**, **DQS[8:0]** and **CB[7:0]**.
2. For 2.5 V DDR SDRAM support.
3. For 1.8 V DDR-II SDRAM support.
4. Miscellaneous signals include all signals that are not PCI-X or SDRAM signals.
5. Ensured by design.

Table 22. I_{CC} Characteristics

Symbol	Parameter	Typ	Max	Units	Notes
I_{LI1}	Input Leakage Current for each signal except **TCK**, **TMS**, **TRST#**, **TDI**		± 2	µA	$0 \le V_{IN} \le V_{CC}$ (4)
I_{LI2}	Input Leakage Current for **TCK**, **TMS**, **TRST#**, **TDI**	-140	-250	µA	V_{IN} = 0.45 V (1, 4)
I_{CC33} Active (Power Supply)	Power Supply Current - PCI-X interfaces Both at 66 MHz Both at 100 MHz Both at 133 MHz		 1.33 1.20 1.04	 A	(1, 2)
I_{CC25} Active (Power Supply)	Power Supply Current - DDR		0.580	A	(1, 2)
I_{CC18} Active (Power Supply)	Power Supply Current - DDR-II		0.487	A	(1, 2)
I_{CC15} Active (Power Supply)	Power Supply Current - IOP/Bridge core		3.2	A	(1, 2)
I_{CC13} Active (Power Supply)	Power Supply Current - Intel XScale® core 800 MHz 667 MHz 500 MHz		 0.453 0.411 0.358	 A	(1, 2)
I_{CC33} Active (Thermal)	Thermal Current - PCI-X interfaces Both at 66 MHz Both at 100 MHz Both at 133 MHz	 1.08 1.00 0.914		 A	(1, 3)
I_{CC25} Active (Thermal)	Thermal Current - DDR	0.295		A	(1, 3)
I_{CC18} Active (Thermal)	Thermal Current - DDR-II	0.255		A	(1, 3)
I_{CC15} Active (Thermal)	Thermal Current - IOP/Bridge core	2.5		A	(1, 3)
I_{CC13} Active (Thermal)	Thermal Current - Intel XScale® core 800 MHz 667 MHz 500 MHz	 0.430 0.390 0.340		 A	(1, 3)

NOTES:
1. Measured with device operating and outputs loaded to the test condition in Figure 14 “AC Test Load for All Signals Except PCI and DDR SDRAM” on page 67.
2. I_{CC} Active (Power Supply) value is provided for selecting the system power supply. This is based on the worst case data patterns and skew material at the following worst case voltages: V_{CC33} = 3.63 V, V_{CC25} = 2.7 V, V_{cc18} = 1.9v, V_{CC15} = 1.575 V, V_{CC13} = 1.41 V.
3. I_{CC} Active (Thermal) value is provided for selecting the system thermal design power (TDP). This is based on the following typical voltages: V_{CC33} = 3.3 V, V_{CC25} = 2.5 V, V_{cc18} = 1.8v, V_{CC15} = 1.5 V, V_{CC13} = 1.35 V.
4. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.

4.4 Targeted AC Specifications

4.4.1 Clock Signal Timings

Table 23. PCI Clock Timings

Symbol	Parameter	PCI-X 133		PCI-X 100		PCI-X 66		PCI 66		PCI 33		Units	Notes
		Min.	Max	Min.	Max	Min.	Max	Min.	Max	Min.	Max		
T_{F1}	PCI clock Frequency	100	133	66	100	50	66	33	66	16	33	MHz	1
T_{C1}	PCI clock Cycle Time - Avg.	7.5	10	10	15	15	20	15	30	30	60	ns	1
	Absolute Minimum	7.375		9.875		14.8		14.8		29.7		ns	3, 4
T_{CH1}	PCI clock High Time	3		3		6		6		11		ns	
T_{CL1}	PCI clock Low Time	3		3		6		6		11		ns	
T_{SR1}	PCI clock Slew Rate	1.5	4	1.5	4	1.5	4	1.5	4	1	4	V/ns	2
PCI Spread Spectrum Requirements													
f_{mod}	PCI clock modulation frequency	30	33	30	33	30	33	30	33			KHz	
f_{spread}	PCI clock frequency spread	-1	0	-1	0	-1	0	-1	0			%	

NOTES:
1. Clock frequency may not change beyond spread-spectrum limits except while is asserted.
2. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform.
3. The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.
4. Clock jitter class 2, per PCI-X Electrical and Mechanical Rev 2.0a specification

Table 24. DDR Clock Timings

Symbol	Parameter	DDR-II 400		DDR333		Units	Notes
		Minimum	Maximum	Minimum	Maximum		
T_{F2}	DDR SDRAM clock Frequency		200		167	MHz	
T_{C2}	DDR SDRAM clock Cycle Time	5.0		6.0/7.5(1)		ns	
T_{CH2}	DDR SDRAM clock High Time	2.15		2.7/3.37(1)		ns	
T_{CL2}	DDR SDRAM clock LowTime	2.15		2.7/3.37(1)		ns	
T_{CS2}	DDR SDRAM clock Period Stability		350		350	ps	
T_{skew2}	DDR SDRAM clock skew for any differential clock pair (**M_CK[2:0]** - **M_CK[2:0]#**)		100		100	ps	
T_{skew3}	DDR SDRAM clock skew for any clock pair and any system memory strobe (**M_CK** - **DQS**).	-285	285	-285	285	ps	2

NOTES:
1. CL = 2.5/2.0.
2. This specification applies for writes only; that is, when the 80331 is driving the strobes as well as the clocks. Refer to the JEDEC specification for an explanation of strobe to clock timing for DDR reads.

4.4.2 DDR/DDR-II SDRAM Interface Signal Timings

Table 25. DDR SDRAM Signal Timings

Symbol	Parameter	Minimum	Max.	Units	Notes
T_{VB1}	DQ, CB and DM write output valid time before DQS.	2.68		ns	(4)
T_{VA1}	DQ, CB and DM write output valid time after DQS.	2.68		ns	(4)
T_{VB3}	Address and Command write output valid before M_CK rising edge.	2.62		ns	(4,8)
T_{VA3}	Address and Command write output valid after M_CK rising edge.	2.62		ns	(4,8)
T_{VB4}	DQ, CB and DM read input valid time before DQS rising or falling edges.	0.35		ns	(5)
T_{VA4}	DQ, CB and DM read input valid time after DQS rising or falling edges.	0.35		ns	(5)
T_{VB5}	CS[1:0]# control valid before M_CK rising edge.	2.62		ns	(4)
T_{VA5}	CS[1:0]# control valid after M_CK rising edge.	2.62		ns	(4)
T_{VB6}	DQS write preamble duration.	4.50 (nominal)		ns	(6)
T_{VA6}	DQS write postamble duration.	3.00 (nominal)		ns	(6)

NOTES:
1. See Figure 7 “Output Timing Measurement Waveforms” on page 63.
2. See Figure 8 “Input Timing Measurement Waveforms” on page 64.
3. Clock to output valid times are specified with a 0 pF loading.
4. See Figure 11 “DDR SDRAM Write Timings” on page 65.
5. See Figure 12 “DDR SDRAM Read Timings” on page 65.
6. See Figure 13 “Write PreAmble/PostAmble Durations” on page 66.
7. See Figure 15 “AC Test Load for DDR SDRAM Signals” on page 67.
8. Address/Command pin group; **RAS#**, **CAS#**, **WE#**, **MA[12:0]**, **BA[1:0]**.

Table 26. DDR-II SDRAM Signal Timings

Symbol	Parameter	Mini	Max	Units	Notes
T_{VB1}	DQ, CB and DM write output valid time before DQS crossing.	2.12		ns	4
T_{VA1}	DQ, CB and DM write output valid time after DQS crossing.	2.12		ns	4
T_{VB3}	Address and Command write output valid before M_CK rising edge	2.12		ns	4
T_{VA3}	Address and Command write output valid after M_CK rising edge	2.12		ns	4,8
T_{VB4}	DQ, CB and DM read input valid time before DQS rising or falling edges	0.35		ns	6
T_{VA4}	DQ, CB and DM read input valid time after DQS rising or falling edges	0.35		ns	6
T_{VB5}	CS[1:0]# control valid before M_CK rising edge.	2.12		ns	4
T_{VA5}	CS[1:0]# control valid after M_CK rising edge.	2.12		ns	4
T_{VB6}	DQS write preamble duration.	3.75 (nom)		ns	9
T_{VA6}	DQS write postamble duration.	2.50 (nom)		ns	9

NOTES:
1. See Figure 7 “Output Timing Measurement Waveforms” on page 63.
2. See Figure 8 “Input Timing Measurement Waveforms” on page 64.
3. Clock to output valid times are specified with a 0 pF loading.
4. See Figure 11 “DDR SDRAM Write Timings” on page 65.
5. See Figure 13 “DQS falling edge output access time to M_CK rising edge.
6. See Figure 12 “DDR SDRAM Read Timings” on page 65. Data to strobe read setup and data from strobe read hold minimum requirements specified are determined with the DQS delay programmed for a 90 degree phase shift.
7. See Figure 15 “AC Test Load for DDR SDRAM Signals” on page 67.
8. Address/Command pin group: **RAS#, CAS#, WE#, MA[12:0], BA[1:0], ODT[1:0]**.
9. See Figure 13 “Write PreAmble/PostAmble Durations” on page 66.

4.4.3 Peripheral Bus Interface Signal Timings

Table 27. Peripheral Bus Signal Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{OV1}	Output Valid Delay from M_CK	1	5	ns	(1, 3)
T_{OF}	Output Float Delay from M_CK	1	5	ns	(1, 3)
T_{IS1}	Input Setup to M_CK	4.5		ns	(2)
T_{IH1}	Input Hold from M_CK	2		ns	(2)
T_{AH1}	**ALE** High time	15		ns	
T_{AV1}	**ALE** high to address Valid		0	ns	
T_{AH2}	**ALE** low to address invalid		15	ns	
T_{AS1}	Address valid to **ALE** low	15		ns	
T_{AO1}	**ALE** low to POE# low	0		ns	
T_{AW1}	**ALE** low to PWE# low	15		ns	
T_{AH3}	PWE# high to Data Invalid	15		ns	
T_{AS2}	Data valid to PWE# high	60		ns	
T_{AC1}	**ALE** low to PCE[1:0]# low	15		ns	

NOTES:
1. See Figure 7 “Output Timing Measurement Waveforms” on page 63.
2. See Figure 8 “Input Timing Measurement Waveforms” on page 64.
3. See Figure 14 “AC Test Load for All Signals Except PCI and DDR SDRAM” on page 67.
4. See Table 32, AC Measurement Conditions.
5. All timing referenced to M_CK is for functional testing, for the cases where M_CK * N = IBCLK.
6. PBI Clock is internal only; 66 MHz with 266 MHz internal bus.

Table 28. PCI Signal Timings

Symbol	Parameter	PCI-X 133 PCI-X 100		PCI-X 66		PCI 66		PCI 33		Units	Notes
		Min.	Max	Min.	Max	Min.	Max	Min.	Max		
T_{OV1}	Clock to Output Valid Delay for bused signals	0.7	3.8	0.7	3.8	1	6	2	11	ns	(1,2,3)
T_{OV2}	Clock to Output Valid Delay for point to point signals	0.7	3.8	0.7	3.8	2	6	2	12	ns	(1,2,3)
T_{OF}	Clock to Output Float Delay		7		7		14		28	ns	(1,7)
T_{IS1}	Input Setup to clock for bused signals	1.2		1.7		3		7		ns	(3,4,8)
T_{IS2}	Input Setup to clock for point to point signals	1.2		1.7		5		10, 12		ns	(3,4)
T_{IH1}	Input Hold time from clock	0.5		0.5		0		0		ns	(4)
T_{RST}	Reset Active Time	1		1		1		1		ms	
T_{RF}	Reset Active to output float delay		40		40		40		40	ns	(5,6)
T_{IS3}	REQ64# to Reset setup time	10		10		10		10		clocks	
T_{IH2}	Reset to REQ64# hold time	0	50	0	50	0	50	0	50	ns	
T_{IS4}	PCI-X initialization pattern to Reset setup time	10		10						clocks	
T_{IH3}	Reset to PCI-X initialization pattern hold time	0	50	0	50					ns	

NOTES:
1. See the timing measurement conditions in; Figure 7 “Output Timing Measurement Waveforms” on page 63.
2. See Figure 16 “PCI/PCI-X TOV(max) Rising Edge AC Test Load” on page 67, Figure 17 “PCI/PCI-X TOV(max) Falling Edge AC Test Load” on page 68, and Figure 18 “PCI/PCI-X TOV(min) AC Test Load” on page 68.
3. Setup time for point-to-point signals applies to **REQ#** and **GNT**# only. All other signals are bused.
4. See the timing measurement conditions in Figure 8 “Input Timing Measurement Waveforms” on page 64.
5. RST# is asserted and deasserted asynchronously with respect to **CLK.**
6. All output drivers must be floated when **RST#** is active.
7. For purposes of Active/Float timing measurements, the HI-Z or ‘off’ state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.

4.4.4 I²C Interface Signal Timings

Table 29. I²C Signal Timings

Symbol	Parameter	Std. Mode		Fast Mode		Units	Notes
		Min.	Max	Min.	Max		
F_{SCL}	**SCL** Clock Frequency	0	100	0	400	KHz	
T_{BUF}	Bus Free Time Between STOP and START Condition	4.7		1.3		µs	(1)
T_{HDSTA}	Hold Time (repeated) START Condition	4		0.6		µs	(1, 3)
T_{LOW}	**SCL** Clock Low Time	4.7		1.3		µs	(1, 2)
T_{HIGH}	**SCL** Clock High Time	4		0.6		µs	(1, 2)
T_{SUSTA}	Setup Time for a Repeated START Condition	4.7		0.6		µs	(1)
T_{HDDAT}	Data Hold Time	0	3.45	0	0.9	µs	(1)
T_{SUDAT}	Data Setup Time	250		100		ns	(1)
T_{SR}	**SCL** and **SDA** Rise Time		1000	20+0.1C_b	300	ns	(1, 4)
T_{SF}	**SCL** and **SDA** Fall Time		300	20+0.1C_b	300	ns	(1, 4)
T_{SUSTO}	Setup Time for STOP Condition	4		0.6		µs	(1)

NOTES:
1. See Figure 9 “I2C/SMBus Interface Signal Timings” on page 64.
2. Not tested.
3. After this period, the first clock pulse is generated.
4. C_b = the total capacitance of one bus line, in pF.I²C

4.4.5 UART Interface Signal Timings

Table 30. UART Signal Timings

Symbol	Parameter	Std. Mode		Units	Notes
		Min.	Max		
T_{XD1}	Ux_TXD output delay from M_CK rising edge		60	ns	1
T_{RXS1}	Ux_RXD data setup time (to M_CK rising edge).	50		ns	
T_{RXH1}	Ux_RXD data hold time (to M_CK rising edge).	50		ns	
T_{CTS1}	Ux_CTS setup time (to M_CK rising edge).	60		ns	
T_{CTH1}	Ux_CTS hold time (to M_CK rising edge).	60		ns	
T_{RTS1}	Ux_RTS setup time (to M_CK rising edge).	60		ns	
T_{RTH1}	Ux_RTS hold time (to M_CK rising edge).	60		ns	

1. See Figure 10 “UART Transmitter Receiver Timing” on page 64.

4.4.6 Boundary Scan Test Signal Timings

Table 31. Boundary Scan Test Signal Timings

Symbol	Parameter	Min.	Max	Units	Notes
T_{BSF}	**TCK** Frequency	0	$0.5T_F$	MHz	
T_{BSCH}	**TCK** High Time	15		ns	Measured at 1.5 V (1).
T_{BSCL}	**TCK** Low Time	15		ns	Measured at 1.5 V (1).
T_{BSCR}	**TCK** Rise Time		5	ns	0.8 V to 2.0 V (1)
T_{BSCF}	**TCK** Fall Time		5	ns	2.0 V to 0.8 V (1)
T_{BSIS1}	Input Setup to **TCK** — **TDI**, **TMS**	3		ns	(4)
T_{BSIH1}	Input Hold from **TCK** — **TDI**, **TMS**	5		ns	(4)
T_{BSOV1}	**TDO** Valid Delay	5	15	ns	Relative to falling edge of **TCK** (2, 3).
T_{OF1}	**TDO** Float Delay	5	15	ns	Relative to falling edge of **TCK** (2, 5).

NOTES:
1. Not tested.
2. Outputs precharged to V_{CC5}.
3. See Figure 7 “Output Timing Measurement Waveforms” on page 63.
4. See Figure 8 “Input Timing Measurement Waveforms” on page 64.
5. A float condition occurs when the output current becomes less than ILO. Float delay is not tested. See Figure 7 “Output Timing Measurement Waveforms” on page 63.

4.5 AC Timing Waveforms

Figure 6. Clock Timing Measurement Waveforms

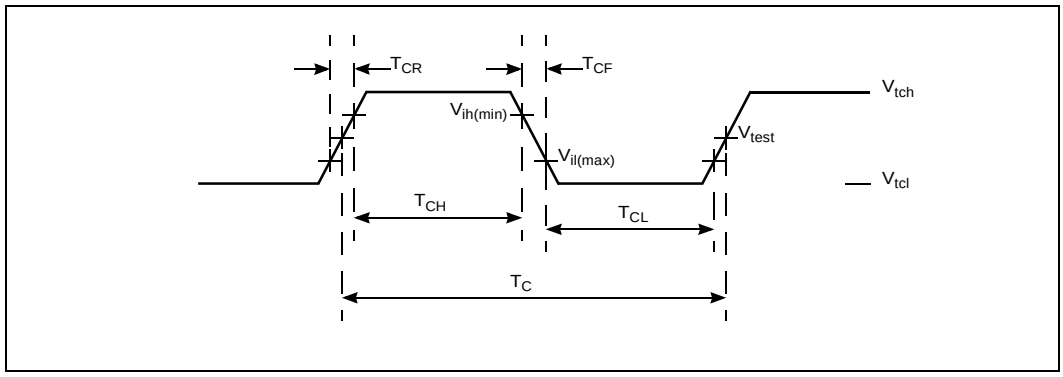


Figure 7. Output Timing Measurement Waveforms

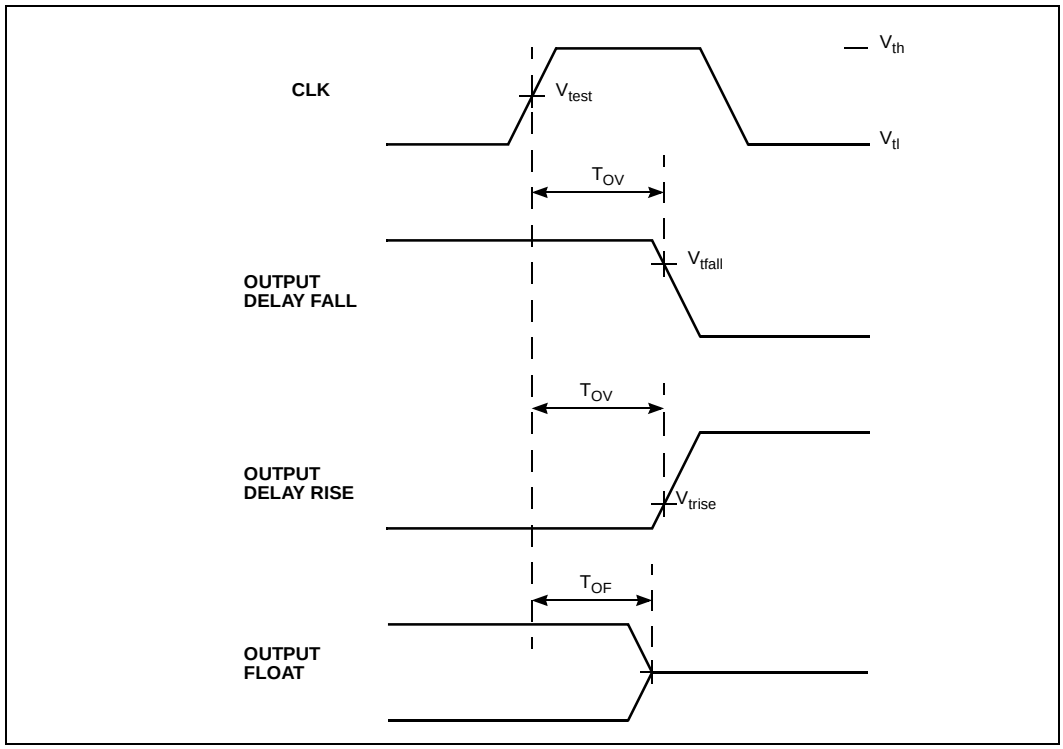


Figure 8. Input Timing Measurement Waveforms

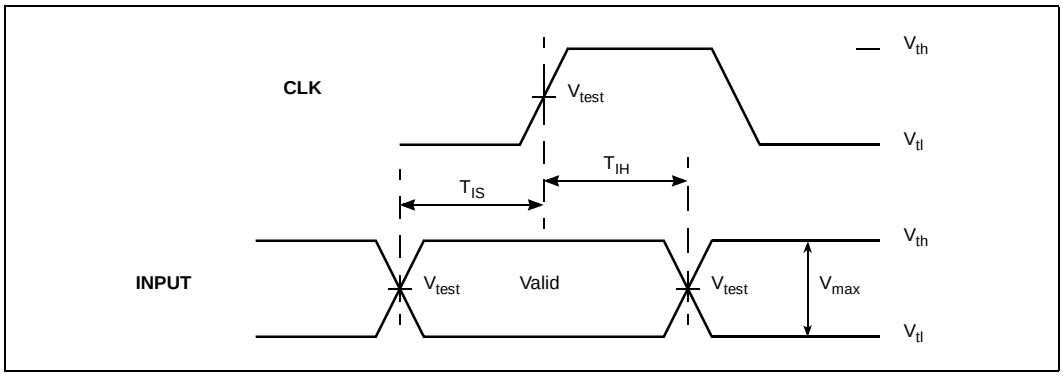


Figure 9. I²C/SMBus Interface Signal Timings

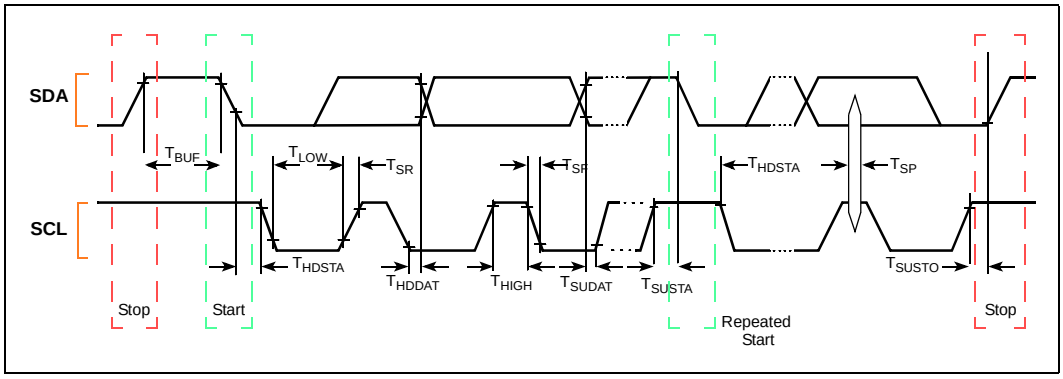


Figure 10. UART Transmitter Receiver Timing

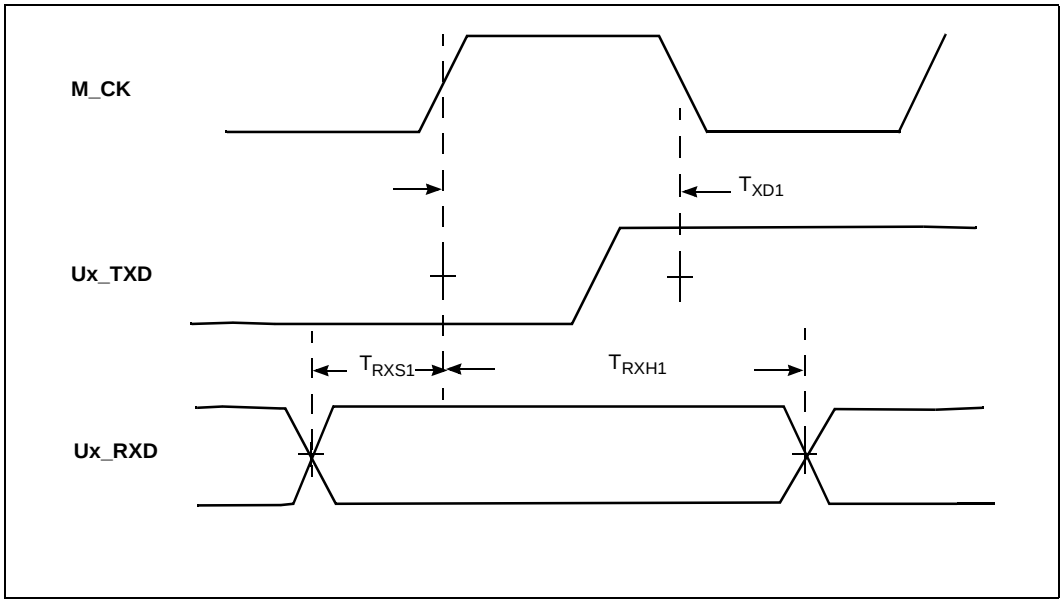


Figure 11. DDR SDRAM Write Timings

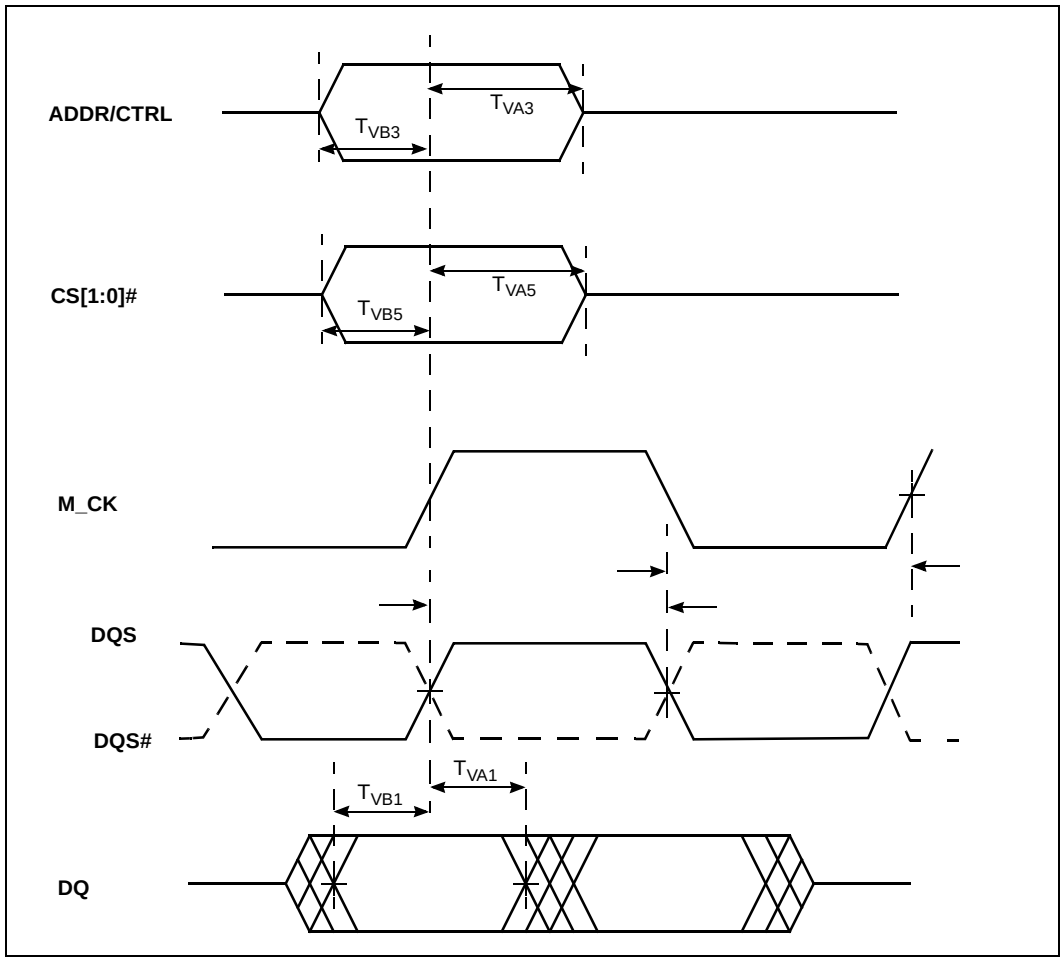


Figure 12. DDR SDRAM Read Timings

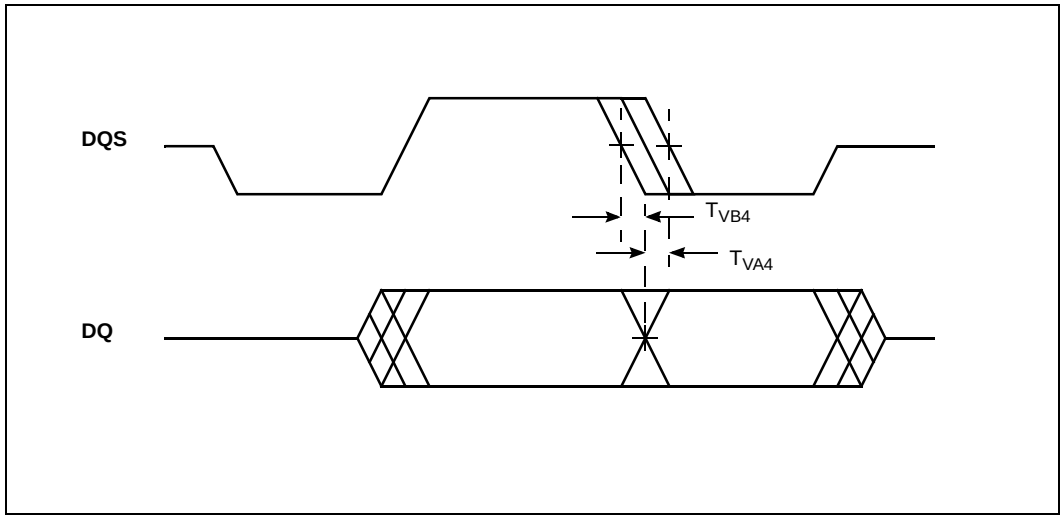
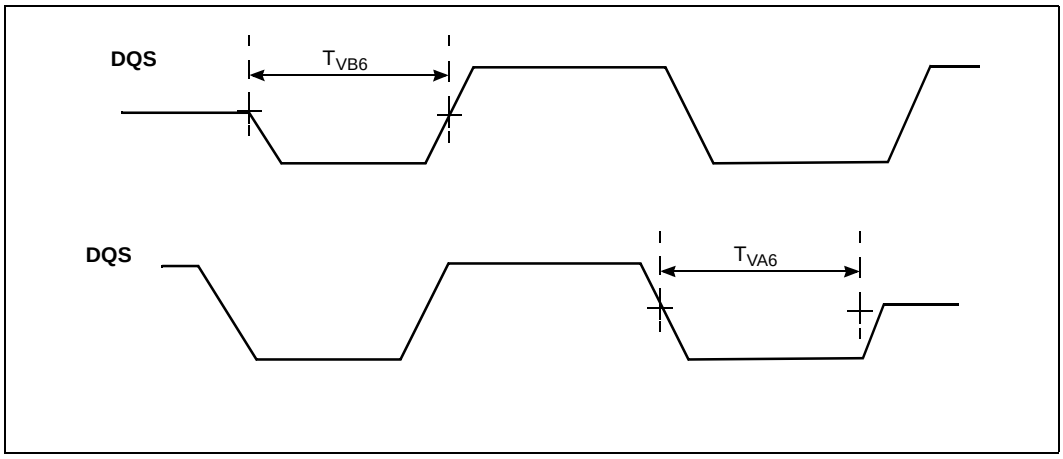


Figure 13. Write PreAmble/PostAmble Durations



4.6 AC Test Conditions

Table 32. AC Measurement Conditions

Symbol	PCI-X	PCI	DDR	DDR-II	PBI	Units
V_{th}	0.6 V_{CC33}	0.6 V_{CC33}	2.0	1.15	2.0	V
V_{tl}	0.25 V_{CC33}	0.2 V_{CC33}	0.5	0.2	0.8	V
V_{test}	0.4 V_{CC33}	0.4 V_{CC33}	1.25	0.90	1.5	V
V_{trise}	0.285 V_{CC33}	0.285 V_{CC33}	1.25	0.90	1.5	V
V_{tfall}	0.615 V_{CC33}	0.615 V_{CC33}	1.25	0.90	1.5	V
V_{max}	0.4 V_{CC33}	0.4 V_{CC33}	1.5	0.97	1.2	V
Slew Rate (1)	1.5	1.5	1.0	1.0	1.0	V/nS

1. Input signal slew rate is measured between V_{il} and V_{ih}.

Figure 14. AC Test Load for All Signals Except PCI and DDR SDRAM

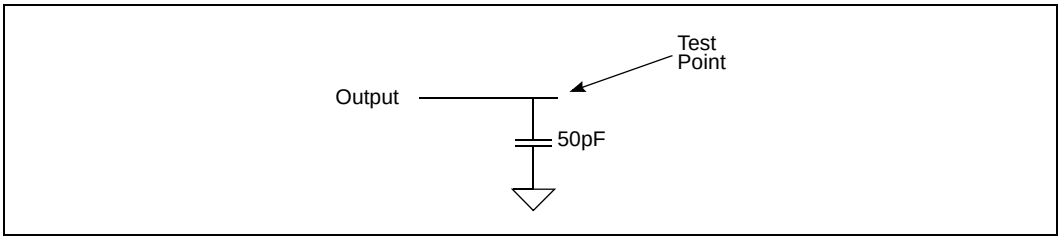


Figure 15. AC Test Load for DDR SDRAM Signals

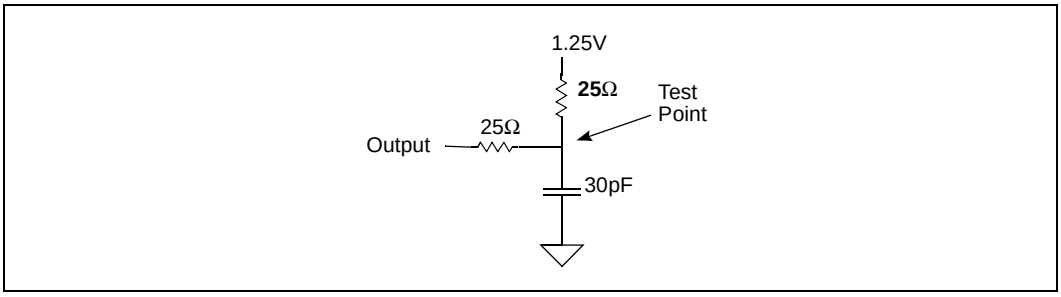


Figure 16. PCI/PCI-X $T_{OV(max)}$ Rising Edge AC Test Load

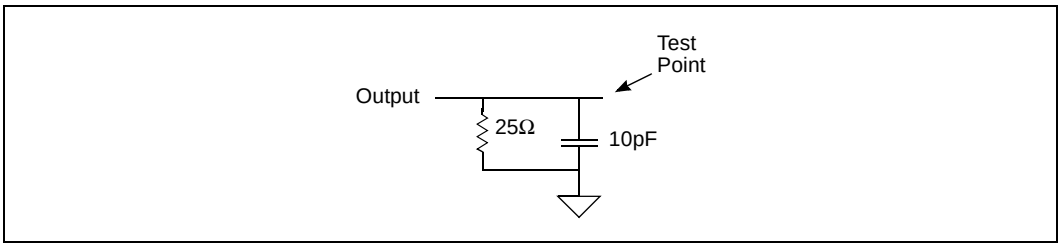


Figure 17. PCI/PCI-X $T_{OV(max)}$ Falling Edge AC Test Load

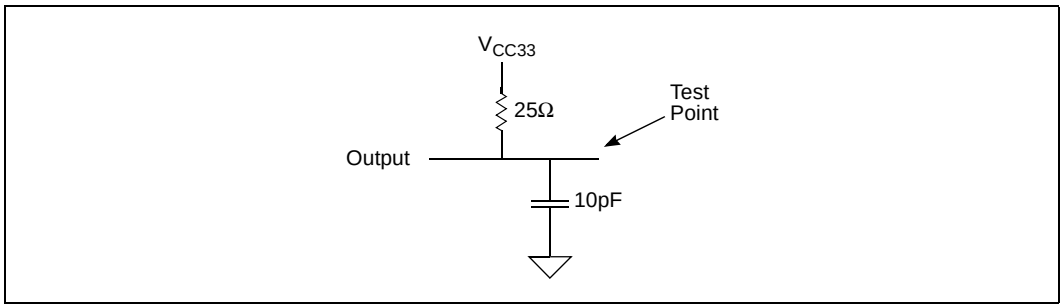


Figure 18. PCI/PCI-X $T_{OV(min)}$ AC Test Load