PI7C7100

3 Port PCI-to-PCI Bridge

Datasheet Brief

Product Features

- All three ports compliant with the *PCI Local Bus Specification, Revision 2.1*
- Compliant with *PCI-to-PCI Bridge Architecture Specification, Revision 1.0*
- 32-Bit Primary and two Secondary Ports
- Circular-Delta Bus Architecture
- Concurrent primary to secondary bus operation and independent intra-secondary port channel to reduce traffic on the primary port
- Provides arbitration for two sets of 8 secondary bus masters
  – Programmable 2-level priority arbiters
  – Disable control for use of external arbiter
- Support PCI transactions for:
  – All I/O and memory commands
  – Type 1 to Type 0 configuration conversion (downstream only)
  – Type 1 to Type 1 configuration forwarding
  – Type 1 to special cycle configuration conversion
- Supports posted memory write buffers in all directions
- Implements delayed transactions for all PCI configuration, I/O and memory read commands
- Supports positive medium decoding
- Enhanced address decoding
  – 32-Bit I/O address range
  – 32-Bit memory-mapped I/O address range
  – VGA addressing and VGA palette snooping
  – ISA-aware mode for legacy support in the first 64KB of I/O address range
- IEEE 1149.1 JTAG interface support
- Full scan support
- 3.3V core logic with 5V tolerant 3.3V PCI signaling interface
- 256-pin plastic PBGA package (NA256)
- Supports system transaction ordering rules
- Hot-Plug "Ready"

Product Description

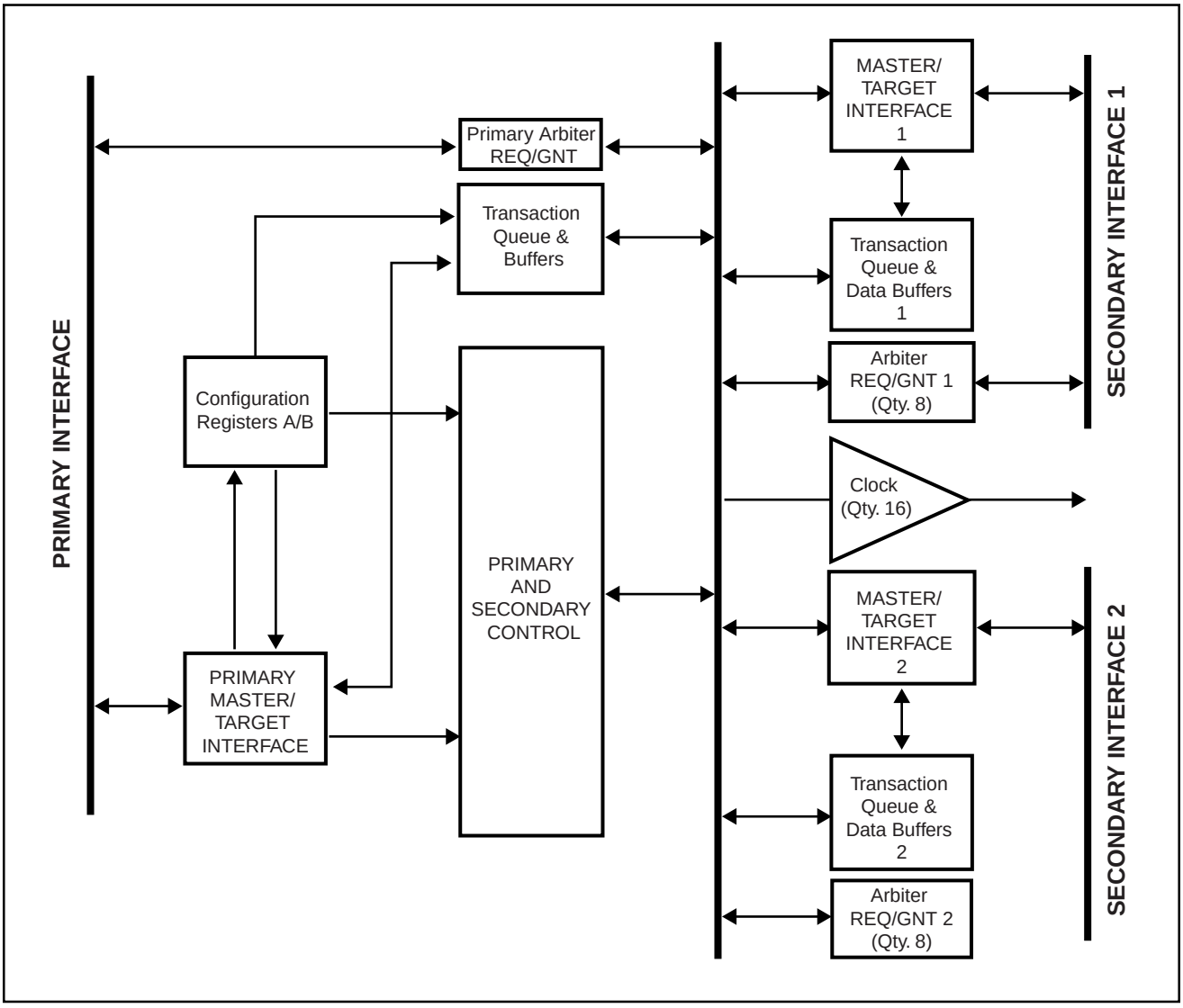
Pericom's PI7C7100 is the first triple port PCI-to-PCI Bridge device designed to be fully compliant with the 32-Bit, 33 MHz implementation of the PCI Local Bus Specification, Revision 2.1.

The PI7C7100 supports synchronous bus transactions between devices on the primary bus and the secondary buses both operating at 33 MHz. The primary and the secondary buses can also operate in concurrent mode, resulting in additional increase in system performance. Concurrent bus operation offloads and isolates unnecessary traffic from the primary bus; thereby enabling a master and a target device on the same secondary PCI bus to communicate even while the primary bus is busy.

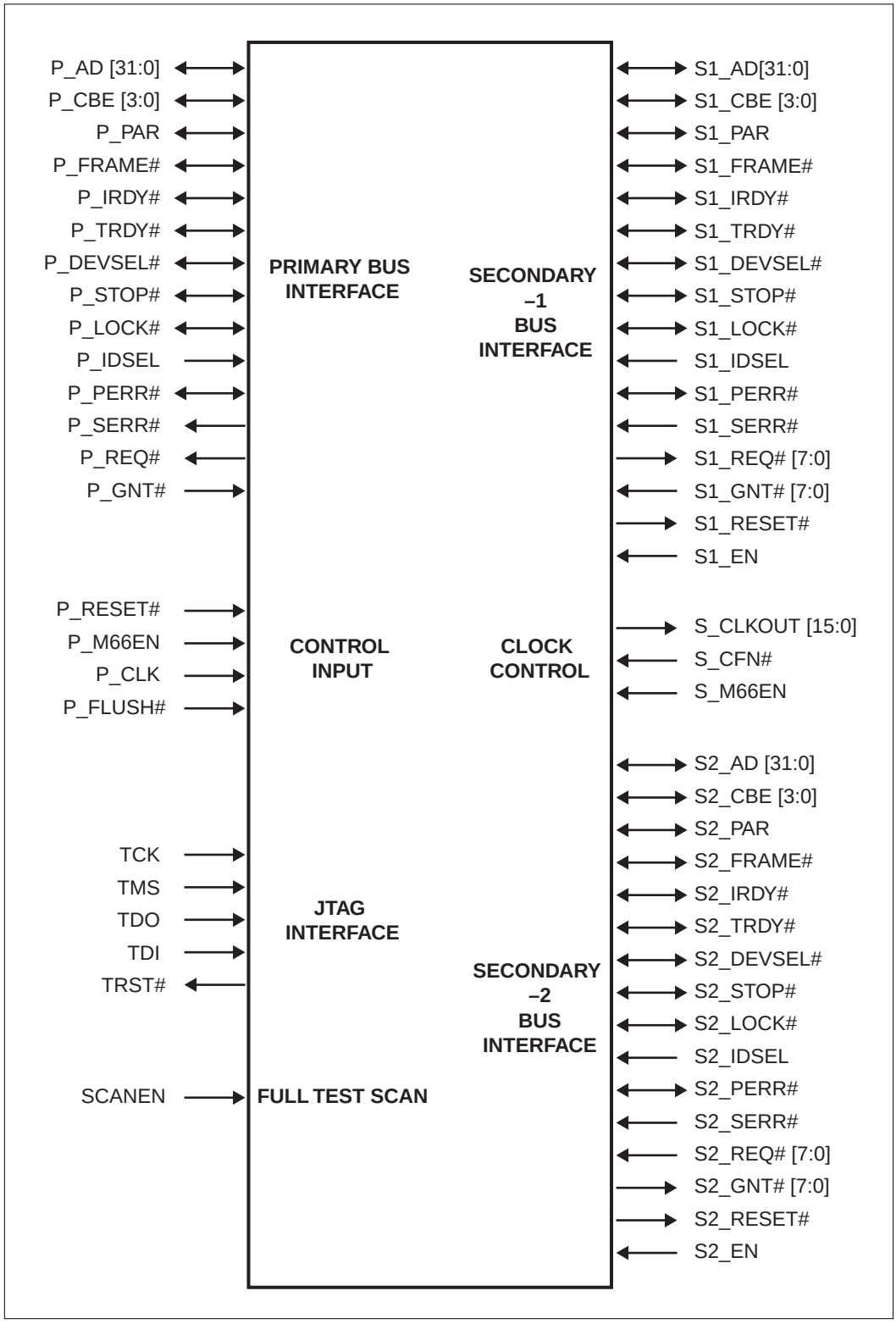
Product Benefits

- Triple port PCI-to-PCI Bridge increases the number of PCI slots that can be supported in a system.
- Single PI7C7100 device instead of two PCI-to-PCI Bridge devices conserves board real estate and provides one less device load on the primary bus.
- Concurrent and intra-secondary bus communication increases overall system performance by reducing bus traffic on the primary bus. Devices on secondary busses can independently communicate while the primary bus is busy.
- Integrated two-level programmable arbiter support for up to 8 devices on each secondary bus maximizes master device control. The internal arbiter can be bypassed with an external arbiter for custom applications.
- Synchronous clock operation on the primary and secondary busses
- Enhanced PCI bridge performance and efficiency through support for delayed transactions.

PI7C7100 Block Diagram



PI7C7100 Pin Information



Applications

The PI7C7100 extends a system's PCI load capability limit beyond that of a single PCI bus. The dual secondary ports on this device allows system designers to add more PCI devices, or more PCI option card slots, than a single PCI bus can support.

Implementing the special concurrent feature in the PI7C7100 enables maximum data through-put between the primary and the secondary buses with minimal system loading. Figure 1, shows the PI7C7100 system block diagram vs the traditional PCI bridge application to illustrate the system performance enhancement resulting from implementing a PI7C7100.

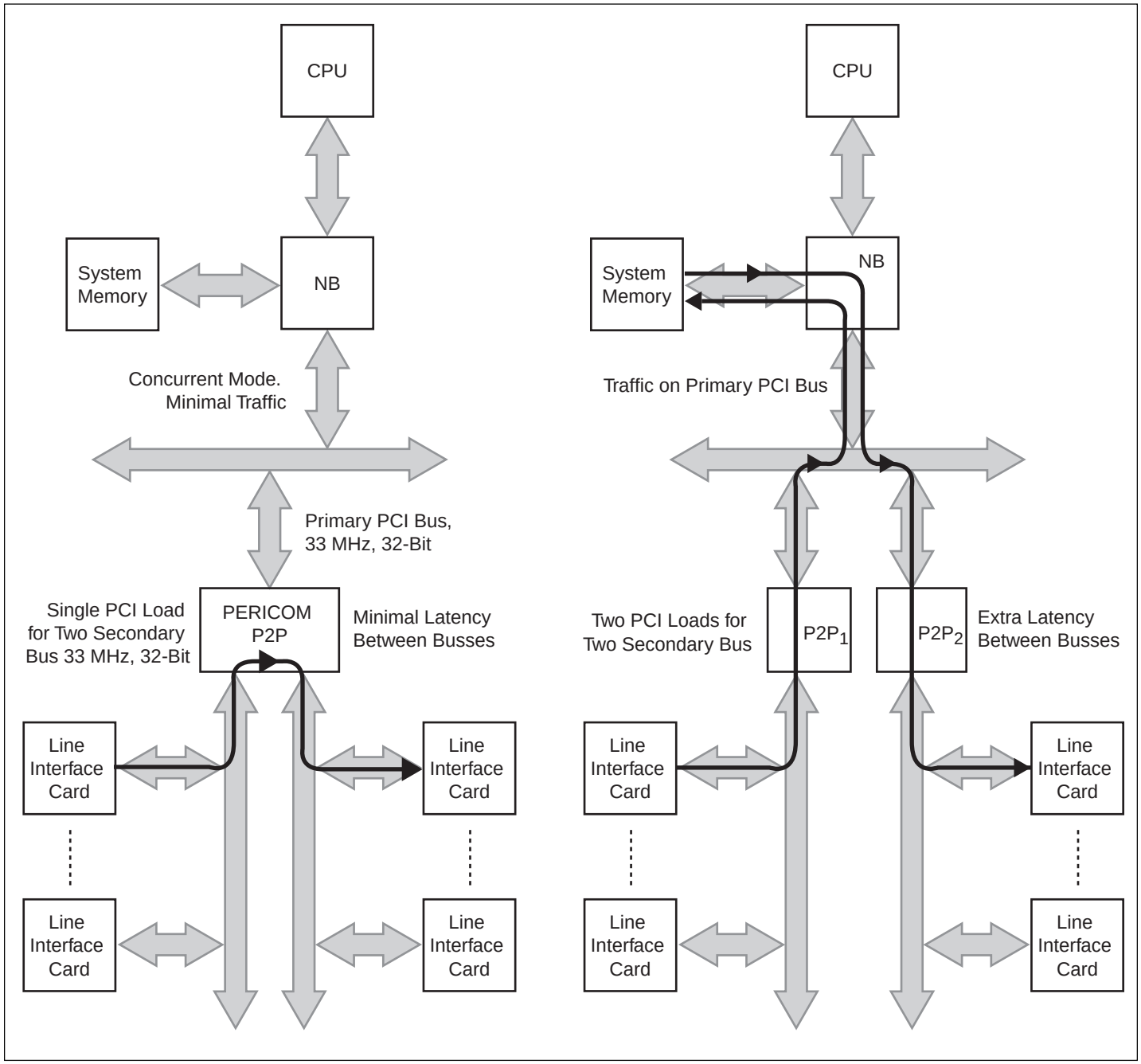


Figure 1. Pericom's Three Port PCI vs. Traditional Two Port PCI in a System Architecture