IMPACT CMOS Base Arrays
IMP Array Conversion Technology

Introduction

The IMPACT™ series of CMOS base arrays is optimized for fast and cost effective conversion to IMP silicon of FPGAs, PLDs and other vendors' CMOS gate arrays. With its own on-shore wafer fabrication facility, IMP is able to support both fast-turn and high-volume, high-quality production demands. As most popular gate arrays and programmable logic netlist formats are supported, there is no need to learn a new CAE system, new tools, or a new library.

Designs are implemented in a family of base arrays ranging from 600 gates with 24 pads, up to 64,000 gates with 256 pads. The sea-of-gates, two-layer metal architecture offers 2-input NAND gate delays of typically 0.3ns. This will meet the performance needs of most FPGA design conversions down to 0.6µ devices.

Many options are supported, including up to 256K of embedded ROM, on-board A to D and D to A functions, and output drive programmable from 2mA up to 48mA

Key Features

- 600 to 64,000 available gates:
- Supports FPGAs down to 0.6µ devices
- Output drive programmable up to 48mA
- Wide package selection (DIP, PLCC, QFP, SOIC, TQFP)
- Operation down to Vcc=3V
- Up to 256K embedded ROM
- A to D and D to A functions
- Slew rate controls
- Power-on resets
- Pull-ups/pull-downs
- Schmitt Triggers
- User reassignable Vcc and GND pins
- In-house on-shore wafer fabrication

Table 1 IMP IMPACT CMOS Base Array Family

Base Array	Pads	Available Gates	Usable Gates	ROM Bits
IMP66100	24	600	400	
IMP66400	36	900	600	
IMP67000	68	2.9K	2.0K	
IMPR0000	74	2.9K	2.0K	64K
IMP67100	84	4.9K	3.2K	
IMPR1100	102	4.9K	3.2K	256K
IMP67200	100	7.4K	4.5K	
IMP67300	128	13.7K	8.2K	
IMP67400	144	17.4K	10.5K	
IMP67500	160	22.7K	13.6K	
IMP67600	184	31.0K	18.6K	
IMP67700	208	41.0K	24.6K	
IMP67800	232	51.8K	31.1K	
IMP67900	256	64.3K	38.6K	

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Table 2 Absolute Maximum Ratings (Vss = 0)

Symbol	Parameter	Rating	Unit
Vdd	DC Supply voltage	-0.3 to +7.0	V
Vin	DC Input Voltage	-0.3 to Vdd+0.3	V
Iin	DC Input Current	±10	V
Tstg	Storage Temperature	-40 to +125	°C

Table 3 Recommended Commercial Operating Conditions (Vss = 0)

Symbol	Parameter	Rating	Unit
Vdd	DC Supply voltage	4.5 to 5.5	V
Ta	Ambient Temperature	0 to +70	°C

Table 4 DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
Vih	High level input voltage				V
	TTL level		2		
	CMOS level		3.5		
	CMOS level Schmitt trigger		2.3		
Vil	Low level input voltage				V
	TTL level			0.8	
	CMOS level			1.5	
	CMOS level Schmitt trigger			1.5	
Iih	High level input current	Vin=Vdd	-10	10	µA
	Input buffer with pull-down	Vin-Vdd	10	50	
Iil	Low level input current	Vin-Vss	-10	10	µA
	Input buffer with pull-up	Vin=Vss	-50	-10	
Voh	High level output voltage	CMOS	Vdd-0.2		V
		Ioh=1mA	2.4		
		Ioh=2mA	2.4		
		Ioh=4mA	2.4		
		Ioh=6mA	2.4		
		Ioh=8mA	2.4		
		Ioh=12mA	2.4		
		Ioh=16mA	2.4		
		Ioh=24mA	2.4		
Vol	Low level output voltage	CMOS		Vss+0.2	V
		Ioh=1mA		2.4	
		Ioh=2mA		2.4	
		Ioh=4mA		2.4	
		Ioh=6mA		2.4	
		Ioh=8mA		2.4	
		Ioh=12mA		2.4	
		Ioh=16mA		2.4	
		Ioh=24mA		2.4	
Ioz	High impedance leakage current	Vout=Vdd or Vss	-10	10	µA
	Output buffer with pull-up	Vout=Vdd or Vss	-50	-10	
	Output buffer with pull-down	Vout=Vdd or Vss	10	50	
Idd	Quiescent supply current	Vin=Vdd or Vss		100	µA