HM63941 Series

Preliminary

4K × 9-Bit CMOS Parallel In-Out FIFO Memory

■ DESCRIPTION

The HM63941 is a First-In, First-Out memory that utilizes a high performance static RAM array with internal algorithm that controls, monitors and declares status of the memory by empty flag, full flag and almost-full flag, to prevent data overflow or underflow.

Expansion logic warrants unlimited expansion capability in width and depth. Both read and write are independent from each other and their corresponding pointers are designed to select the proper locations out of the entire array serially without address information to load or unload data.

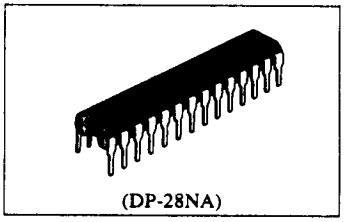
Data is toggled in and out of the device through the use of the write enable ($\overline{W}$) and read enable ($\overline{R}$) pins. The device has a read/write cycle time of 35/45/60ns. Organization of HM63941 provides a 9-bit data bus. the ninth bit could be used for control or parity for error checking at the option of the user. The HM63941 is fabricated using the Hitachi CMOS 1.3micron technology. The device is available in DIP.

■ FEATURES

- First-In, First-Out Dual Port Memory
- 4k × 9 Organization
- Low-Power CMOS 1.3micron Technology
- Asynchronous and Simultaneous Read and Write
- Fully Expandable in Depth and/or Width
- Single 5V (±10%) Power Supply
- Empty and Full Warning Flags
- Almost-Full Flag
- Access Time 25/35/45ns
- Package. . . . . .28-pin DIP Package

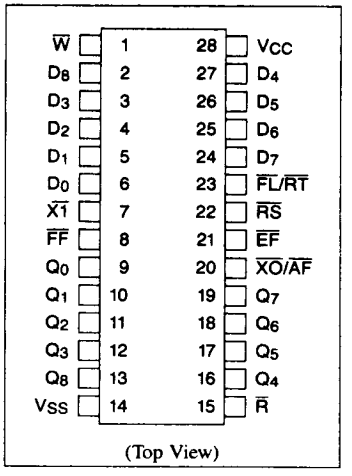
■ ORDERING INFORMATION

Type Name	Access Time	Package
HM63941P-25	25ns	28-pin Plastic DIP
HM63941P-35	35ns	
HM63941P-45	45ns	



(DP-28NA)

■ PIN ARRANGEMENT



(Top View)

■ PIN DESCRIPTION

Pin Name	Function
D_0–D_8	Data inputs
$\overline{RS}$	Reset
$\overline{W}$	Write enable
$\overline{R}$	Read enable
$\overline{FL}$	First load
$\overline{RT}$	Retransmit
$\overline{XI}$	Expansion-in
$\overline{XO}$	Expansion-out
$\overline{AF}$	Almost-full flag
$\overline{FF}$	Full flag
$\overline{EF}$	Empty flag
Q_0–Q_8	Data outputs

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■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage(1)	V_T	−0.5(2) to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

NOTES: 1. Relative to V_{SS}.
2. −3.5V for pulse width ≤ 10ns.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.0	—	6.0	V
	V_{IL}	−0.5(1)	—	0.8	V

NOTE: 1. −3.0V for pulse width ≤ 10ns.

■ DC CHARACTERISTICS (T_a = 0°C to +70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{in} = 0V − V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{R}$ = V_{IH}, V_{out} = 0V − V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC1}	Average Operating Current	—	—	80	mA
	I_{CC2}	$\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}	—	—	10	mA
Standby Power Supply Current	I_{SB}	All Inputs ≥ V_{CC} − 0.2V or ≤ V_{CC}	—	—	1	mA
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V

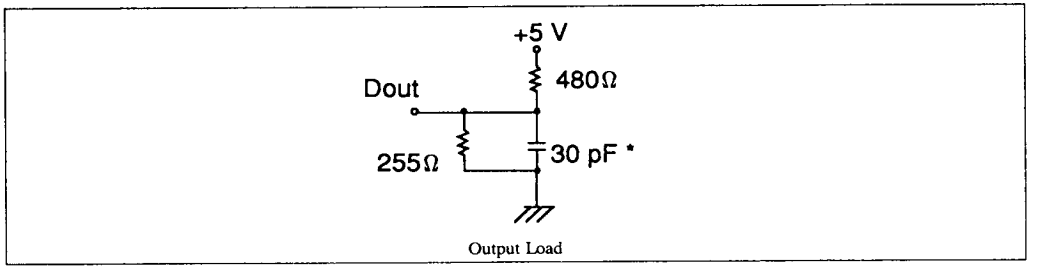
■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Test Conditions	Typ.	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	—	TBD	pF
Output Capacitance	C_{out}	V_{out} = 0V	—	TBD	pF

■ AC CHARACTERISTICS (T_a = 0°C to 70°C, V_{CC} = 5 ± 10%)

• Test Conditions

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Timing Reference Level: 1.5V
- Input Rise and Fall Times: 5ns
- Output Load: See Figure



Output Load

*Including scope and jig.

• **Read Cycle**

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	35	—	45	—	60	—	ns
Access Time	t_A	—	25	—	35	—	45	ns
Read Recovery Time	t_{RR}	10	—	10	—	15	—	ns
Read Pulse Width	t_{RPW}	25	—	35	—	45	—	ns
Read Low to DB Low Z	t_{RLZ}	5	—	5	—	10	—	ns
Read High to DB High Z	t_{RHZ}	—	15	—	20	—	25	ns
Data Valid from Read High	t_{OH}	5	—	5	—	5	—	ns

• **Write Cycle**

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	35	—	45	—	60	—	ns
Write Recovery Time	t_{WR}	10	—	10	—	15	—	ns
Write Pulse Width	t_{WPW}	20	—	35	—	45	—	ns
Data Setup Time	t_{DS}	15	—	20	—	25	—	ns
Data Hold Time	t_{DH}	0	—	0	—	5	—	ns

• **Reset Cycle**

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset Cycle Time	t_{RSC}	35	—	45	—	60	—	ns
Reset Pulse Width	t_{RS}	25	—	35	—	45	—	ns
Reset Recovery Time	t_{RSR}	10	—	10	—	15	—	ns

• **Retransmit Cycle**

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Retransmit Cycle Time	t_{RTC}	35	—	45	—	60	—	ns
Retransmit Pulse Width	t_{RT}	20	—	35	—	45	—	ns
Retransmit Recovery Time	t_{RTR}	10	—	10	—	15	—	ns

• **Flag Timing**

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset to Empty Flag Low	t_{EFL}	—	30	—	45	—	60	ns
Read Low to Empty Flag Low	t_{REF}	—	25	—	35	—	45	ns
Read High to Full Flag High	t_{RFF}	—	25	—	35	—	45	ns
Write High to Empty Flag High	t_{WEF}	—	25	—	35	—	45	ns
Write Low to Full Flag Low	t_{WFF}	—	25	—	35	—	45	ns
Write Low to Almost-Full Low	t_{WAF}	—	30	—	40	—	55	ns
Read High to Almost-Full High	t_{RAF}	—	30	—	40	—	55	ns

SIGNAL DESCRIPTIONS

Inputs

- Reset ($\overline{RS}$)
  The device is reset whenever $\overline{RS}$ input is taken to low state, for minimum reset pulse width. When device is reset, both read and write pointers are set to the first location. A reset cycle is required after power on. Both read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must be in the high state during reset. Empty flag ($\overline{EF}$) will go low and full flag ($\overline{FF}$) and almost-full ($\overline{AF}$) will go high during reset cycle.
- Write enable ($\overline{W}$)
  Write cycle is initiated at the falling edge of $\overline{W}$, if the full flag ($\overline{FF}$) is not set, provided that data set-up and hold time requirements relative to the rising edge of ($\overline{W}$) are met. Data is stored in the device sequentially and independently of any simultaneous read operation. To inhibit further write operations and prevent internal data overflow full flag ($\overline{FF}$) will go low.
- Read enable ($\overline{R}$)
  Read cycle is initiated at the falling edge of $\overline{R}$, if the empty flag ($\overline{EF}$) is not set. Data is accessed on a first-in, first-out basis independently of simultaneous write operation. As read enable ($\overline{R}$) goes high, all outputs will return to high impedance state, till next read operation. After the last data has been read from the FIFO, the empty flag ($\overline{EF}$) will go low, preventing further read operations with output kept in high impedance state. Empty flag ($\overline{EF}$) will go high during a valid write cycle (t_{WEF}), thereafter a valid read can start.
- First load/retransmit ($\overline{FL}/\overline{RT}$)
  For depth expansion mode, this pin is grounded to indicate that it is the first device, while this pin of the rest of devices should connect to V_{CC} for correct operation. In single device mode, this pin resets the read pointer to the beginning of the FIFO memory, therefore data can be reread from the beginning. Both $\overline{R}$ and $\overline{W}$ should be kept high while $\overline{RT}$ is taken low.
- Expansion-in ($\overline{XI}$)
  For single device mode expansion-in ($\overline{XI}$) is grounded. For depth expansion mode, expansion-in ($\overline{XI}$) should be connected to expansion-out ($\overline{XO}$) of previous device.
- Data In (D_0 to D_8)
  Data inputs for 9-bit wide data.

Outputs

- Full Flag ($\overline{FF}$)
  The full flag ($\overline{FF}$) will go low when FIFO is full, inhibiting further write operations until one or more read operations are completed or the FIFO is reset.
- Empty flag ($\overline{EF}$)
  The empty flag ($\overline{EF}$) will go low when the FIFO becomes empty, inhibiting further read operations, until one or more write operations are completed, or FIFO is set to retransmit.
- Expansion-out ($\overline{XO}$)/Almost-full flag ($\overline{AF}$)
  This output has dual functionality depending how it is used. In depth expansion configuration expansion-out ($\overline{XO}$) is connected to next expansion-in ($\overline{XI}$). The expansion-out ($\overline{XO}$) of the last FIFO is connected to the expansion-in ($\overline{XI}$) of the first FIFO. In this way the first FIFO indicates the next FIFO that it will receive the next data. In like manner, any FIFO which becomes full will indicate the next FIFO that it will receive the next data. The second function of this output is in stand alone and/or parallel expansion configurations to indicate the system user that the FIFO is almost full.
- Data outputs (Q_0 to Q_8)
  Data outputs for 9-bit wide data. These outputs are in high impedance state when $\overline{R}$ is in high state.

VARIOUS OPERATIONS MODE

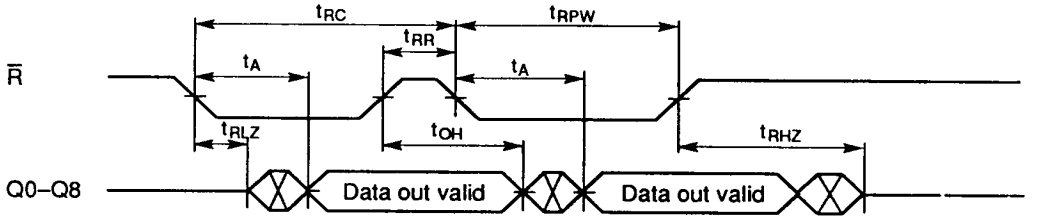
- Single device mode
  If only one FIFO is used, the expansion-in ($\overline{XI}$) pin should be grounded.
- Width expansion mode
  Width expansion by 9-bit increments may be achieved when separately paralleling the data inputs and the data outputs. In this configuration any flags of any device may be used. To avoid output contention of the flags for short periods of time, the flag outputs should not be wired together.
- Depth expansion mode
  Multiple of FIFOs could provide multiple of 4k × 9 as (N) × (4k) by 9-bits wide, where N is the number of FIFOs connected in depth expansion mode.

  The following arrangement must be provided.

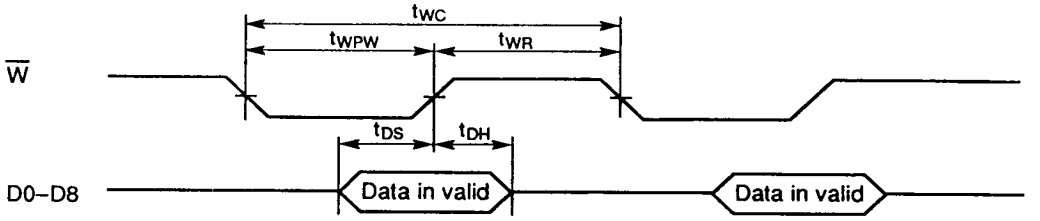
  1. First load ($\overline{FL}$) of the first FIFO should be connected to ground.
  2. All other ($\overline{FL}$) should be connected to V_{CC}.
  3. Connect the expansion-out ($\overline{XO}$) of each FIFO to expansion-in ($\overline{XI}$) of the next FIFO serially and $\overline{XO}$ of the last FIFO to $\overline{XI}$ of the first FIFO.
  4. Connect all the empty flag ($\overline{EF}$) together to OR gate and connect all the full flag ($\overline{FF}$) together to OR gate to obtain two separate valid empty flag ($\overline{EF}$) and full flag ($\overline{FF}$) outputs.
  5. ($\overline{RT}$) and ($\overline{AF}$) will not be available in this mode.
- Compound expansion mode
  Combination of width and depth expansion modes will provide larger FIFO arrays.

■ TIMING WAVEFORM

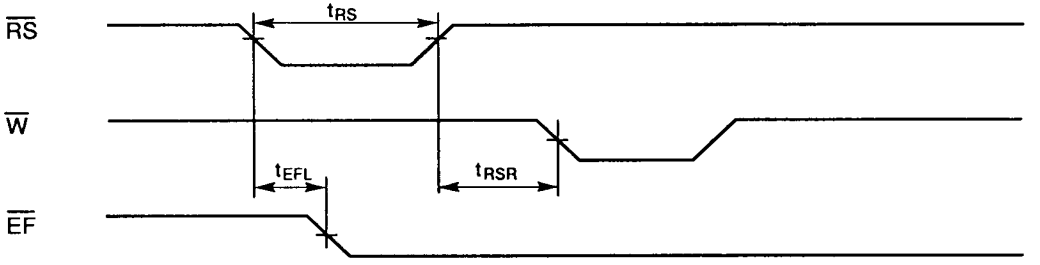
• Read Cycle



• Write Cycle

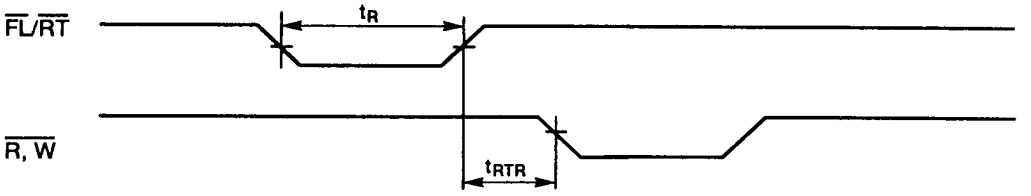


• Reset Cycle

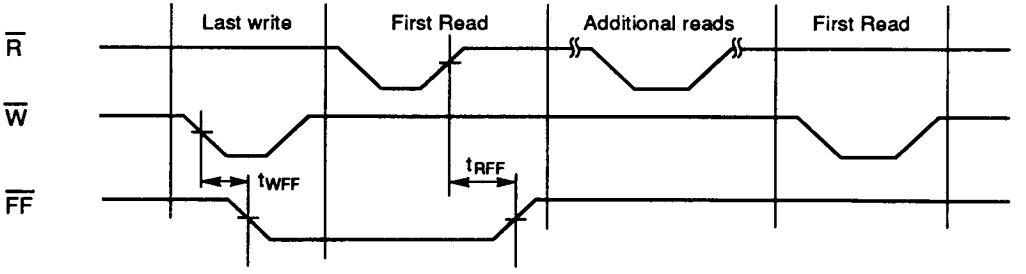


NOTES: 1. $\overline{W} = \overline{R} = V_{IH}$ during reset.
2. $t_{RSC} = t_{RST}, t_{RSR}$.

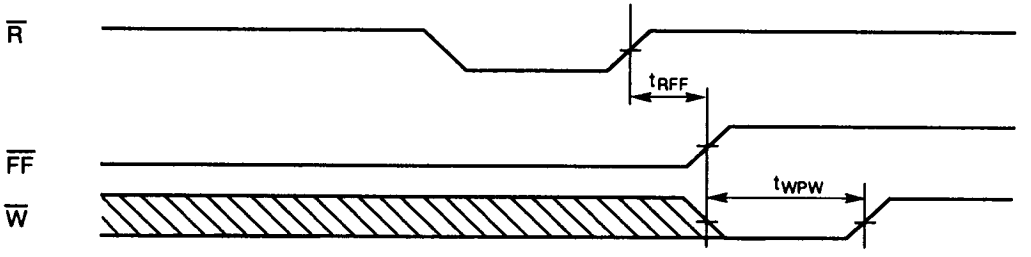
• **Retransmit Cycle**



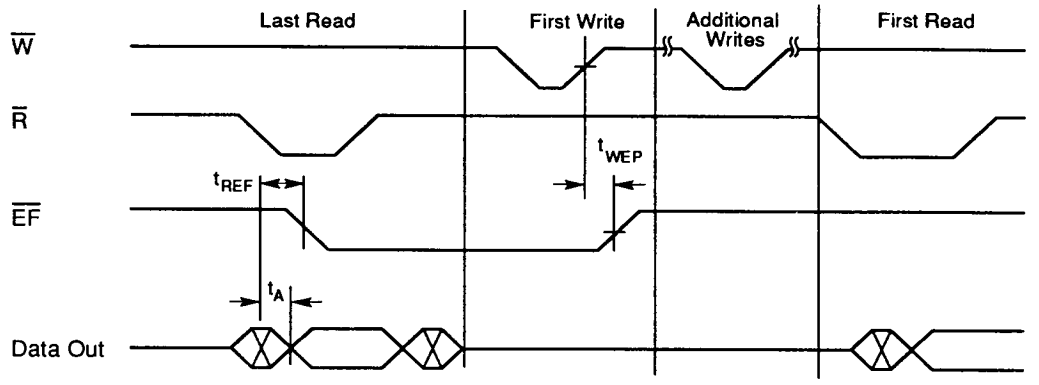
• **Full-Flag Cycle** (From Last Write to First Read)



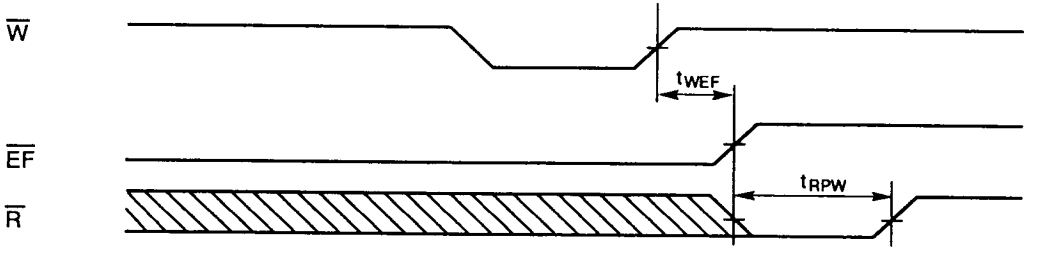
• **Full-Flag Cycle** (Effective Write Pulse Width After $\overline{FF}$ High)



• **Empty-Flag Cycle** (From Last Write to First Read)



• **Empty-Flag Cycle** (Effective Read Pulse Width After $\overline{EF}$ High)



• **Almost-Full Flag Cycle**