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C E M 5 5 3 0

30 CHANNEL SAMPLE & HOLD

Preliminary, January 1987

Description

The CEM 5530 is a 30 channel multiplexed Sample and Hold intended for generating multiple system control voltages or moderate speed multiplexed digital audio. Containing an auto zeroing op amp, analog multiplexer, 5 bit decoder, and 30 individual Sample and Holds capable of settling to 12 bits in under 2 uS, the 5530 can sample a voltage from a DAC into any one of its 30 outputs with less than 2 mV error from -5 to +5 volts.

Operation of the 5530 is straightforward: Bringing INH high puts all channels in the hold mode and causes the input op amp to auto zero. The DAC data and channel address are then changed, and while the DAC and decoder are settling, input offset is being nulled out. Finally, INH is brought low again to sample the input voltage into the addressed channel. As the auto zeroing process requires a minimum of 2 uS, every channel can be updated with full accuracy in less than 4 uS.

Each channel output can swing to within 2.5 volts of either supply, allowing -5 to +5 volt outputs with +/-7.5 volt supplies, or -2.5 to +2.5 volt outputs with +/-5 volt supplies. Ease of use is further enhanced with outputs which can handle moderate capacitive loading with little degradation in performance, and CMOS logic inputs which are TTL compatible regardless of supplies.

With all hold capacitors on-chip and requiring no external components, the CEM 5530 makes interface between microprocessor and voltage controlled devices exceptionally simple and economical.

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Features

- 30 Sample & Holds in a single 40 pin DIP
- 12 bit accuracy
- 16 bit linearity
- Acquisition to 12 bits in < 2 uS
- On-chip auto zeroing of input offset
- Low droop: 1 mV/mS max.
- Hold capacitors on-chip
- Supply independent TTL compatible CMOS inputs
- Large outputs: 10V with 15V supply
- Can handle capacitive loading without degrading performance

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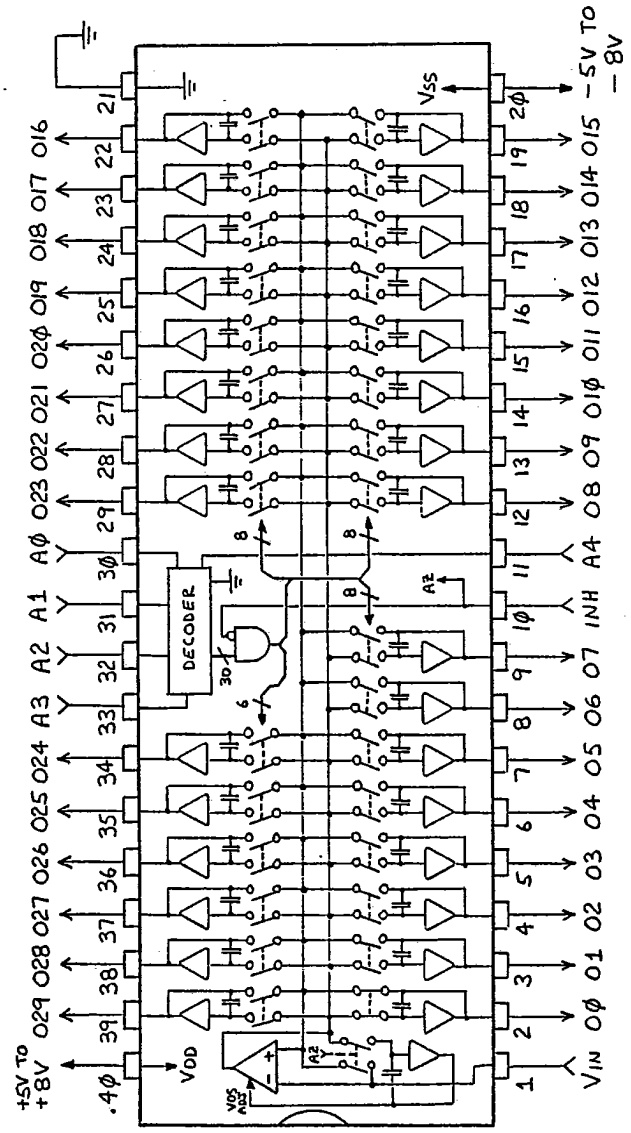

CEM 553Ø 3Ø CHANNEL SAMPLE & HOLD

2A

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CEM 5530 Preliminary Specifications

VDD = +8V VSS = -5V TA = 20°C

Parameter	Min.	Typical	Max.	Units
Acquisition Time [1]				
to 0.4%	---	1.2	---	uS
to 0.025%	---	2	---	uS
Auto Zero Time [2]	2	---	---	uS
Aperture Time [3]	---	100	---	nS
Aperture Jitter	---	10	---	nS
Address Hold Time	---	100	---	nS
Feedthrough	---	2	---	mV
Hold Step	---	5	---	mV
Input/Output Offset [4]	---	2	---	mV
Hold Droop	---	0.2	1	mV/mS
Channel Crosstalk [5]	-60	---	---	dB
Digital Noise Leakage [6]	---	2	---	m.V.R.M.S.
Voltage Range	-2.5	---	+5	V
Linearity	---	.01	---	%
Input Bias Current	---	---	1	nA
Input Capacitance	---	2	---	pF
Output Slew Rate	---	4	---	V/uS
Output Impedance	---	10	---	ohm
Output Source Drive	---	2	---	mA
Output Sink Drive [7]	---	0.3	---	mA
Logic Low Level	---	---	0.8	V
Logic High Level	2.8	---	---	V
Logic Input Current	---	---	1	uA
Max Logic Swings	-.5	---	VDD	V
Supply Voltage	10	---	15	V
Positive Supply Current	---	28	---	mA
Negative Supply Current	---	28	---	mA

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Notes: 1) For 5V output step change; the amplifier settling time is slightly less than this figure.

2) The INHIBIT logic signal must be at a high level at least this amount of time for the input amplifier to be properly auto-zeroed.

3) Address inputs and the voltage input may change only after this amount of time has elapsed upon INHIBIT returning to a high level (Hold Mode).

4) While in the sample or track mode for the channel being addressed (INHIBIT low).

5) Between adjacent channels. Crosstalk is lower between non-adjacent channels.

6) Digital noise consists mostly of narrow spikes coincident with input logic level transitions.

7) VSS - Vo = 2.5V

Power Supplies

As long as the maximum supply voltage between VDD (pin 40) and VSS (pin 20) is not allowed to exceed 16V, then the positive supply (VDD) may range from 4.5V to 10V, while the negative supply (VSS) may be between -4.5V and -10V. The values selected for the supplies affect the maximum input and output voltage swings before significant distortion: The maximum positive swing is 2.5V less than the positive supply, and the maximum negative swing is 2.5V above the negative supply. Thus, +8V supplies will accomodate inputs and outputs between +5V and $-5\overline{V}$, while +5V supplies will allow voltage swings between +2.5V and $-2.5\overline{V}$. Supplies need not be symetrical: For a 0 to +5V output, +8, -2.5V to -5V supplies may be used.

The threshold levels of all logic inputs are TTL compatible and unaffected by either supply.

Outputs

Each channel output can source up to 2mA for any positive supply. The output sink current capability, however, is dependent on the difference between the most negative output voltage excursion and the negative supply, according to the following:

$$Io^{-}(mA) = .1(VSS - Vo + 1)^2$$

Thus, for an output of Vo = -2.5V with VSS = -5V, the maximum sink current is 225uA (minimum load of 12K to ground); but for an output of 0V with VSS = -5V, the maximum sink current rises to 1.6mA. Since up to 2mA can be sourced by the outputs, the sink capability for low VSS-Vo differentials may be increased with an external pull down resistor to preferably a supply more negative than VSS. For example, a 10K resistor to -12V will provide 1mA source and sink capability (2.5K minimum load for $\pm$2.5V outputs).

The outputs can handle moderate capacitive loading up to 20pF. Much greater capacitances (up to 1uF) may be driven by isolating the output from the capacitive load with a 1K series resistor. Normally, long PC board traces from the outputs should be avoided; if not possible, a 1K isolation resistor physically positioned close to the 5530 is recommended.

Basic Operation and Timing

The basic channel update cycle, shown in Figure 1, begins with INHIBIT signal returning to a high level to disable the previous channel. The channel address and input voltage (normally from a DAC) must not be allowed to change until the aperture time, nominally 100nS, after INHIBIT becomes high. The length of time

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for which INHIBIT must remain high has two requirements: Since the input offset of the input op-amp is nulled out during this period, INHIBIT must remain high at least long enough for the auto-zeroing process to complete, or 2uS minimum. .The other constraint is that INHIBIT must remain high at least the address hold time (nominally 100nS) after the address has changed, to allow for address decoder settling. Normally, the new input voltage value also is allowed to settle out during this high period.

Then, when INHIBIT changes to its low state, the output of the addressed channel will change to equal the input voltage. The INHIBIT should remain low long enough for the Sample & Hold to acquire the new value to the desired resolution (acquisition time). If the input voltage has not finished settling by the time INHIBIT changes low, then INHIBIT should remain low for the acquisition time plus the additional time required for input settling. Normally, it is a good idea to keep INHIBIT high as long as possible, bringing it low only the amount of time required to properly refresh and update the channel Sample & Hold.

During the output hold time when INHIBIT is high or the channel is not being addressed, the output will change only at the droop rate; thus the complete cycle of auto-zero plus Sample & Hold acquisition should be repeated at intervals frequent enough to prevent the droop voltage (ripple) from exceeding the maximum desired amount.

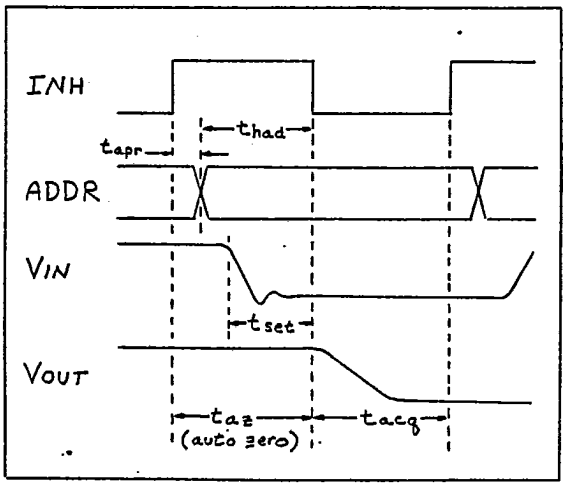

FIG. 1: CEM5530 TIMING