Am100480

16,384 x 1 IMOX™ ECL Bipolar RAM

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Fast access time (15 ns) — improves system cycle speeds.
- Enhanced output voltage level compensation providing 6X (improvement in) V_{OL} and V_{OH} stability over supply and temperature ranges.
- Internally voltage and temperature compensated providing flat AC performance.
- Fully compatible with 100K series ECL logic – no board changes required.
- Emitter follower outputs — easy wire-ORing
- Power dissipation decreases with increasing temperature.

GENERAL DESCRIPTION

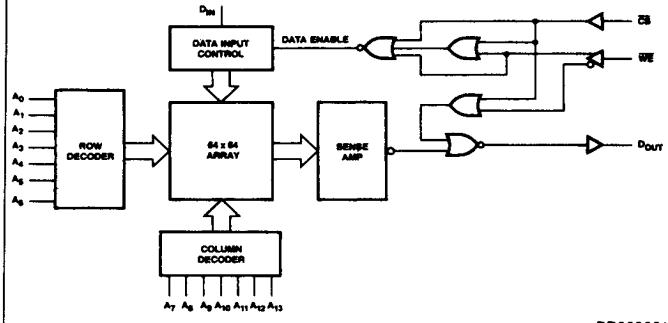
The Am100480-15 and Am100480-25 are fully decoded 16,384-bit ECL RAMs organized 16,384 words by one bit. Bit selection is achieved by means of a 14-bit address, A_0 through A_{13}. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write enable ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write enable lines are LOW, the data input (D_{IN}) is written into the addressed memory word.

Reading is performed with the chip select line LOW and the write enable line HIGH. The information stored in the addressed bit is read out on the noninverting output (D_{OUT}).

During the writing operation, or when the chip select line is HIGH, the output of the memory goes to a LOW state.

BLOCK DIAGRAM



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MODE SELECT TABLE

Input			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH
L = LOW
X = Don't Care

PRODUCT SELECTOR GUIDE

Highlights of Key Performance Parameters (Commercial)

Part Number	Am100480-15	Am100480-25
Address Access Time (t_{AA})	15 ns	25 ns
Write Pulse Width (t_W)	15 ns	25 ns
Write Recovery (t_{WR})	18 ns	20 ns
Chip Select Access/ Recovery and Write Disable Times (t_{ACS}, t_{RCS}, t_{WS})	8 ns	10 ns
Power Supply (I_{EE})	220 mA	200 mA

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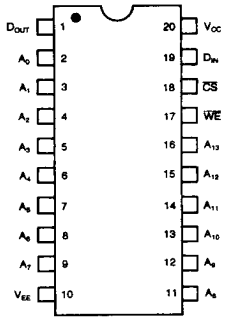
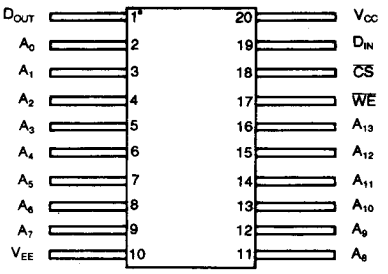
CONNECTION DIAGRAMS
Top View



CD006040



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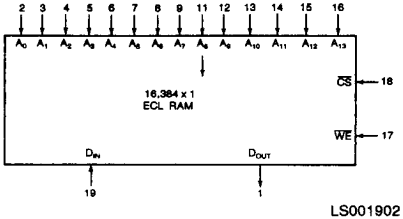
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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V_{CC} = Pin 20
V_{EE} = Pin 10

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

AM100480 -15 D C B

E. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to +85°C)

C. PACKAGE TYPE
D = 20-Pin Ceramic DIP (CD 020)
F = 20-Pin Flatpak (CF 020)

B. SPEED OPTION
-15 = 15 ns
-25 = 25 ns

A. DEVICE NUMBER/DESCRIPTION
Am100480
16,384 x 1 IMOX ECL Bipolar RAM

Valid Combinations	
AM100480-15	DC, DCB
AM100480-25	FC, FCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Case Temperature with
Power Applied ..... −55 to +125°C
V_{EE} Pin Potential to GND Pin ..... −7.0 V to +0.5 V
Input Voltage (DC) ..... V_{EE} to +0.5 V
Output Current (DC Output HIGH) .... −30 mA to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices (Note 2)
Temperature ..... 0 to +85°C
Supply Voltage ..... −5.7 V to −4.2 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS V_{EE} = −4.5 V, V_{CC} = GND (Note 2)

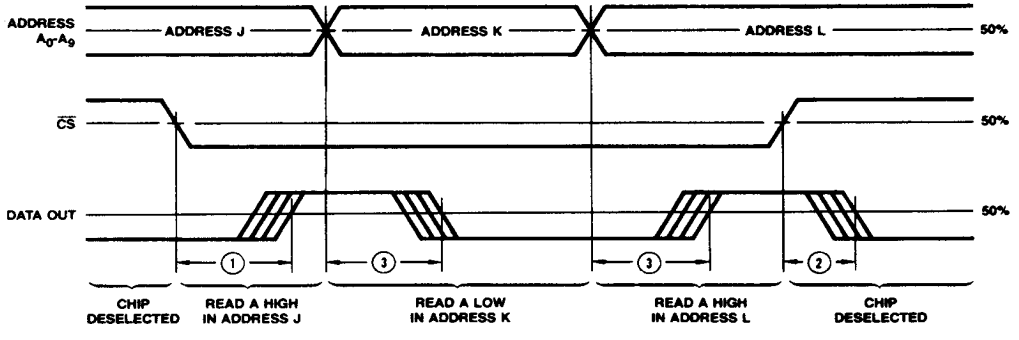
Parameter Symbol	Parameter Description	Test Conditions (Note 2)		B (Note 3)	Typ. (Note 1)	A (Note 3)	Units
V_{OH}	Output Voltage HIGH	V_{IN} = V_{IHA} or V_{ILB}	Loading is 50 Ω to −2.0 V	−1025	−955	−880	mV
V_{OL}	Output Voltage LOW			−1810	−1715	−1620	mV
V_{OHC}	Output Voltage HIGH	V_{IN} = V_{IHB} or V_{ILA}		−1035			mV
V_{OLC}	Output Voltage LOW					−1610	mV
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for All Inputs (Note 4)		−1165		−880	mV
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for All Inputs (Note 4)		−1810		−1475	mV
I_{IH}	Input Current HIGH	V_{IN} = V_{IHA}				220	µA
I_{IL}	Input Current LOW Chip Select ($\overline{CS}$)	V_{IN} = V_{ILB}		0.5		170	µA
	All Other Inputs			−50			
I_{EE}	Power Supply Current (Pin 10)	All Inputs and Outputs Open	Am100480-15	−220			mA
			Am100480-25	−200			

Notes: 1. Typical values are:
V_{EE} = −4.5 V, V_{CC} = GND, T_A = 25°C
2. Output Load = 50 Ω and 30 pF to −2.0 V, T_A = 0 to +85°C for DIPs. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Approximate resistance values of the package are:
θ_{JA} (Junction-to-Ambient) = 90°C/Watt (still air)
θ_{JA} (Junction-to-Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
T_C = 0 to +85°C for Flatpak and LCC packages
θ_{JC} (Junction-to-Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification: The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

SWITCHING CHARACTERISTICS V_{EE} = −4.8 V to −4.2 V, V_{CC} = GND (Note 2)

No.	Parameter Symbol	Parameter Description	Test Conditions	Am100480-15 Min.	Am100480-15 Typ. (Note 1)	Am100480-15 Max.	Am100480-25 Min.	Am100480-25 Typ. (Note 1)	Am100480-25 Max.	Units
READ MODE										
1	t_{ACS}	Chip Select Access Time	Measured at 50% of input to 50% of output			8			10	ns
2	t_{RCS}	Chip Select Recovery Time				8			10	
3	t_{AA}	Address Access Time				15			25	
WRITE MODE										
4	t_W	Write Pulse Width (to Guarantee Writing)	$t_{WSA} = t_{WSA}$ (Min.)	15			25			ns
5	t_{WSD}	Data Setup Time Prior to Write		2			5			ns
6	t_{WHD}	Data Hold Time After Write		3			5			ns
7	t_{WSA}	Address Setup Time Prior to Write	$t_W = t_W$ (Min.)	2			5			ns
8	t_{WHA}	Address Hold Time After Write		3			5			ns
9	t_{WSCS}	Chip Select Setup Time Prior to Write	Measured at 50% of input to 50% of output	2			5			ns
10	t_{WHCS}	Chip Select Hold Time After Write		3			5			ns
11	t_{WS}	Write Disable Time				8			10	ns
12	t_{WR}	Write Recovery Time				18			20	ns
RISE TIME AND FALL TIME										
13	t_r	Output Rise Time	Measured between 20% and 80% points		2.5			2.5		ns
14	t_f	Output Fall Time			2.5			2.5		
CAPACITANCE										
15	C_{IN}	Input Pin Capacitance	Measure with a pulse technique on sample basis		4			4		pF
16	C_{OUT}	Output Pin Capacitance			7			7		

SWITCHING WAVEFORMS (Cont'd.)



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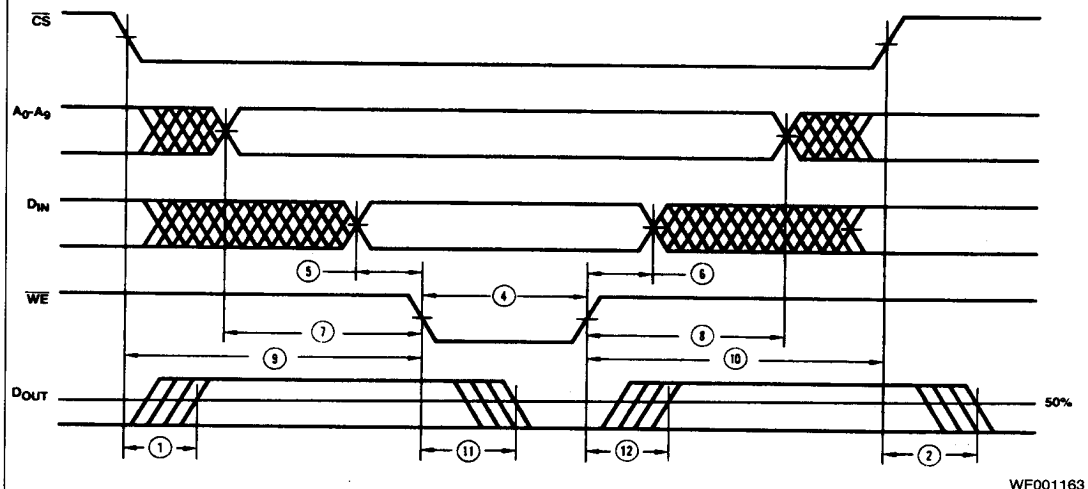
Read Mode

SWITCHING WAVEFORMS



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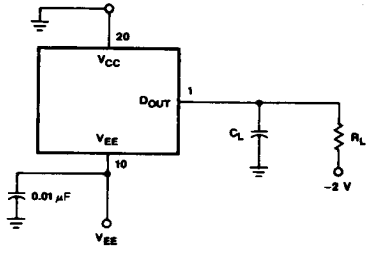
Write Mode

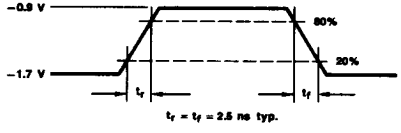
3

SWITCHING TEST CIRCUIT



TC000223

SWITCHING TEST WAVEFORM



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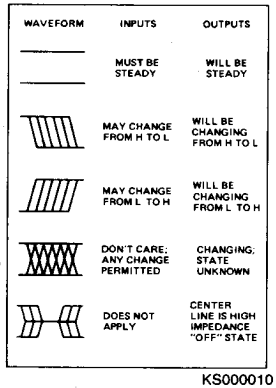
KEY TO SWITCHING WAVEFORMS



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R_L = 50 Ω termination of measurement system
C_L = 30 pF (including stray jig capacitance)