

**HEXFET® POWER MOSFET
 THRU-HOLE (Low-ohmic TO-257AA)**

**IRF7YSZ44VCM
 60V, N-CHANNEL**

Product Summary

Part Number	BVDSS	RDS(on)	ID
IRF7YSZ44VCM	60V	0.0195Ω	20A*

Seventh Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon unit area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

These devices are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high-energy pulse circuits.



**Low Ohmic
 TO-257AA**

Features:

- Low RDS(on)
- Avalanche Energy Ratings
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight

Absolute Maximum Ratings

	Parameter		Units
ID @ VGS = 10V, TC = 25°C	Continuous Drain Current	20*	A
ID @ VGS = 10V, TC = 100°C	Continuous Drain Current	20*	
IDM	Pulsed Drain Current ①	80	
PD @ TC = 25°C	Max. Power Dissipation	50	W
	Linear Derating Factor	0.4	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	71	mJ
IAR	Avalanche Current ①	20	A
EAR	Repetitive Avalanche Energy ①	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	1.6	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Lead Temperature	300 (0.063in./1.6mm from case for 10s)	
	Weight	4.3 (Typical)	g

* Current is limited by package

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	0.064	—	V/°C	Reference to 25°C, I _D = 250μA
R _{DSON}	Static Drain-to-Source On-State Resistance	—	—	0.0195	Ω	V _{GS} = 10V, I _D = 20A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	17	—	—	S (r)	V _{DS} = 15V, I _{DS} = 20A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	V _{DS} = 60V, V _{GS} = 0V
		—	—	250		V _{DS} = 48V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	50	nC	V _{GS} = 10V, I _D = 20A V _{DS} = 48V
Q _{gs}	Gate-to-Source Charge	—	—	18		
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	25		
t _{d(on)}	Turn-On Delay Time	—	—	20	ns	V _{DD} = 30V, I _D = 20A, V _{GS} = 10V, R _G = 9.1Ω
t _r	Rise Time	—	—	120		
t _{d(off)}	Turn-Off Delay Time	—	—	60		
t _f	Fall Time	—	—	90		
L _S + L _D	Total Inductance	—	6.8	—	nH	Measured from drain lead (6mm/ 0.25in. from package) to source lead (6mm/0.25in. from package)
C _{iss}	Input Capacitance	—	1730	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	375	—		
C _{rss}	Reverse Transfer Capacitance	—	60	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	20*	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	80		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _j = 25°C, I _S = 20A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	105	ns	T _j = 25°C, I _F = 20A, di/dt ≤ 100A/μs
Q _{RR}	Reverse Recovery Charge	—	—	220	nC	V _{DD} ≤ 25V ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

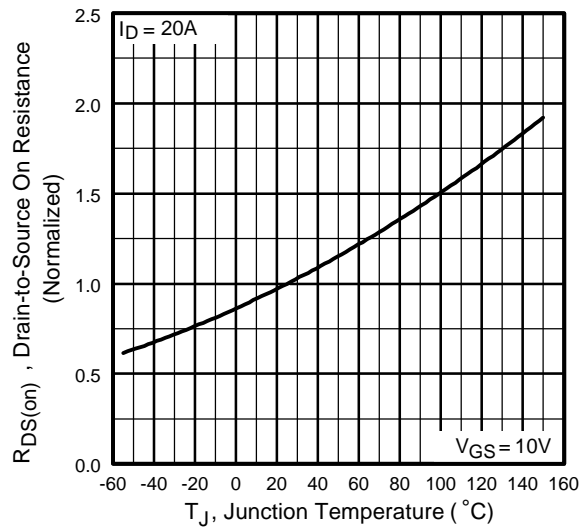
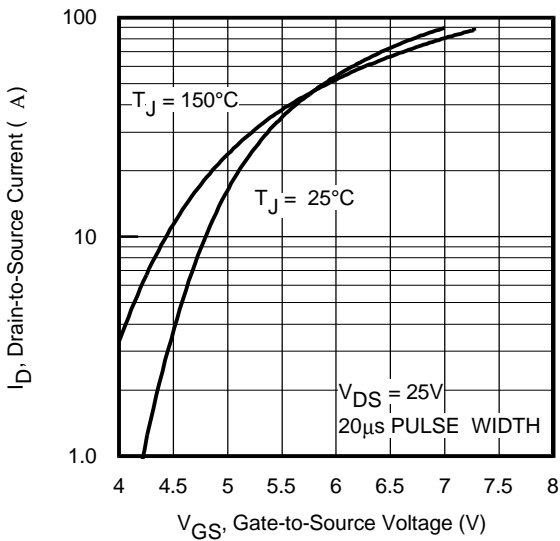
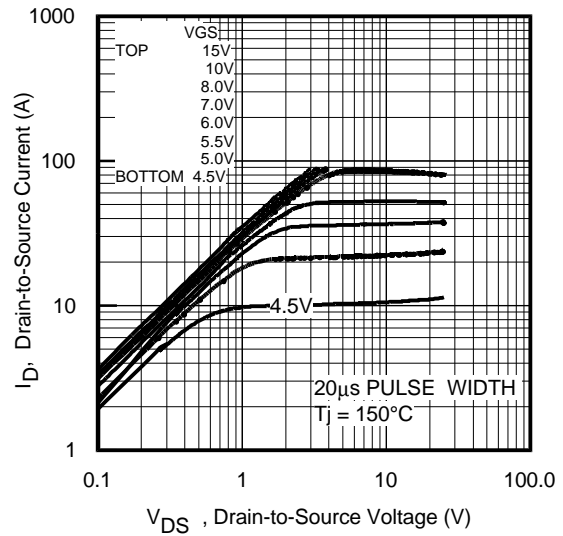
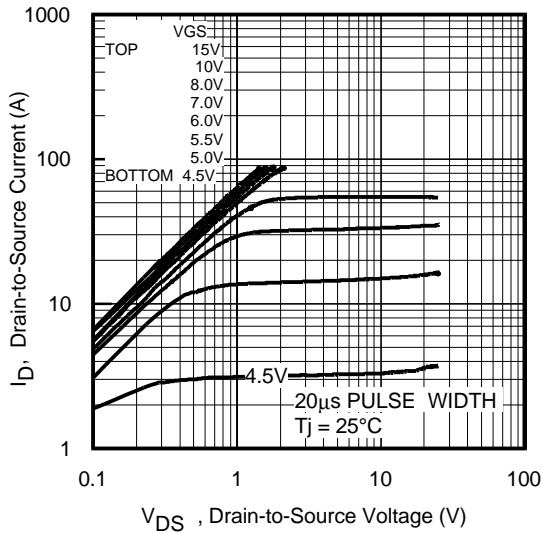
* Current is limited by package

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	2.5	°C/W	

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page



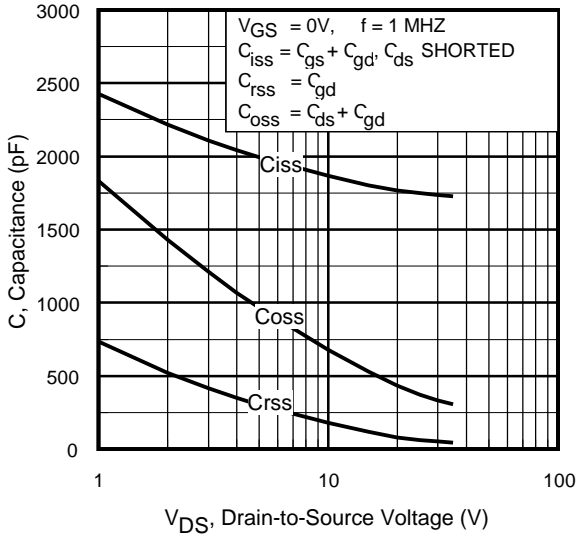


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

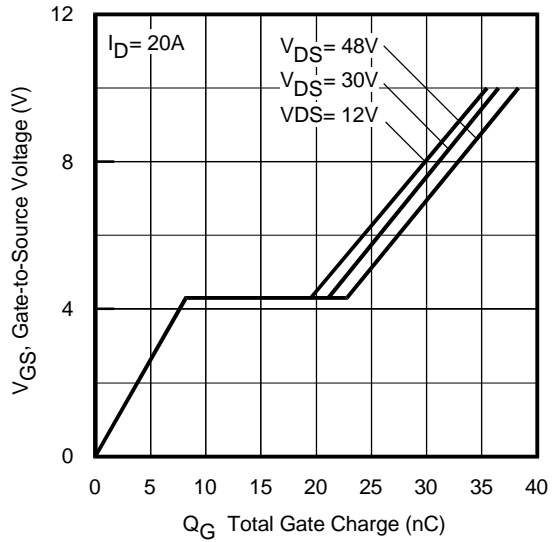


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

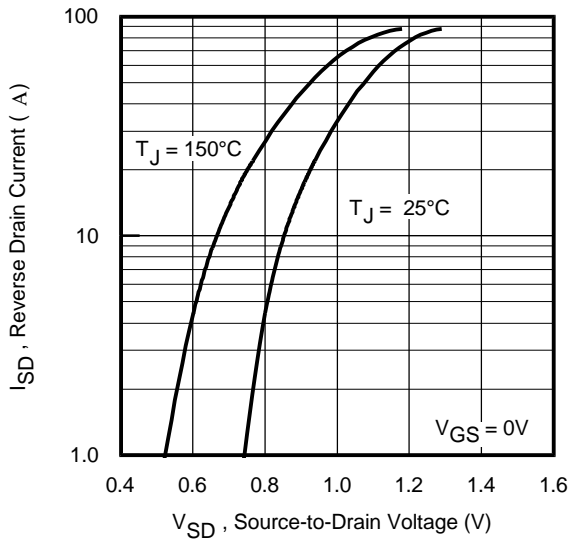


Fig 7. Typical Source-Drain Diode Forward Voltage

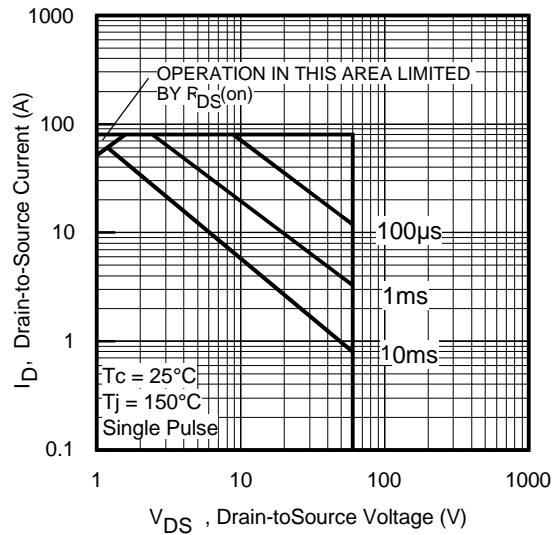


Fig 8. Maximum Safe Operating Area

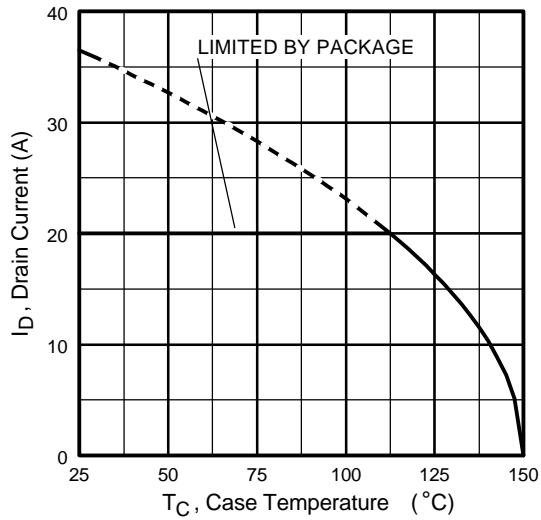


Fig 9. Maximum Drain Current Vs. Case Temperature

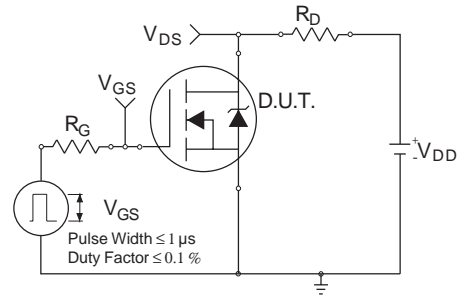


Fig 10a. Switching Time Test Circuit

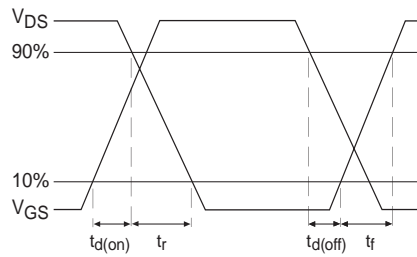


Fig 10b. Switching Time Waveforms

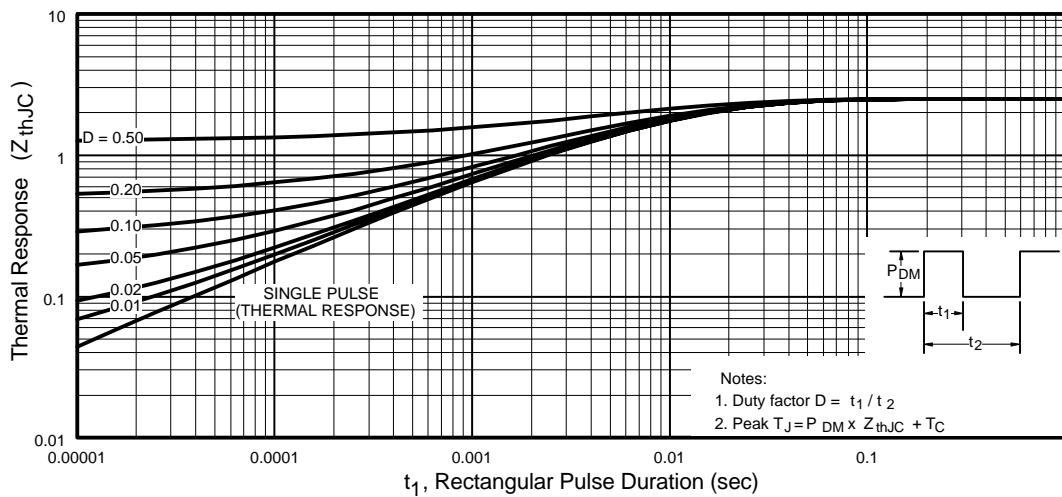


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

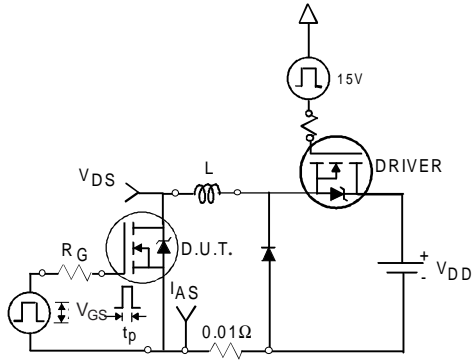


Fig 12a. Unclamped Inductive Test Circuit

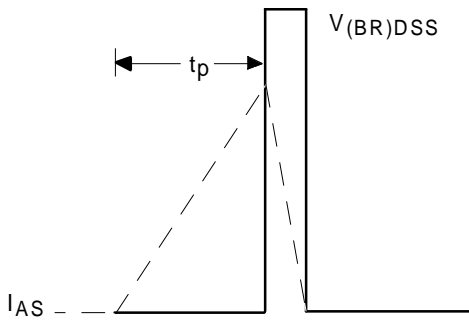


Fig 12b. Unclamped Inductive Waveforms

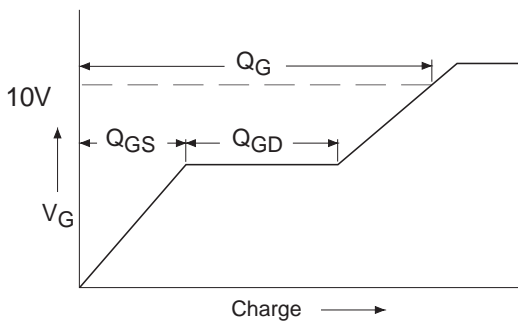


Fig 13a. Basic Gate Charge Waveform

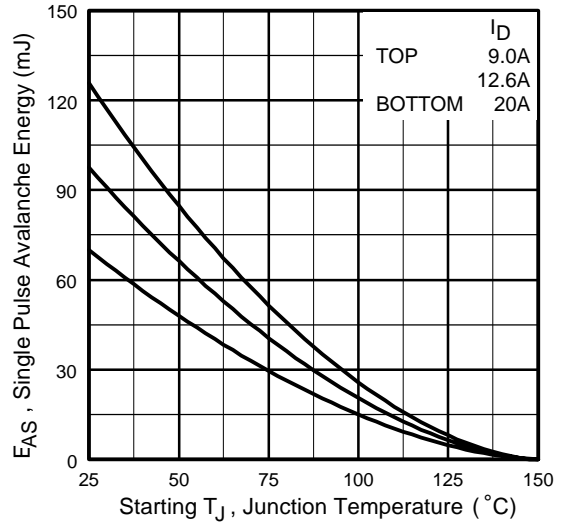


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

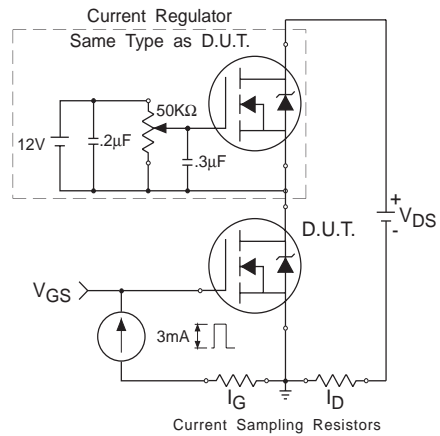
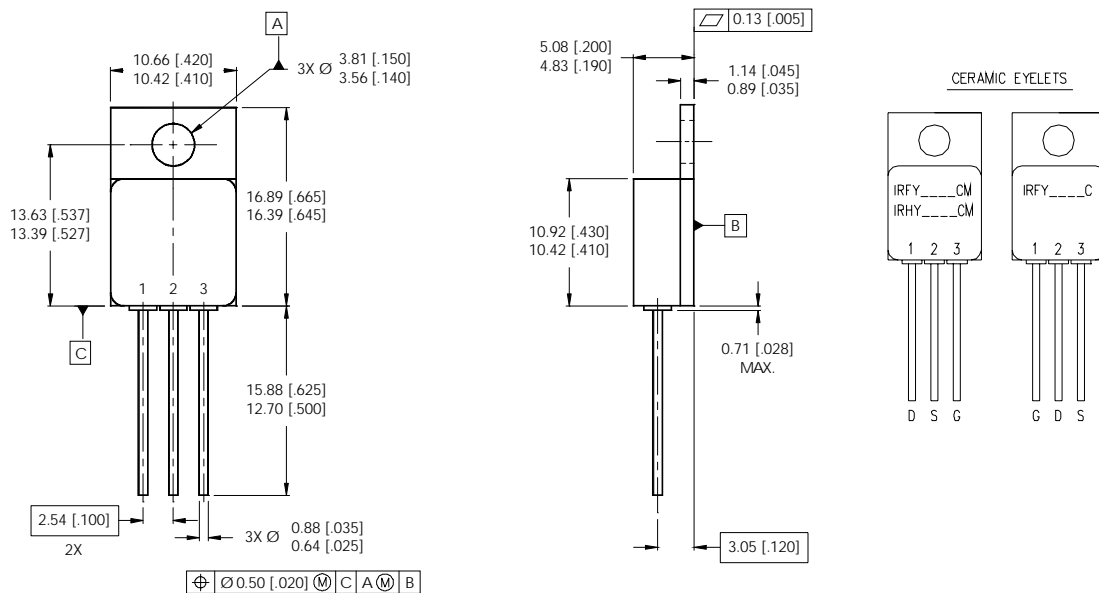


Fig 13b. Gate Charge Test Circuit

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 25\text{ V}$, Starting $T_J = 25^\circ\text{C}$, $L = 0.35\text{mH}$
Peak $I_{AS} = 20\text{A}$, $V_{GS} = 10\text{V}$, $R_G = 25\Omega$
- ③ $I_{SD} \leq 20\text{A}$, $di/dt \leq 310\text{A}/\mu\text{s}$,
 $V_{DD} \leq 60\text{V}$, $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\ \mu\text{s}$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions — Low-ohmic TO-257AA



NOTES:

- 1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994.
- 2. CONTROLLING DIMENSION: INCH.
- 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-257AA.

PIN ASSIGNMENTS

- 1 = DRAIN
- 2 = SOURCE
- 3 = GATE