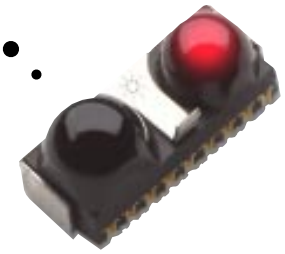
Agilent HSDL-3310
IrDA® Data Compliant
1.152 Mb/s Infrared Transceiver
Data Sheet



Functional Description

The HSDL-3310 is a small form factor infrared (IR) transceiver module that provides interface between logic and IR signals for through-air, serial, half-duplex IR data link. The module is compliant to IrDA physical layer specifications 1.3 and is IEC 825-Class 1 eye safe.

The HSDL-3310 is designed to interface with input/output logic circuits as low as 1.8 V.

The HSDL-3310 can be shut down completely to achieve very low power consumption. In the shut-down mode, the PIN diode will be inactive and thus producing very little photocurrent even under very bright ambient light. Also, HSDL-3310 incorporates adjust-able optical power feature to enhance low power consumption.

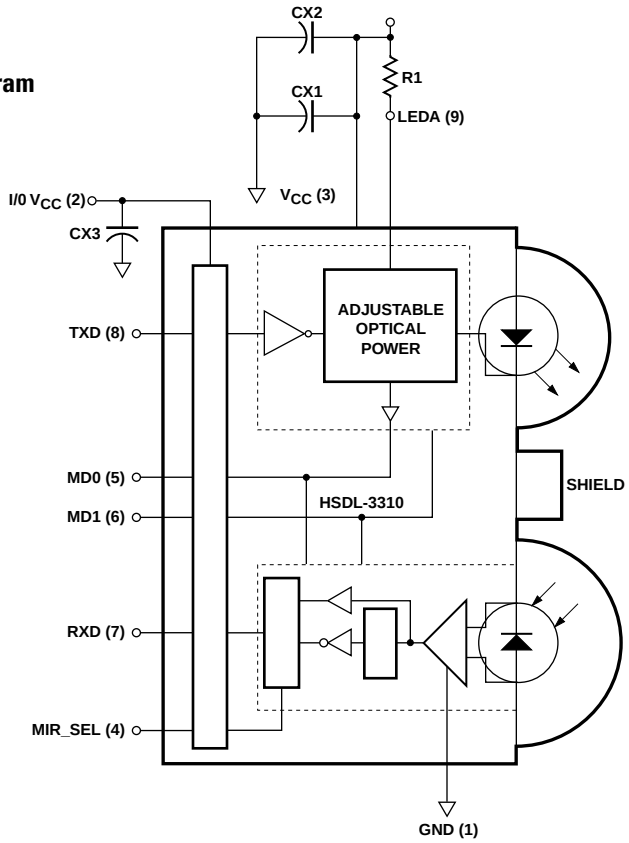
Applications

- **Mobile telecommunication**
  - **Cellular phone**
  - **Pager**
  - **Smart phone**
- **Data communication**
  - **PDA**
  - **Printer**
- **Digital imaging**
  - **Digital camera**
  - **Photo-imaging printer**
- **Electronic wallet**
- **Medical and industry data collection**

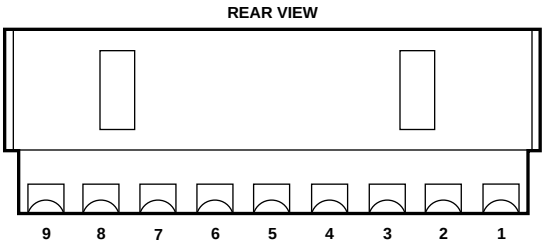
Features

- **Fully compliant to IrDA 1.3 specifications:**
  - **2.4 kb/s to 1.152 Mb/s**
  - **Excellent nose-to-nose operation**
  - **Typical link distance > 1.5 m**
- **Guaranteed temperature performance, –20 to 70 °C**
  - **Critical parameters are guaranteed over specified temperatures and supply voltages**
- **Low power consumption**
  - **Low shutdown current (10 nA typical)**
  - **Complete shutdown for TXD, RXD, and PIN diode**
- **Input/output interfacing voltage of as low as 1.8 V**
- **Small module size**
  - **4 x 10 x 5 mm max (H x W x D)**
- **Adjustable optical power management**
  - **Adjustable LED driver current for saving power while maintaining link integrity**
- **Typically withstands >100 mV_{p-p} power supply ripple**
- **V_{CC} supply 2.7 to 5.5 volts**
- **Integrated EMI shield**
- **LED stuck-high protection**

Functional Block Diagram



Pinout



I/O Pins Configuration Table

Pin	Symbol	Description	Note
1	GND	Ground	Connect to system ground.
2	I/OV_{CC}	Input/Output ASIC V_{CC}	Connect to ASIC logic controller V_{CC} voltage or supply voltage. The voltage at this pin must be equal to or less than supply voltage.
3	V_{CC}	Supply Voltage	Regulated 2.7 to 5.5 volts.
4	MIR_SEL	MIR Select	This pin to be driven high to select MIR mode and low for SIR mode. Do not float this pin.
5	MD0	Mode 0	This pin must be driven either high or low. Do not float this pin.
6	MD1	Mode 1	This pin must be driven either high or low. Do not float the pin.
7	RXD	Receiver Data Output. Active Low.	Output is a low pulse response when a light pulse is seen. Active low.
8	TXD	Transmitter Data Input. Active High.	Logic high turns the LED on. If held high longer than ~ 50 μs, the LED is turned off. TXD must be either driven high or low. Do not float this pin.
9	LEDA	LED Anode	Tied to external resistor, R1, to regulated V_{CC} from 2.7 to 5.5 volts.
–	SHIELD	EMI Shield	Do not connect shield directly to ground pin; connect to system ground via a low inductance trace.

Transceiver Control Truth Table

MD0	MD1	MIR_SEL	RXD	TXD
1	0	X	Shutdown	Shutdown
0	0	0	SIR	Full Distance Power
0	1	0	SIR	50 cm Distance Power
1	1	0	SIR	30 cm Distance Power
0	0	1	MIR	Full Distance Power
0	1	1	MIR	50 cm Distance Power
1	1	1	MIR	30 cm Distance Power

X = Don't care

Transceiver I/O Truth Table

		Inputs		Outputs	
Transceiver Mode	**MIR_SEL**	**TXD**	**EI**	**IE (LED)**	**RXD**
Active	X	$\geq V_{IH}$	X	High (On)	NV
Active	0	$\leq V_{IL}$	EI_H[1]	Low (Off)	Low[3]
Active	1	$\leq V_{IL}$	EI_H[2]	Low (Off)	Low[3]
Active	X	$\leq V_{IL}$	EI_L	Low (Off)	High
Shutdown	X	X[4]	Low (Off)	Low (Off)	NV[5]

X = Don't care NV = Not valid EI = In-Band infrared intensity at detector

Notes:
1. In-Band EI ≤ 115.2 kb/s and MIR_SEL=0
2. In-Band EI ≥ 0.576 Mb/s and MIR_SEL=1
3. Logic low is a pulsed response.
4. To maintain low shutdown current, TXD needs to be driven high or low and not to be left floating.
5. RXD is internally pull-up to V_{CC} through high impedance PMOS transistor (equivalent impedance is greater than 300 kΩ).

Recommended Application Circuit Components

Component	Recommended Value
R1	2.2 Ω ± 5%, 0.5 Watt, for 2.7 ≤ V_{CC} ≤ 3.3 V operation 2.7 Ω ± 5%, 0.5 Watt, for 3.0 ≤ V_{CC} ≤ 3.6 V operation 5.6 Ω ± 5%, 0.5 Watt, for 4.5 ≤ V_{CC} ≤ 5.5 V operation
CX1[1], CX3	0.47 µF ± 20%, X7R Ceramic
CX2[2]	6.8 µF ± 20%, Tantalum

Notes:
1. CX1 must be placed within 0.7 cm from HSDL-3310 for optimum noise immunity.
2. When using with noisy power supplies, supply rejection can be enhanced by including CX2 as shown in "HSDL-3310 Functional Block Diagram."

Caution: The component is susceptibile to damage from electrostatic discharge. It is advised that normal static precautions be taken during handling and assembling of this component to prevent damage and/or degradation, which may be caused by ESD.

Absolute Maximum Ratings

For implementations where case to ambient thermal resistance is ≤ 50°C/W.

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	–40	100	°C
Operating Temperature	T_A	–20	70	°C
LED Supply Voltage	V_{LED}	0	7	V
Supply Voltage	V_{CC}	0	7	V
Input/Output Voltage	I/OV_{CC}	0	7	V
Input Voltage: TXD, MD0, MD1	V_I	0	7	V
Output Voltage: RXD	V_O	–0.5	7	V

Recommended Operating Conditions

Parameter		Symbol	Min.	Max.	Units	Conditions
Operating Temperature		T_A	–20	70	°C	
Supply Voltage		V_{CC}	2.7	5.5	V	
Input/Output Voltage		I/OV_{CC}	1.8	5.5	V	
Logic Input Voltage for TXD, MD0, MD1,MIR_SEL	Logic High	V_{IH}	2/3 IOV_{CC}	IOV_{CC}	V	
	Logic Low	V_{IL}	0	1/3 IOV_{CC}	V	
Receiver Input Irradiance	Logic High	EI_H	0.0036	500	mW/cm^2	For in-band signals ≤ 115.2 kb/s[1]
			0.0090	500	mW/cm^2	0.576 Mb/s ≤ in-band signals ≤ 1.152 Mb/s[1]
	Logic Low	EI_L		0.3	$\mu W/cm^2$	For in-band signals
LED (Logic High) Current Pulse Amplitude		I_{LEDA}	400	600	mA	$V_{LED} = V_{CC} = 3.0$, V_I (TXD) ≥ V_{IH} MD0 = 0, MD1 = 0
Receiver Data Rate			0.0024	1.152	Mb/s	
Ambient Light						See IrDA Serial Infrared Physical Layer Link Specification, Appendix A for ambient levels

Electrical & Optical Specifications

Specifications (Min. and Max. values) hold over the recommended operating conditions unless otherwise noted. Unspecified test conditions may be within the operating range. All typical values (Typ.) are at 25°C with V_{CC} and IOV_{CC} set to 3.0 V unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Receiver						
Viewing Angle	$2\phi_{1/2}$	30			°	
Peak Sensitivity Wavelength	λ_p		880		nm	
RXD Output Voltage						
Logic High	V_{OH}	IOV_{CC} –0.2		IOV_{CC}	V	I_{OH} = –200 μA, EI ≤ 0.3 μW/cm^2
Logic Low	V_{OL}	0		0.4	V	I_{OL} = 200 μA
RXD Pulse Width (SIR)[2]	t_{RPW} (SIR)	1		7.5	μs	$\theta_{1/2} \leq 15°$, C_L = 9 pF
RXD Pulse Width (MIR)[3]	t_{RPW} (MIR)	200		750	ns	$\theta_{1/2} \leq 15°$, C_L = 9 pF
RXD Rise and Fall Times	t_r, t_f		25	100	ns	C_L = 9 pF
Receiver Latency Time[4]	t_L		25	50	μs	
Receiver Wake Up Time[5]	t_{RW}		18	100	μs	EI = 10 mW/cm^2
Transmitter						
Radiant Intensity	IE_H	100	220		mW/sr	I_{LEDA} = 400 mA, $\theta_{1/2} \leq 15°$, TXD ≥ V_{IH} . MD0 = 0, MD1 = 0, T_A = 25°C
Viewing Angle	$2\theta_{1/2}$	30		60	°	
Peak Wavelength	λ_p		875		nm	
Spectral Line Half Width	$\Delta\lambda_{1/2}$		35		nm	
TXD Logic Levels						
High	V_{IH}	2/3 IOV_{CC}		IOV_{CC}	V	
Low	V_{IL}	0		1/3 IOV_{CC}	V	
TXD Input Current						
High	I_H		0.02	1	μA	$V_I \geq V_{IH}$
Low	I_L	–1	–0.02	1	μA	$0 \leq V_I \leq V_{IL}$
LED Current						
Off	I_{VLED}		0.03	1	μA	$V_{VLED} = V_{CC}$ = 3.0 V, V_I(TXD) ≤ V_{IL} MD0 = 0, MD1 = 0
Wakeup Time[6]	t_{TW}		30	100	μs	
Maximum Optical Pulse Width[7]	$t_{PW(Max)}$		25	50	μs	
TXD Rise and Fall Time (Optical)	t_r, t_f			40	ns	t_{PW} (TXD) = 217 ns at 1.152 Mb/s
TXD Pulse Width (SIR)	t_{TPW} (SIR)	1.5	1.6	1.8	μs	t_{PW} (TXD) = 1.6 μs at 115.2 kb/s
TXD Pulse Width (MIR)	t_{TPW} (MIR)	148	217	260	ns	t_{PW} (TXD) = 217 ns at 1.152 Mb/s

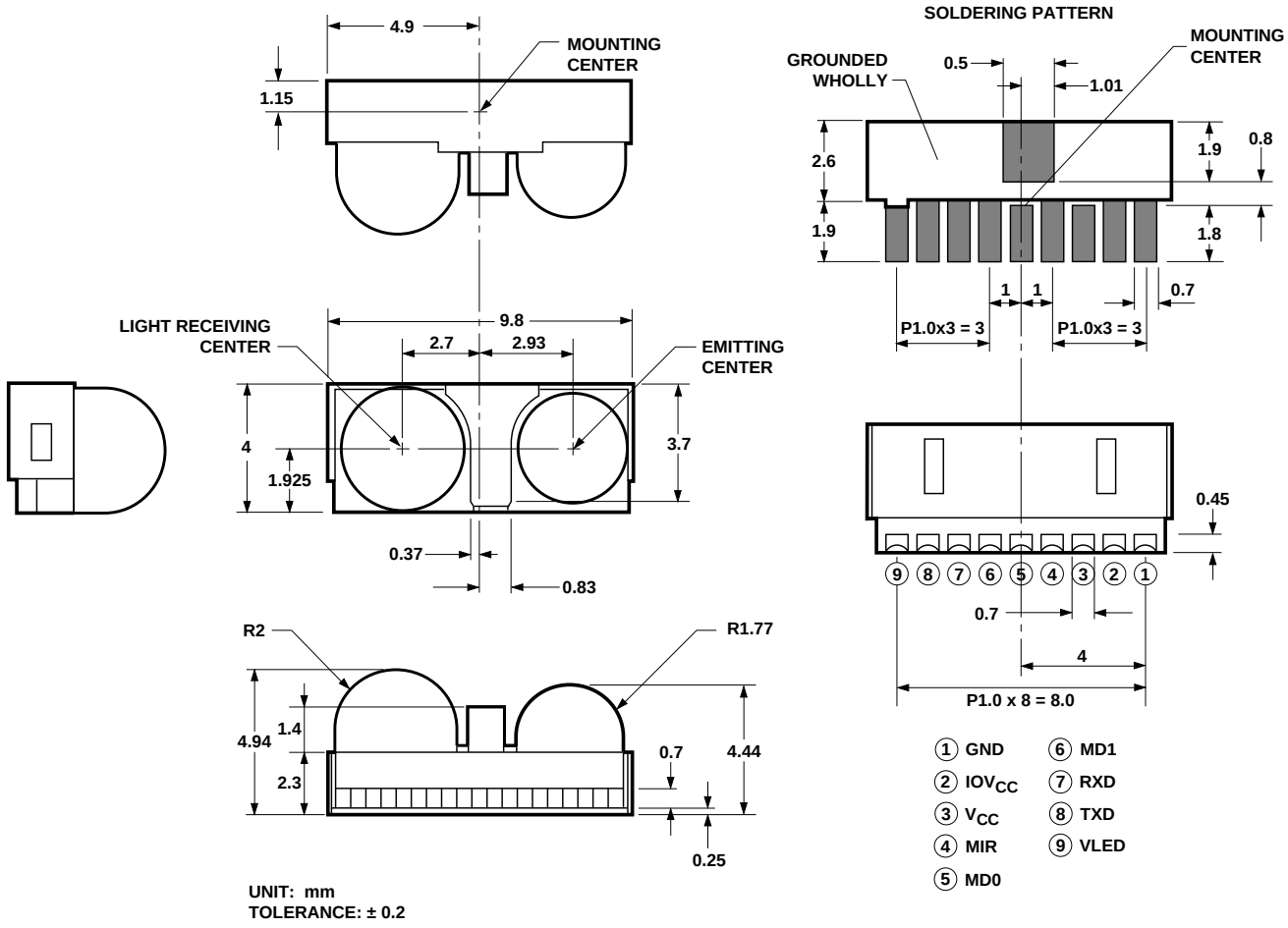
Transceiver

MD0, MD1, MIR_SEL Input Current	High	I_H		0.01	1	µA	$V_I \geq V_{IH}$, $V_{CC} = IOV_{CC} = 5$
	Low	I_L	–1	-0.02	1	µA	$0 \leq V_I \leq V_{IL}$, $V_{CC} = IOV_{CC} = 5$
Supply Current	Shutdown	I_{CC1}		0.01	1	µA	$V_{SD} \geq IOV_{CC} - 0.5$, $T_A = 25°C$, $V_{CC} = 5.0$ V
	Idle	I_{CC2}		290	400	µA	$V_I(TXD) \leq V_{IL}$, EI = 0
	Active	I_{CC3}		2	8	mA	$V_I(TXD) \leq V_{IL}$

Notes:

1. An in-band optical signal is a pulse/sequence where the peak wavelength, λp, is defined as 850 nm $\leq \lambda p \leq$ 900 nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification.
2. For in-band signals 2.41 kbps to 115.2 kbps where 3.6 µW/cm^2 ≤ EI ≤ 500 mW/cm^2.
3. For in-band signals 0.576 Mbps to 1.152 Mbps where 9 µW/cm^2 ≤ EI ≤ 500 mW/cm^2.
4. Latency is defined as the time from the last TXD light output pulse until the receiver has recovered its full sensitivity.
5. Receiver wake up time is measured from the MD0 pin high to low transition or MD1 pin low to high transition or V_{CC} power on to valid RXD output.
6. Transmitter wake up time is measured from the MD0 pin high to low transition or MD1 pin low to high transition or V_{CC} power on to valid light output in response to a TXD pulse.
7. Maximum optical pulse width is defined as the maximum time that the LED will remain on. This is to prevent the long LED turn on time.

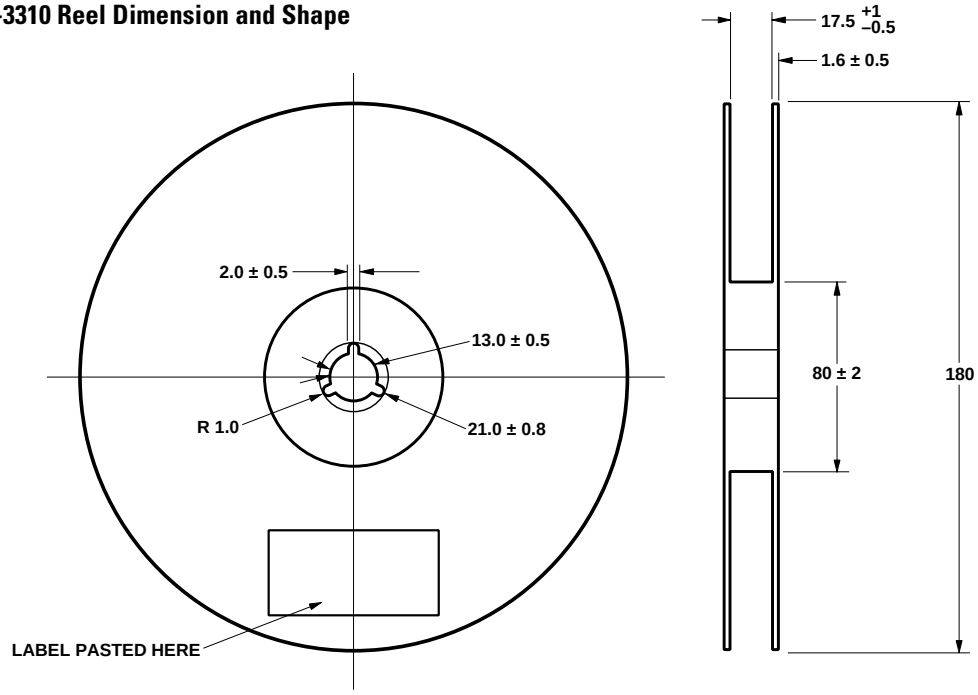
HSDL-3310 Package Outline with Dimensions and Recommended PC Board Layout



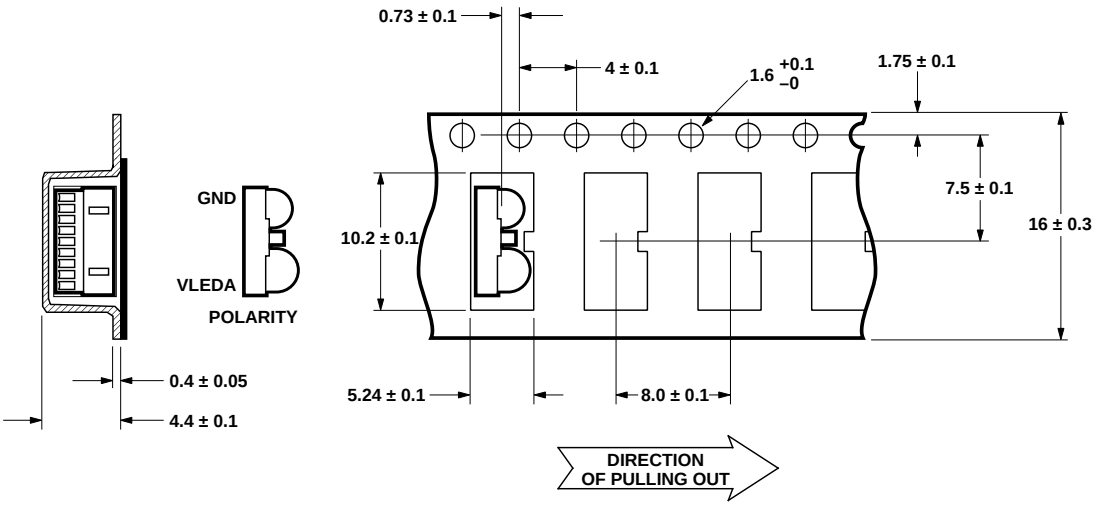
HSDL-3310 Ordering Information

Part Number	Package	Standard Package Increment
HSDL-3310#007	Front View	400
HSDL-3310#017	Front View	10

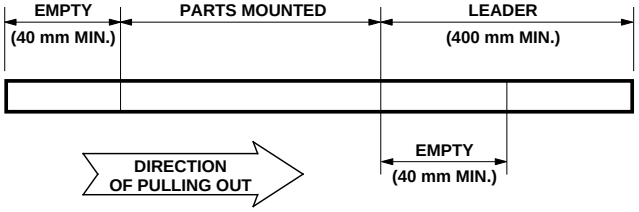
HSDL-3310 Reel Dimension and Shape



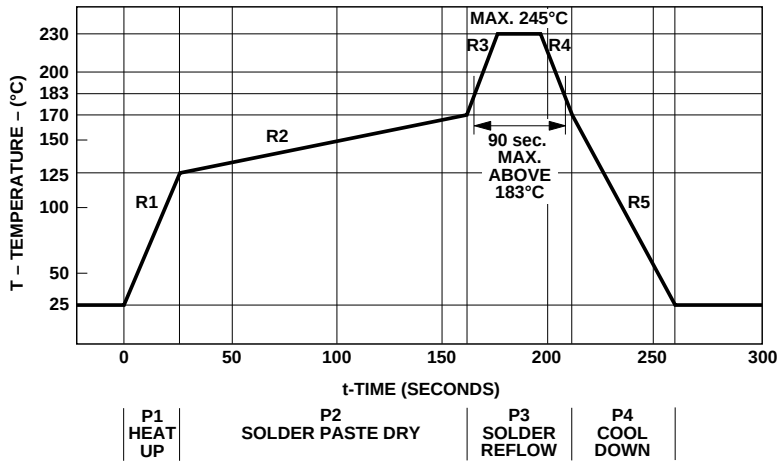
HSDL-3310 Tape and Carrier Dimensions



HSDL-3310 Tape Configuration



Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime
Heat Up	P1, R1	25°C to 125°C	4°C/s
Solder Paste Dry	P2, R2	125°C to 170°C	0.5°C/s
Solder Reflow	P3, R3	170°C to 230°C (245°C max.)	4°C/s
	P3, R4	230°C to 170°C	-4°C/s
Cool Down	P4, R5	170°C to 25°C	-3°C/s

The reflow profile is a straight line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates. The ΔT/Δtime rates are detailed in the above table. The temperatures are measured at the component to printed-circuit board connections. We recommend using convection (forced-medium) reflow instead of IR reflow to eliminate the possibility of delamination damage and shadow effects.

In **process zone P1**, the PC board and HSDL-3310 castellation I/O pins are heated to a temperature of 125°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 4°C per second to allow for even heating of both the PC board and HSDL-3310 castellation I/O pins.

Process zone P2 should be of sufficient time duration (> 60 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 170°C (338°F).

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 230°C (446°F) for optimum results. The dwell time above the liquidus point of solder should be between 15 and 90 seconds. It usually takes about 15 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 90 seconds, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 170°C (338°F), to allow the solder within the connections to freeze solid.

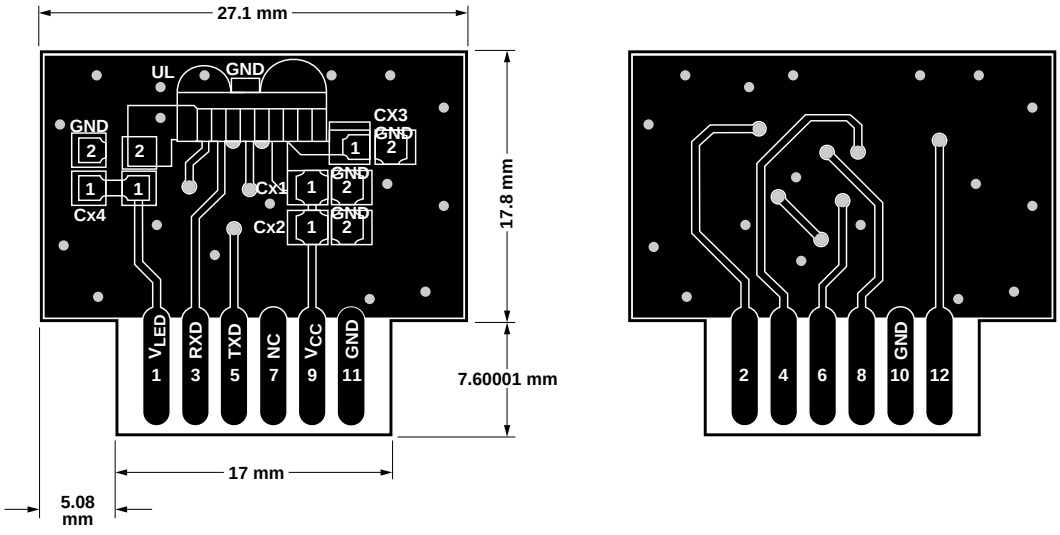
Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed –3°C per second maximum. This limitation is necessary to allow the PC board and HSDL-3310 castellation I/O pins to change dimensions evenly, putting minimal stresses on the HSDL-3310 transceiver.

PCB Layout Suggestion

The following PCB layout shows a recommended layout that should result in good electrical and EMI performance. Things to note:

1. In case a separate ground plane is available in a multi-layer board, the ground plane should be continuous under the part, but should not extend under the trace.
2. The shield trace is a wide, low inductance trace back to the system ground.
3. The AGND pin is connected to the ground plane and not to the shield tab.
4. C1 is an optional V_{CC} filter capacitor. It may be left out if the V_{CC} is clean.
5. V_{LED} can be connected to either unfiltered or unregulated power. If C1 is used, and if V_{LED} uses the same supply as V_{CC}, the connection should be made such that V_{LED} is filtered by C1 as well.

A reference layout of a 2-layer Agilent evaluation board for HSDL-3310 based on the guidelines stated above is shown below. For more details, please refer to Agilent Application Note 1114, *Infrared Transceiver PC Board Layout for Noise Immunity*, or to design guidelines in *Agilent IrDA Data Link Design Guide*.



TOP LAYER

BOTTOM LAYER

1.0 Solder Pad, Mask, and Metal Solder Stencil Aperture

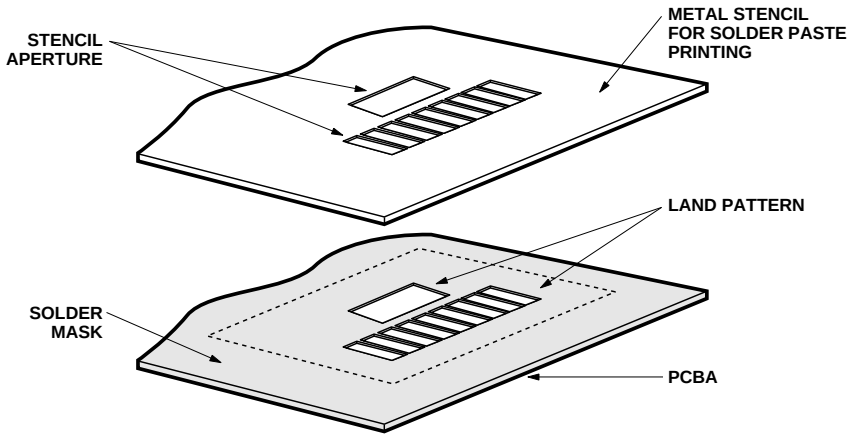


Figure 1. Stencil and PCBA.

1.1 Recommended Land Pattern for HSDL-3310

DIM.	mm	INCHES
a	2.40	0.095
b	0.65	0.026
c (PITCH)	1.00	0.039
d	1.80	0.071
e	1.70	0.067
f	3.71	0.146
g	3.66	0.144

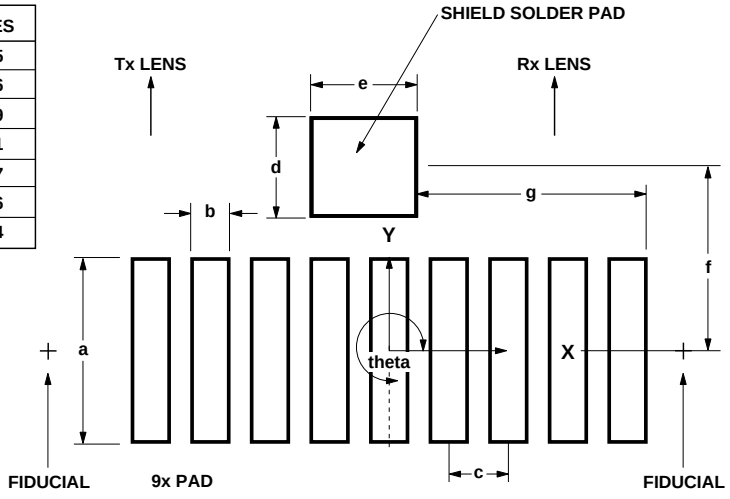


Figure 2. Top view of land pattern.

1.2 Adjacent Land Keepout and Solder Mask Areas

Dim.	mm	Inches
h	min. 0.2	min. 0.008
j	10.8	0.425
k	4.7	0.185
l	3.2	0.126

- Adjacent land keep-out is the maximum space occupied by the unit relative to the land pattern. There should be no other SMD components within this area.
- "h" is the minimum solder resist strip width required to avoid solder bridging adjacent pads.
- It is recommended that 2 fiducial cross be place at mid-length of the pads for unit alignment.

Note: Wet/Liquid Photo-Imageable solder resist/mask is recommended.

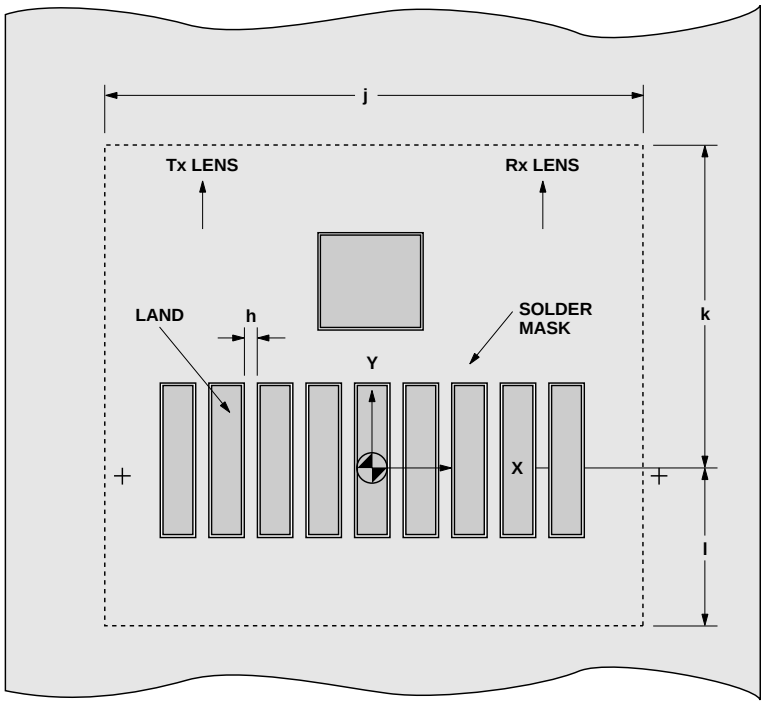


Figure 3. PCBA – Adjacent land keep-out and solder mask.

2.0 Recommended Solder Paste/ Cream Volume for Castellation Joints

Based on the evaluation for HDSL-3600, the printed solder paste volume required per castellation pad is 0.30 cubic mm (based on either no-clean or aqueous solder cream types with typically 60 to 65% solid content by volume).

2.1 Recommended Metal Solder Stencil Aperture

It is recommended that only 0.152 mm (0.006 inch) or 0.127 mm (0.005 inch) thick stencil be used for solder paste printing. This is to ensure adequate printed solder paste volume and no shorting. The following combination of metal stencil aperture and metal stencil thickness should be used:

See Figure 4.0			
t, Nominal Stencil Thickness		**l, Length of Aperture**	
mm	**inches**	**mm**	**inches**
0.152	0.006	3.0 ± 0.05	0.12 ± 0.002
0.127	0.005	3.7 ± 0.05	0.15 ± 0.002
w, the width of aperture is fixed at 0.65 mm (0.026 inch)			
Aperture opening for shield pad is 1.8 mm x 1.8 mm as per land dimension.			

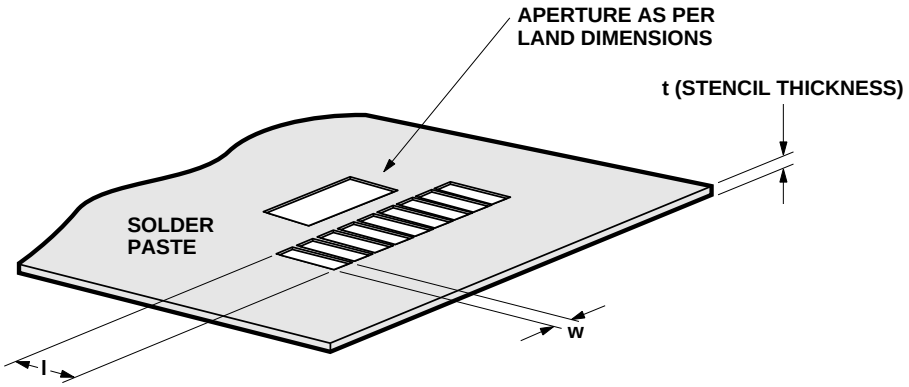


Figure 4. Solder paste stencil aperture.

Moisture-Proof Packaging

The HSDL-3310 is shipped in moisture-proof packaging. Once opened, moisture absorption begins.

Recommended Stortage Conditions

Storage Temperature	10°C to 30°C
Relative Humidity	Below 60% RH

Time from Unsealing to Soldering

After removal from the bag, the parts should be soldered within two days if stored at the recommended storage conditions. If the parts have been removed from the bag for more than two days, the parts must be stored in a dry box.

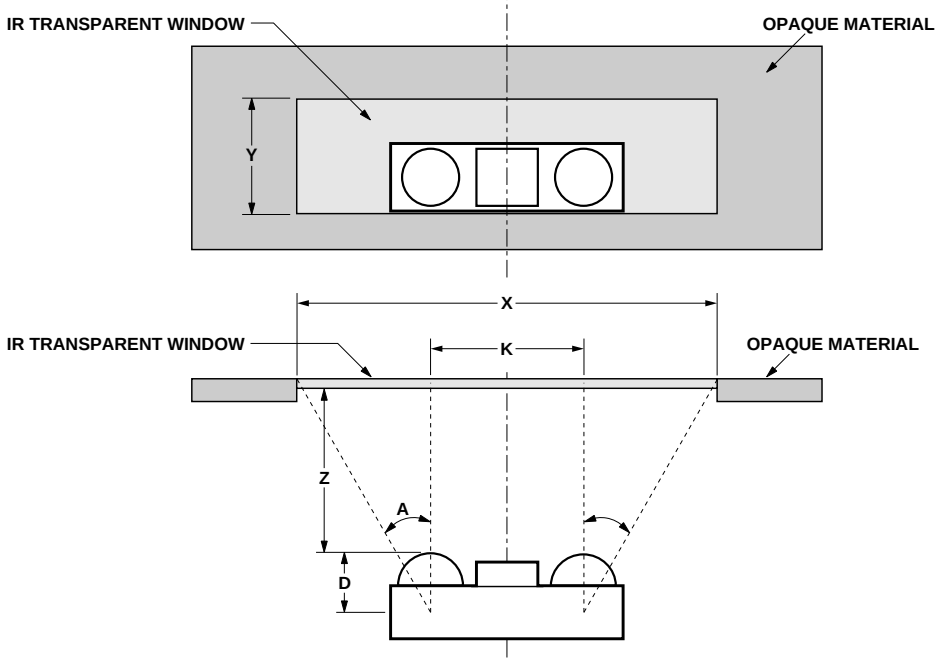
Baking

If the parts are not stored in a dry environment, they must be baked before reflow process to prevent damage to parts. Baking should be done only once.

Packaging	Baking Temperature	Baking Time
In Reel	10°C	≥ 48 hours
	100°C	≥ 4 hours
In Bulk	125°C	≥ 2 hours
	150°C	≥ 1 hour

Optical Port Dimensions for HSDL-3310

To ensure IrDA compliance, some constraints on the height and width of the window exist. The minimum dimensions ensure that the IrDA cone angles are met without vignetting. The maximum dimensions minimize the effects of stray light. The minimum size corresponds to a cone angle of 30° and the maximum size corresponds to a cone angle of 60°.



In the figure above, X is the width of the window, Y is the height of the window, and Z is the distance from the HSDL-3310 to the back of the window. The distance from the center of the LED lens to the center of the photodiode lens, K, is 5.63 mm. The equations for computing the window dimensions are as follows:

$X = K + 2*(Z + D)*\tan A$
$Y = 2*(Z + D)*\tan A$

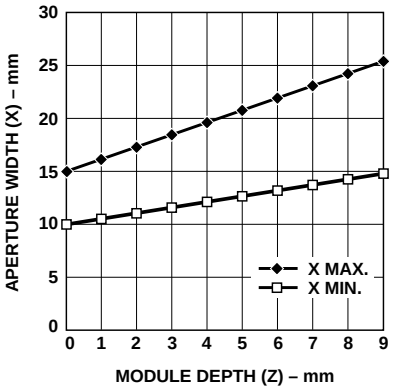
The above equations assume that the thickness of the window is negligible compared to the distance of the module from the back of the window (Z). If they are comparable, Z' replaces Z in the above equation. Z' is defined as

$Z' = Z + t/n$

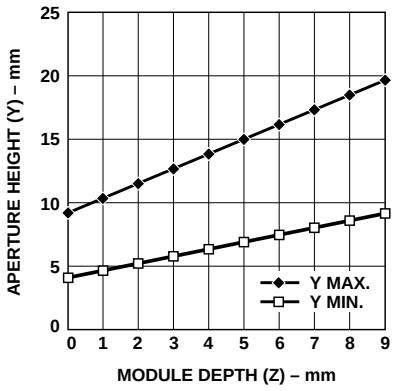
where 't' is the thickness of the window and 'n' is the refractive index of the window material.

The depth of the LED image inside the HSDL-3310, D, is 8 mm. 'A' is the required half angle for viewing. For IrDA compliance, the minimum is 15° and the maximum is 30°. These equations result in the following tables and graphs:

Module Depth (Z) mm	Aperture Width (X) mm		Aperture Height (Y) mm	
	Max.	Min.	Max.	Min.
0	14.8676	9.917187	9.237604	4.287187
1	16.0223	10.45309	10.3923	4.823085
2	17.17701	10.98898	11.54701	5.358984
3	18.33171	11.52488	12.70171	5.894882
4	19.48641	12.06078	13.85641	6.430781
5	20.64111	12.59668	15.01111	6.966679
6	21.79581	13.13258	16.16581	7.502577
7	22.95051	13.66848	17.32051	8.038476
8	24.10521	14.20437	18.47521	8.574374
9	25.25991	14.74027	19.62991	9.110273



Aperture width (X) vs. module depth.



Aperture height (Y) vs. module depth.

Window Material

Almost any plastic material will work as a window material. Polycarbonate is recommended. The surface finish of the plastic should be smooth, without any texture. An IR filter dye may be used in the window to make it look black to the eye, but the total optical loss of the window should be 10 percent or less for best optical performance. Light loss should be measured at 875 nm.

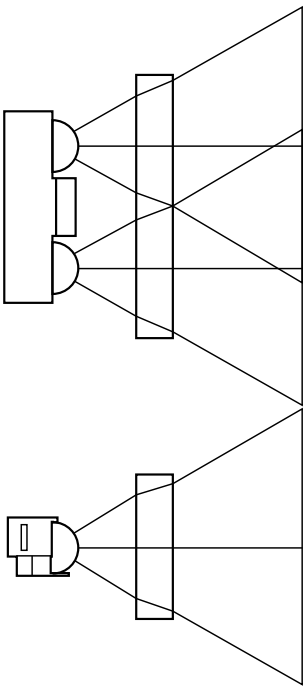
Shape of the Window

From an optics standpoint, the window should be flat. This ensures that the window will not alter either the radiation pattern of the LED, or the receive pattern of the photodiode.

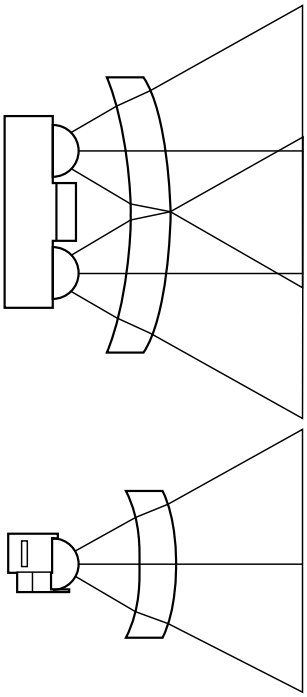
If the window must be curved for mechanical or industrial design reasons, place the same curve on the back side of the window that has an identical radius as the front side. While this will not completely eliminate the lens effect of the front curved surface, it will significantly reduce the effects. The amount of change in the radiation pattern is dependent upon the material chosen for the window, the radius of the front and back curves, and the distance from the back surface to the transceiver. Once these items are known, a lens design can be made which will eliminate the effect of the front surface curve.

The following drawings show the effects of a curved window on the radiation pattern. In all cases, the center thickness of the window is 1.5 mm, the window is made of polycarbonate plastic, and the distance from the transceiver to the back of the window is 3 mm.

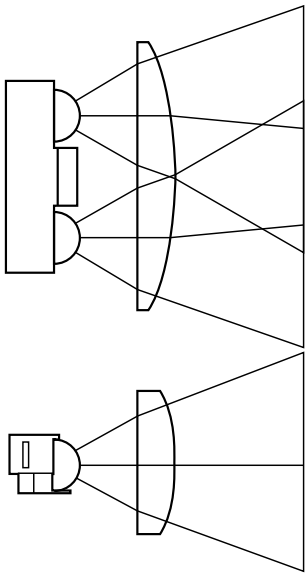
Flat Window
(First Choice)



Curved Front and Back
(Second Choice)



Curved Front, Flat Back
(Do Not Use)



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